B R O O K T R E E

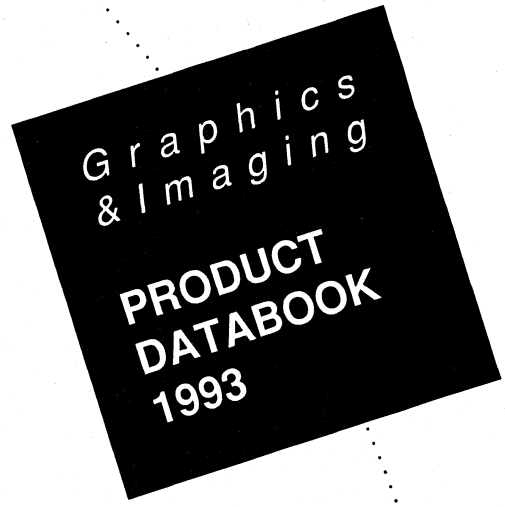
GRAPHICS AND IMAGING

PRODUCT DATABOOK

Quick Reference to Products

* Information on this product can be found in Brooktree's ATE Databook.

BROOKTREE



Thank you for your interest in Brooktree products.

Our commitment is to provide a steady stream of innovative products that offer the highest quality, lowest cost/performance solutions and back them with comprehensive support services. These include timely and accurate technical information and responsive, experienced applications assistance.

At Brooktree, listening to our customer's requirements is what we do first. Solving our customer's problems is what we do best.

CONTENTS

Brooktree®

Section 1

INTRODUCTION

Brooktree®

Company Facts

Brooktree began operations in 1983 following its development of an advanced architecture for data conversion. The architecture, invented by company cofounder and chief scientist Henry Katzenstein, permits the combination of high-performance analog and digital circuitry on a single monolithic Integrated Circuit (IC), which can be manufactured with standard bipolar or CMOS processes.

Brooktree is a publicly held company (NASDAQ:BTRE) located in San Diego, California. Facilities of 148,000 square feet house all design, test, and quality assurance activities as well as marketing, sales, and administration. Brooktree has established a worldwide network of distributors and factory representatives with offices in the United States, Europe, and the Far East.

The company's products are manufactured under agreement with several domestic and international foundry sources. Second-source agreements are in effect with a number of suppliers.

Since its first volume shipments in 1985, Brooktree has achieved leadership share in the workstation graphics market and a large share of the markets for PC graphics and electronic imaging.

Products

Our first product, introduced in early 1985, was a 75 MHz 8-bit CMOS Video Digital-to-Analog Converter (VIDEODAC). By mid-1985, Brooktree had introduced six CMOS VIDEODAC products (our VIDEODAC line) to the high-performance graphics market. Further system integration led to our family of RAMDACs, which combine triple VIDEODACs, color palette RAMs, and pixel input multiplexers on a single chip. Today, Brooktree has the broadest range of RAMDACs available on the market.

In 1988, Brooktree entered the imaging market with its first CMOS flash video A/D converter. Further system-level integration led to our family of image digitizers, which combine one or more A/D converters and many additional functions required to digitize a video signal. In 1991, Brooktree announced its first video encoder that allows workstation and PC users to convert high-quality computer graphics/video into format for output to TV monitors and videotape. This new video product will be joined by a variety of future ICs from Brooktree that will provide customers with system-level solutions for developing desktop video hardware.

Other product families from Brooktree include ICs for automatic test equipment and data communication systems. For further information on these products, please call your local sales representative or the Brooktree factory.

Strategy

Brooktree will combine the elements of its high-performance mixed-signal design capabilities and proprietary test technology to provide a unique family of application-specific products. The company will continue to develop highly integrated products for use in computer graphics and imaging while exploring other applications where its mixed-signal technology can be applied.

Data Sheet Designations

Advance Information

This is the first official information released about a potential product. The datasheet contains basic information about the product and contains the target parametric and functional specifications. It usually precedes sample devices by approximately six months. This datasheet has the phrase "Advance Information" in the upper left corner on the front page.

Preliminary Information

This datasheet is released with sample devices. It contains a more extensive discussion of device operation and provides more complete parametric information. The functional operation is fully defined and the parametric information is the result of early testing of the initial devices. Not all of the parametric specifications may be fully tested or characterized. This datasheet has the phrase "Preliminary Information" in the upper left corner on the front page.

Final datasheet

This datasheet evolves from the Preliminary Information datasheet. It is a result of test information collected from fully characterized devices. This datasheet is distinguished by the absence of any designation, except the part number, at the top of the front page.

Device Designations

Engineering Sample

Devices which have exhibited most of the functionality for which it was designed. Engineering samples are used to enable selected customers to evaluate the device as early as possible. While some of the AC and DC parameters may be tested, the accuracy or completeness of the testing is not guaranteed. In addition, the product has not been put through Brooktree's quality and reliability testing. They have standard markings with an additional "ES" marked on top of the package. These devices have a Preliminary datasheet under document control.

Pre-Qual

These devices have production silicon, testing, and burn-in. Most characterization is done, but the device must still pass a QA life-test qual. These devices have standard markings with an additional "PQ" marked on top of the package. These devices have a Preliminary datasheet under document control.

Full Production

These devices have production silicon, testing, burn-in, and have successfully passed a QA life-test qual. These devices have standard markings with no additional designators. These devices have a Final datasheet under document control.

Section 2

QUALITY ASSURANCE

Introduction

Brooktree Corporation is committed to being the supplier of choice in all markets it pursues. Meeting or, indeed, exceeding all requirements and expectations of its customers is necessary to accomplish this goal. This is a bold statement that requires the highest levels of quality and reliability in all aspects of our business. Many definitions have been offered for the terms "quality" and "reliability," but Brooktree believes these terms can only be measured by the overall level of end-customer satisfaction. Endeavoring to achieve its stated objectives, Brooktree strives to create close, strategic relationships with its customers. In this way, requirements and expectations can be clearly defined, and the achievement of quality can be more easily realized.

Quality is a critical aspect of product success, and Brooktree has established an aggressive schedule of measuring, testing, and monitoring its products and processes to guarantee all customer requirements are met and to ensure continuous improvement. Substantial investments in experienced personnel and state-of-the-art capital equipment have been made in all areas of the company to ensure quality and reliability are designed and built into all Brooktree product.

Quality Assurance Program

Ensuring the quality of a Brooktree product is a many-faceted task. The Brooktree Quality Assurance Program incorporates all elements of the supply chain, from raw material suppliers to subcontractors, internal operations, and, most importantly, the customers. The program starts with the understanding and documentation of customer requirements. Every attempt is made to understand these requirements and to translate them into Brooktree operating procedures and specifications. When these requirements have been documented, they are communicated to the relevant operating departments for incorporation into production operations. The Quality Assurance Department reviews every lot before it is shipped to verify all customer requirements have been satisfied.

The quality of Brooktree's suppliers is considered a key factor contributing to overall product quality. Therefore, the extension of the Quality Assurance Program to suppliers and subcontractors is especially critical to Brooktree products. The reason for this is evident in Figure 1, the manufacturing flow. Brooktree uses subcontractors to perform its core manufacturing operations (wafer fabrication and device assembly). This requires that Brooktree form tight, strategic relationships with its suppliers (subcontractors). Strong emphasis is placed on process capability and control. Brooktree works closely with its subcontractors to achieve these goals, employing such techniques as design of experiments and statistical process control. Suppliers' performance is consistently measured based on their own data as well as data collected from Brooktree-performed process monitors and audits.

Another measure of quality is product conformance to published specifications. This is determined by measuring the percentage of defects in a given sample size. The Quality Assurance Program includes material inspections that employ statistically valid sample plans. These sampling plans are determined to ensure, with a high degree of statistical confidence, enough data is collected to estimate the defect level of the overall population of product being shipped. This data collection is ongoing and is used to drive continuous improvement in the products and processes used during manufacturing. Pareto analysis is performed on a regular basis to determine the largest contributors to the overall defect level. Then, corrective action is taken to improve any processes necessary and to eliminate that type of defect.

All quality requirements and manufacturing process controls are documented in Brooktree-controlled specifications and procedures. The Document Control Department manages these documents and controls the process by which these requirements and controls are changed. An effective plan for review of proposed changes and distribution of updated documents, both internal and external to Brooktree suppliers, ensures that improvements in product and process requirements are implemented efficiently.

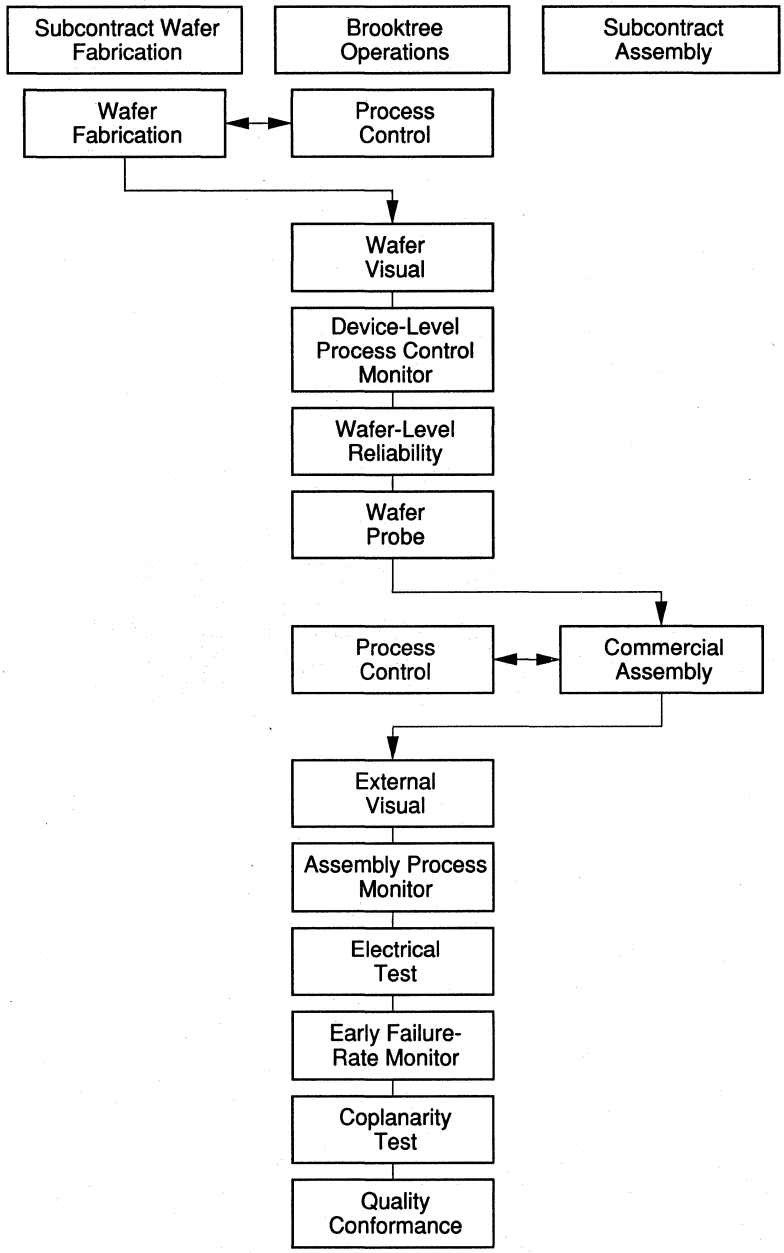


Figure 1. Standard Product Manufacturing Flow.

Reliability Assurance Program

Reliability is quality over time, a measurement of the time the product continues to perform to original specifications. This must be guaranteed by using a worst case design methodology, precisely controlled wafer processing and device assembly, and testing to the highest quality standards.

Product reliability is verified through accelerated testing and physical and environmental stress testing. The stress tests performed for product qualification are listed in Tables 1–3. These tests are repeated at regular intervals to verify continuing process and product integrity. Strict engineering-change-control procedures are used to ensure a controlled process.

The basic method used to estimate product life is accelerated environmental testing. These tests expose the product to stresses greater than those expected in actual use. The number of device failures that occur can be related to the magnitude of the stress applied. The common practice is to express the results in failures in 10^9 hours, or FITs. (One FIT is equal to one failure per billion device hours of operation. It can also be expressed in the common notation of 0.0001-percent failures per 1000 hours).

Figure 2 is an idealized graph of device failure rate versus time, often called the bathtub curve. Three distinct regions are of importance. Region A is characterized by high failure rates that show up in early use and then decrease with time. This area of early life failures must be minimized and, if possible, eliminated prior to shipment of the product to the final customer. Brooktree has an aggressive program for continuously assessing this Early Failure Rate (EFR) for its products. When the EFR does not meet customer requirements, screening techniques, primarily high-temperature burn-in, are used to eliminate the early failures before shipment.

Region B is characterized by a constant failure rate and indicates the normal operating region that will ensure maximum useful service and reliability. This region is thoroughly evaluated for all wafer-fabrication processes employed at Brooktree, as well as for all new designs. This is a key measurement of product reliability. Strict requirements are placed on all processes and products to meet aggressive reliability goals.

Region C indicates the wearout region where device failure rate increases. The wearout region is seldom reached in well-designed semiconductor integrated circuits under normal operating conditions. Results of accelerated life testing are extrapolated to estimates of in-service reliability through use of the Arrhenius model.

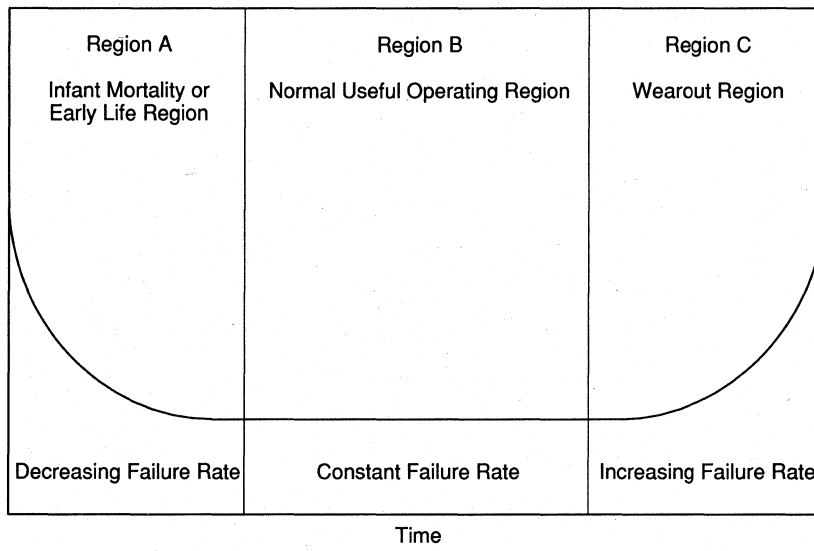


Figure 2. Device Failure Rate Versus Time.

Description	Methods and Conditions (Note 1)	Sample Size (Note 2)	Notes
High-Temperature Operating Life Electrical (25° C)	2000 Hours, TA = 125° C (Note 3)	280	Read Points at T0, 8, 16, 24, 32, 40, 48, 96, 500, 1000, 1500, and 2000 Hours
High-Temperature Storage Electrical (25° C)	2000 Hours, TA = 150° C	55	Read Points at T0, 1000 and 2000 Hours
Temperature Cycle Electrical (25° C)	See Figure 3 for Surface-Mount Package Precondition Flow Method 1010, Condition C, –65° C to +150° C, 500 Cycles Method 1010, Condition A, 0° C to + 125° C, 3000 Cycles	153	Read Points a T0, 500 Cycles for Method C, 1500 and 3000 Cycles for Method A
Thermal Shock Electrical (25° C)	Method 1011, Condition B, –55° C to +125° C, 200 Cycles	116	Read Points a t T0 and 200 Cycles
Steady-State Temperature/Humidity Electrical (25° C)	See Figure 3 for Surface-Mount Package Precondition Flow. 85° C/85% RH, 168 Hours, Unbiased 85° C/85% RH, 1500 Hours, Biased	195	Plastic Packages Only Read Points at T0, 500, 1000, and 1500 Hours
Pressure Cooker Electrical (25° C)	121° C, 2.0 ATM, 96 Hours, 100% RH	77	Plastic Packages Only Read Points at T0 and 96 Hours
Destructive Physical Analysis	High-Magnification Visual, Device Cross-section, Design Rule Verification, Step Coverage, Passivation Integrity	1 Wafer	
Device-Level Testing	On Wafer: SWEAT, TDDB, QBD,HCI, Mobile Ion Oven EM Testing: EM1: J_S = 10x, T_S = 250°C EM2: J_S = 20x, T_S = 250°C EM3: J_S = 20x, T_S = 200°C Flatlines, Contacts/Vias	5/Wafer 20	All Wafer Tested 20 Samples per Structure, per Test Condition

Note 1: Test methods reference MIL-STD-883C.
Note 2: Samples are selected from three wafer lots (processed with a minimum of 1 week separating each wafer lot).
Note 3: Power supplies shall be set at 0.5 V less than absolute maximum specified supply voltage; TA shall be reduced, if necessary, to guarantee TJ to be less than 175° C for ceramic packages, or less than 150° C for plastic packages.

Table 1. Wafer Fabrication Process Qualification Tests.

Description	Methods and Conditions (Note 1)	Sample Size (Note 2)	Notes
Plating Thickness	Per Applicable Package Specification	4	
Solderability	Method 2003	4	
Resistance to Solvents	Method 2015	4	
Lead Integrity Fine Leak Gross Leak	Method 2004, Condition B Method 1014, Condition A or B Method 1014, Condition C	22	Fine/Gross Leak Performed for CERDIP Packages Only
Temperature Cycle Fine/Gross Leak Electrical (25° C)	Method 1010, Condition C, –65° C to +150° C, 500 Cycles Method 1010, Condition A, 0° C to +125° C, 3000 Cycles	153	Fine/Gross Leak Performed at T0 and 3500 Total Cycles Electrical Read Points at T0, 500 Cycles (Condition C), 1500 Cycles and 3000 Cycles (Condition A)
Thermal Shock Fine/Gross Leak Electrical (25° C)	Method 1011, Condition B, –55° C to +125° C, 200 Cycles	116	Read Points at T0 and 200 Cycles (Electrical, Fine and Gross Leak)
Mechanical Shock Vibration Constant Accelleration Fine/Gross Leak Electrical (25° C)	Method 2002, Condition B Method 2007, Condition A Method 2001, Condition E, Y1 Axis Only	77	Read Points at T0 and End of Sequence (Electrical, Fine and Gross Leak)
Salt Atmosphere Fine/Gross Leak	Method 1009	34	Read Points at T0 and End of Test
Resistance to Solder Heat Fine/Gross Leak Electrical (25° C)	15-Second Dip to Within 1/8" of Body Solder at 260° C	22	Read Points at T0 and End of Test (Electrical, Fine and Gross Leak)
Destructive Physical Analysis	X-Ray, Internal Visual, Bond Strength, Die Shear/Pull, Cross-section	6	2 Samples From Each of 3 Assembly Lots

Note 1: Test methods reference MIL-STD-883C.
Note 2: Samples to be selected from three assembly lots (processed with a minimum of 1 week between each lot).

Table 2. Hermetic Assembly Process Qualifications Tests.

Description	Methods and Conditions (Note 1)	Sample Size (Note 2)	Notes
Plating Thickness	Per Applicable Package Specification	4	
Solderability	Method 2003	4	
Resistance to Solvents	Method 2015	4	
Temperature Cycle Electrical (25° C)	See Figure 3 for Surface-Mount Package Preconditioning Flow. Method 1010, Condition C, –65° C to +150° C, 500 Cycles Method 1010, Condition A, 0° C to +125° C, 3000 Cycles	153	Read Points at T_0, 500 Cycles (Condition C), 1500 Cycles and 3000 Cycles (Condition A)
Thermal Shock Electrical (25° C)	Method 1011, Condition B, –55° C to 125° C, 200 Cycles	116	Read Points at T_0 and 200 Cycles
Steady-State Temperature/Humidity Electrical (25° C)	See Figure 3 for Surface-Mount Package Precondition Flow 85° C/85% RH, 168 Hours, Unbiased 85° C/85% RH, 1500 Hours, Biased	195	Plastic Packages Only Read Points at T_0; 500, 1000, and 1500 Hours
Pressure Cooker (Electrical 25° C)	See Figure 3 for Surface-Mount Package Precondition Flow 121° C, 2.0 ATM, 96 Hours, 100% RH	77	Read Points at T_0 and 96 Hours
Salt Atmosphere	Method 1009	34	
High-Temperature Operating Life Electrical (25° C)	T_A = 125° C (T_J < 150° C), 1500 Hours	150	Read Points at T_0; 8, 16, 24, 32, 40, 48, 96, 168, 500, 1000, and 1500 Hours
Resistance to Solder Heat Electrical (25° C)	15-Second Dip to Within 1/8" of Body in Solder at 260° C	22	Read Points at T_0 and End of Test
Destructive Physical Analysis	X-Ray, Internal Visual, Bond Strength, Die Shear/Pull, Cross-section	6	3 Samples From Each of 3 Assembly Lots

Note 1: Test methods reference MIL-STD-883C.
Note 2: Samples to be selected from three assembly lots (processed with a minimum of 1 week between each lot).

Table 3. Plastic Package Assembly Process Qualifications Tests.

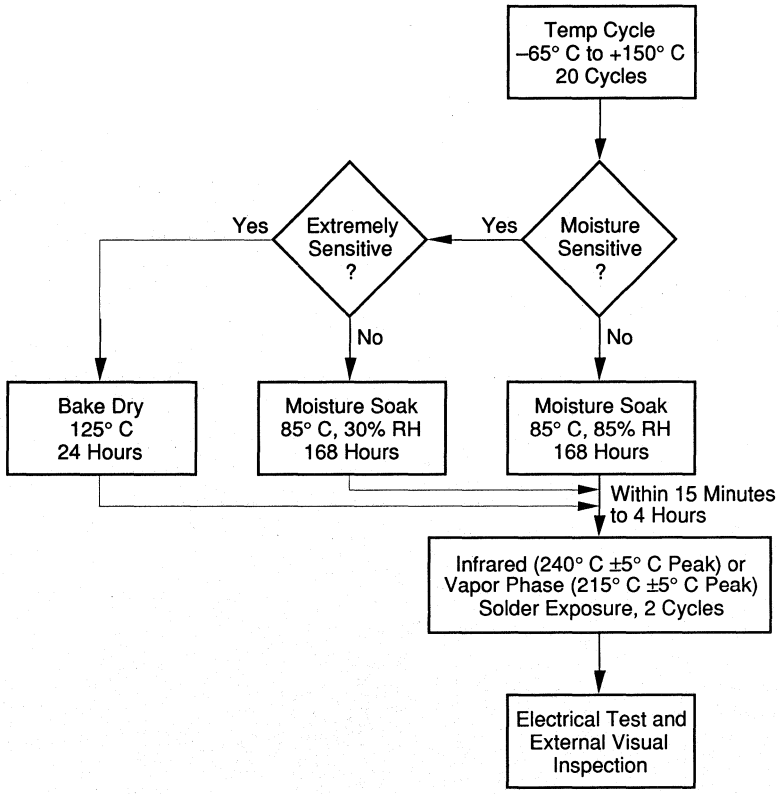


Figure 3. Preconditioning Flow for Plastic Surface Mount Packages.

Product Development

Quality and reliability planning begins with the product development cycle. It is vital that every possible effort to improve the quality and reliability of the product is made during the development cycle. Therefore, specific design goals must be defined with proven reliable materials and manufacturing methods, and controlled production processes must be implemented with accurate testing and monitoring.

Design

Brooktree's Development Engineering Department has established a comprehensive design methodology developed to produce reliable devices. Product definition begins with experienced system designers who can accurately specify the electrical interface and functional boundary requirements. This ensures that all new devices will have specifications and worst case operating and environmental conditions identified before design begins.

Design engineers use schematic capture and simulation software to verify the operation of the design over temperature, power supply, and processing variations. The Device Engineering group constantly monitors wafer fabrication processes and extracts critical parametric information from them to keep the models used to simulate designs as accurate and current as possible. Designers are required to adhere to documented design rules, which are written to ensure device reliability. These rules address the allowable amount of Electrostatic Discharge (ESD), latchup protection, and current-density limitations to prevent phenomena such as electromigration. Each circuit design is computer simulated with worst case methodology.

Conformance to strict layout rules immunizes products to process variation while maximizing reliability. An extensive set of checks is provided by several state-of-the-art Computer Aided Design (CAD)

tools that ensures the design layout is correct and the wafers can be consistently processed with confidence in yield and reliability.

Wafer/Device-Level Testing

Each wafer lot received at Brooktree is sample tested for key device parameters. This Process Control Monitor (PCM) is intended to identify any statistical variations in the process that may affect product quality, reliability, or performance. Any significant variation identified is thoroughly analyzed, and corrective action is generated if necessary. Also, each wafer lot is sample tested using Wafer-Level Reliability (WLR) techniques. WLR attempts similar stress testing to traditional reliability tests described above, but in a much shorter time. While direct correlation with the above-described tests is not always possible, this technique is used to detect statistical variation in the wafer fabrication process. Any observed variation is thoroughly analyzed to ensure no impact on actual device reliability.

In addition to the electrical testing, a physical sample is taken from each wafer lot and archived at Brooktree. On a monthly basis a sample is pulled from each wafer fabrication process technology, and complete destructive physical analysis is performed to monitor critical dimensions and general workmanship. The results are analyzed similarly to the electrical test results to detect statistical variation in the process. As described above, any significant deviation is thoroughly analyzed to determine its potential effect on product quality, reliability, and performance.

Wafer Probe

Wafer probe is performed at Brooktree to ensure the tightest quality and reliability controls early in the life of the product. Statistically calculated limits are put on the results of wafer probe to look for statistical deviation in device performance caused by variations in the wafer fabrication process. Any out-of-control situations are thoroughly analyzed to determine root cause, and corrective action is taken if necessary. Wafer-probe test conditions and limits are guard banded to ensure early removal of defective devices. Correlation between the final test programs and probe programs is an effective gate to prevent a nonfunctional device from entering the assembly operation. Rejected dice are marked with an ink dot to allow easy identification after the individual die is scribed from the wafer.

Device Assembly

The Quality Assurance Department monitors the performance of various processing steps by requiring mandatory sampling of each lot moving through critical assembly operations. Brooktree has instituted several sampling points in the assembly area, including: wafer inspection, raw-material inspection, second-optical (high-magnification) die inspection, die attach control, wire-bond control, third-optical (low-magnification) inspection, hermeticity testing, QA final inspection, and QA shipping audit. Daily monitors, and audits of equipment and operators ensure that the final product meets all predefined quality criteria.

Device Packaging

Brooktree packaging uses standard, semicustom, and custom packages. Package designs, outlines, and footprints comply, wherever possible, with industry standards developed by organizations such as JEDEC and EIAJ. Since product performance is affected by package design, custom packages are constructed when necessary to preserve the reliability and performance of the enclosed device.

Final Testing

Final electrical testing is performed at Brooktree with state-of-the-art test equipment and techniques. Test parameters and test conditions are such that proper performance is guaranteed to datasheet requirements and to tighter standards where possible. Test limits are guard banded to compensate for tester inaccuracy, thereby minimizing measurement-correlation errors between the factory and customer. Digital test vectors are also verified by fault grading to ensure that the vector set is sufficiently extensive to identify any potential fault conditions. To comply with quality-conformance requirements, Quality Engineering verifies proper processing, proper electrical performance over specified operating temperatures and voltage ranges, and visual criteria.

Qualification

All Brooktree products are labeled with the classification of the products' reliability for consumer use. Each product datasheet contains a designation as to the product development and specification parameters status. The product datasheet designations are "Advanced," "Preliminary," and "Final." When the device has been fully characterized to all the specifications and datasheet parameters, and has completed the environmental tests outlined in Tables 1–3, it is labeled production worthy, and the datasheet status becomes "final."

Failure Analysis

Even under the strictest of standards, failures do occur. To control this situation and to learn from it, the Failure Analysis group identifies reliability problems and analyzes the root causes of failures with inhouse stress tests as well as customer field returns. The data from these analyses is used to generate corrective action, a key to the continuous improvement cycle. Brooktree provides customers with specific feedback so that the customer is ensured that appropriate action has been taken.

Terms and Definitions

Activation Energy—The excess energy over the ground state, which must be acquired by an atomic or molecular system in order for a specific process to occur.

Arrhenius Model (Acceleration Factor)—The Arrhenius model defines a relationship between the failure rate and time that is commonly used to correlate accelerated life environmental testing to useful lifetime. The equation is used to calculate failure rates based on lower junction temperatures and normal operating environmental conditions.

The acceleration factor is the reaction rate of a process at one temperature compared with the reaction rate of the same process at another temperature. The acceleration factor equation determines the multiplication factor of time that the change in temperature caused on the reaction process.

The following is the Arrhenius model for acceleration factors:

$$AF = e[Ea/K(1/T1 - 1/T2)]$$

Where:

AF = Acceleration Factor
e = Natural logarithm base of 2.71828
Ea = The activation energy for semiconductor material
K = Boltzmann's constant (8.626×10^{-5} eV/Kelvin)
T1 = Lower temperature in degrees Kelvin
T2 = Higher temperature in degrees Kelvin

Example: The AF for a temperature change from 85°C to 125°C is 25.9 with an assumed activation energy (Ea) of 1.0eV. This factor is the time multiplication factor: 1 hour at 125°C is equivalent to 25.9 hours (over 1 day) at 85°C.

Bias—The electrical connection to the device pins that allows specified signals, loading, and power supply voltage to be applied. Bias is often referred to as "electrical bias."

Biased Humidity—An environmental test in which the subject device is exposed to high humidity and temperature conditions (85-percent relative humidity and 85°C) while the device is under an electrical bias. This procedure is designed to measure the device's susceptibility to electrolysis or electrolytic corrosion. The acceleration factor for a humidity change from 50 percent to 85 percent has been standardized as approximately 10. When bias humidity and temperature results are analyzed, the acceleration factors of humidity and temperature are estimated separately.

Burn-in—A thermal and electrical stress test designed to eliminate early failures. The early device failures (infant mortality) are detected and removed, thus enhancing reliability.

Environmental Tests—Several tests that determine the long-term stability and reliability of products. The product is exposed to various conditions and extremes of temperature, humidity, pressure, or mechanical stress that stimulate potential faults to appear. Detection of device failures is thus accelerated.

Failure in Time (FIT)—A standard reliability unit that measures the device failure rate as a function of device hours. One FIT is equal to one device failure per billion device hours of operation (1 FIT = 0.0001% failures/1000 hours).

Terms and Definitions *(continued)*

Infant Mortality—Initial failures of devices that occur in early life operation. This is the region of the device failure-rate curve (Figure 2) where the device failure rate decreases with time. Product reliability is enhanced when environmental screening (burn-in) eliminates these early failures.

Pressure Cooker—A test that subjects the device to an atmosphere of high-temperature moisture under a pressure of approximately 2 atmospheres. This test exposes susceptibility to galvanic corrosion caused by chemical instability of the encapsulating materials.

Qualification—Qualification includes the test procedures as defined by the Quality Assurance and Reliability Engineering Department that a product must survive before being considered a reliable manufacturing product.

Quality[1]—During use the extent to which a product successfully serves the purpose of the user is called "fitness for use." This concept of fitness for use is popularly called "quality." Several parameters can be used to characterize product quality. Quality of design is a technical measure of the product's level or degree of excellence in meeting the intended needs of the user. Three activities that compose the quality of design are: quality of market research, quality of concept, and quality of specification. Quality of conformance is the extent to which the product conforms to design. Conformance can be measured by testing to the product specification. Conformance may also be termed "quality of manufacturing" or "quality of production." The quality of products over time is characterized by the time-oriented factors, such as availability, reliability, and maintainability.

Quality Assurance (QA)—The activity of providing, to all concerned, the evidence needed to establish confidence and assurance that all the activities that affect product quality are being performed adequately.

Reliability—Quality of products over time. It can be determined by the product's ability to perform without failure. The classic definition is: "the probability of a product performing without failure a specified function under given conditions for a specified period of time."

Sampling—An inspection method to estimate, with statistical confidence, the quality of a product or process by careful examination of a small number of devices from a larger population. A sampling plan is used to set the sample size, based on the desired level of confidence and the desired level of quality.

Screening—The process of subjecting all products to nondestructive stresses to accelerate and identify early failures.

Stress—An extreme environmental, electrical, or physical condition applied to a device to evaluate the device performance or to accelerate reaction rates.

Temperature Cycling—A test that determines the thermal expansion compatibility of materials used in device packaging. The test exposes the device to temperature extremes in a series of cycles, alternating from the high extreme to the low extreme, repetitively. The device is under no electrical bias.

Thermal Shock—A temperature cycling test in which the temperature transitions are very rapid, less than 10 seconds. The device is immersed in suitable liquid baths, each having extreme high or low temperatures to expose such failures as device cracking and package leaking.

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1. Quality Control Handbook, Third Edition.
McGraw Hill 1974, Juran, Joseph M., Frank M. Gryna Jr., and R.S. Bingham Jr.

Section 3

IMAGING PRODUCTS

Brooktree®

Contents

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt218

20 MSPS
Monolithic CMOS
8-bit Flash
Video A/D Converter

3

Distinguishing Features

- 20 MSPS Operation
- Bt208 Pin Compatilibity
- No Video Amplifier Requirement
- ±1/4 LSB Typical DL Error
- ±1/2 LSB Typical IL Error
- External Zero and Clamp Control
- Overflow Output
- On-Chip Reference
- Output Enable Control
- TTL Compatiblility
- +5 V CMOS Monolithic Construction
- 24-pin 0.3" DIP or 28-pin PLCC Package
- Typical Power Dissipation: 500 mW

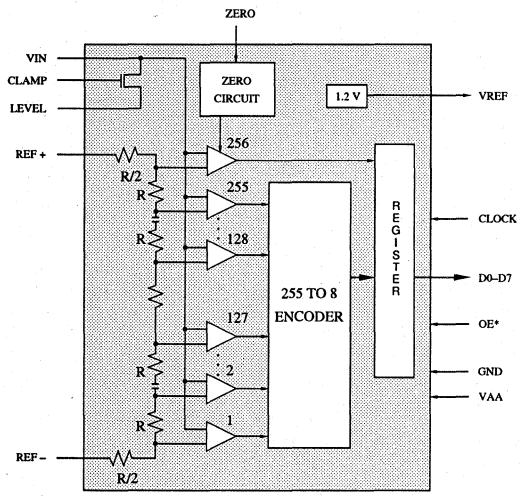
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt252, Bt254
- Bt261

Functional Block Diagram



Product Description

The Bt218 is an 8-bit flash A/D converter designed specifically for video digitizing applications. A flash converter topology is used with 256 high-speed comparators in parallel to digitize the analog input signal.

Flexible input ranges enable NTSC and CCIR video signals to be digitized without requiring a video amplifier.

The TTL-compatible output data and OVERFLOW are registered synchronously with the clock signal. The OE* three-states the D0–D7 outputs asynchronously to CLOCK.

The ZERO input is used to zero the comparators, while CLAMP allows DC restoration of an AC-coupled video signal (by forcing the VIN input to the voltage on the LEVEL pin).

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L218001 Rev. C

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt218 contains 256 high-speed comparators, a 255-to-8 encoder, an output register, and a resistor divider network. Of the 256 comparators, 255 are used to digitize the analog signal; the additional comparator is used to generate the OVERFLOW bit.

General Operation

The Bt218 converts an analog signal in the range of REF– ≤ Vin ≤ REF+, generating a binary number from $00 to $FF, and an OVERFLOW output (see Table 1).

The values of REF+ and REF– are flexible to enable various video signals to be digitized without requiring a video amplifier. Refer to the Recommended Operating Conditions and Application Information sections for suggested configurations.

Figure 1 shows the input/output timing of the Bt218. The sample is taken following the falling edge of CLOCK. The binary data and OVERFLOW are registered and output onto the D0–D7 and OVERFLOW pins on the second rising edge of CLOCK.

Comparator Zeroing

The ZERO input is used to periodically zero the comparators. The comparators have an initial threshold mismatch caused by manufacturing tolerances. Zeroing charges capacitors in the comparators that offset this threshold mismatch. But because capacitors discharge, the comparators must be periodically zeroed.

While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, D0–D7 and OVERFLOW are not updated. They retain the data loaded before the ZERO cycle.

Input Signal Clamping

CLAMP and LEVEL are used only in applications where the video signal is AC coupled to VIN. While CLAMP is a logical one, the VIN input is forced to the voltage level of the LEVEL pin to DC restore the video signal.

In applications where the video signal is DC coupled to VIN, the LEVEL pin should float or be connected to VIN, or CLAMP should always be a logical zero (on the 28-pin PLCC package only) .

Vin (V) (Note 1)	Overflow	D0–D7	OE*
> 0.998	1	$FF	0
0.996	0	$FF	0
0.992	0	$FE	0
:	:	:	:
0.500	0	$81	0
0.496	0	$80	0
0.492	0	$7F	0
:	:	:	:
0.004	0	$01	0
< 0.002	0	$00	0
		3-state	1

Note 1: With REF+ = 1.000 V and REF– = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV.

Table 1. Output Coding Example.

Timing Waveforms

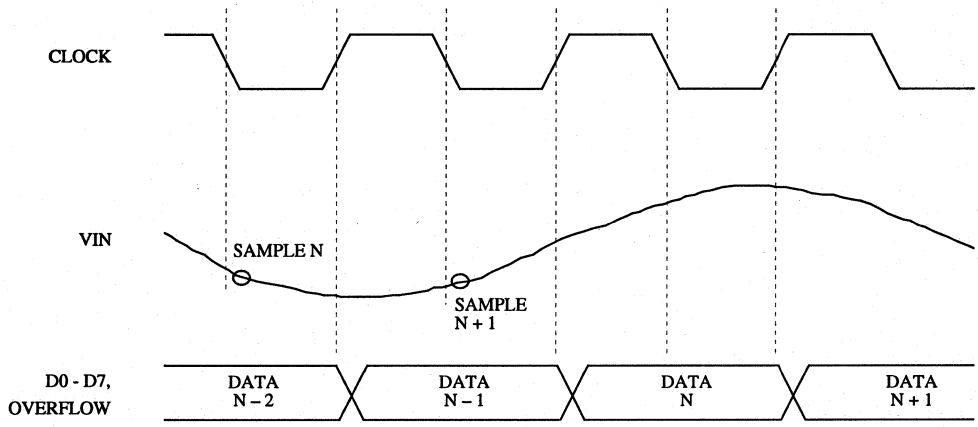


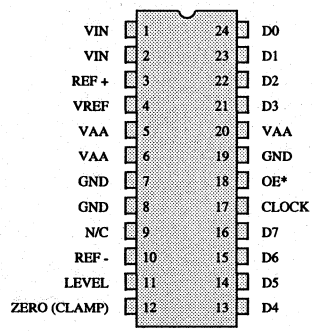
Figure 1. General Operation.

Pin Descriptions

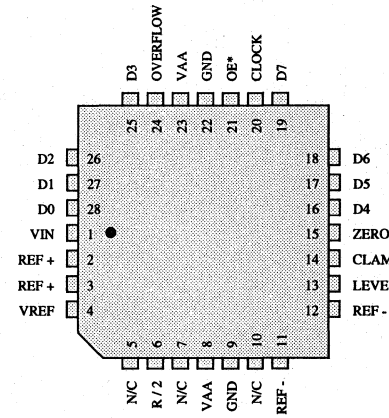
Pin Name	Description
D0–D7	Data outputs (TTL compatible). D0 is the least significant data bit. These outputs are latched and output following the second rising edge of CLOCK. Coding is binary. For optimum performance, D0–D7 should have minimal loading. If a large capacitive load is being driven, an external buffer is recommended.
OE*	Output enable control input (TTL compatible). Negating OE* three-states D0–D7 asynchronously. The OVERFLOW output is not affected by the state of OE*.
OVERFLOW	Overflow output (TTL compatible). OVERFLOW is latched and output following the second rising edge of CLOCK. OE* does not affect the OVERFLOW output signal. OVERFLOW is not available on the DIP package.
CLOCK	Clock input (TTL compatible). It is recommended that this pin be driven by a dedicated TTL buffer to minimize sampling jitter.
REF+	Top of ladder voltage reference (voltage input). REF+ sets the VIN voltage level that corresponds to $FF on the D0–D7 outputs. All REF+ pins must be connected together as close to the device as possible. For noise immunity reasons, a decoupling capacitor is not recommended on REF+.
REF–	Bottom of ladder voltage reference (voltage input). Typically, this input is connected to GND. REF– sets the VIN voltage level that corresponds to $00 on the D0–D7 outputs. All REF– pins must be connected together as close to the device as possible.
R/2	Midtap of reference ladder (voltage output). R/2 is not available on the DIP package. If not used, this pin should remain floating. If used, it should be buffered by a voltage follower. For noise immunity reasons, a decoupling capacitor is not recommended on R/2.
VIN	Analog signal inputs (voltage input). All VIN pins must be connected together as close to the device as possible.
ZERO/CLAMP	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators are zeroed and D0–D7 output data is held to the current state. ZERO is latched on the rising edge of CLOCK. On the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, zeroing and clamping occur simultaneously. Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN inputs are forced to the voltage level on the LEVEL pin to perform DC restoration of an AC-coupled video signal. CLAMP is asynchronous to clock. On the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, ZERO and CLAMP are asserted simultaneously.

Pin Descriptions *(continued)*

Pin Name	Description
LEVEL	Level control input (voltage input). This input is used to specify what voltage level is to be used for clamping while CLAMP is a logical one. LEVEL is used only to DC restore AC coupled video signals. In applications where the video signal is DC coupled to VIN, the LEVEL pin should float or be connected to VIN.
VREF	Voltage reference output pin. This pin provides a 1.2 V (typical) output. A decoupling capacitor is not recommended on VREF.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup.



24-pin 0.3" DIP Package



28-pin Plastic J-Lead (PLCC) Package

Note: N/C pins are reserved and must remain floating.

PC Board Layout Considerations

PC Board Considerations

For optimum performance, before PCB layout is begun, the CMOS digitizer layout examples in the Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements, Application Notes AN-13, 14, and 15, respectively, should be studied. These application notes can be found in the Brooktree Applications Handbook.

The layout should be optimized for lowest noise on the Bt218 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

A single ground plane covering both digital and analog logic should be used.

Power Planes

The Bt218 and any associated analog circuitry should have their own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt218.

The regular PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt218 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that the regular PCB power plane does not overlay the analog power plane.

Supply Decoupling

The bypass capacitors should be installed with the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

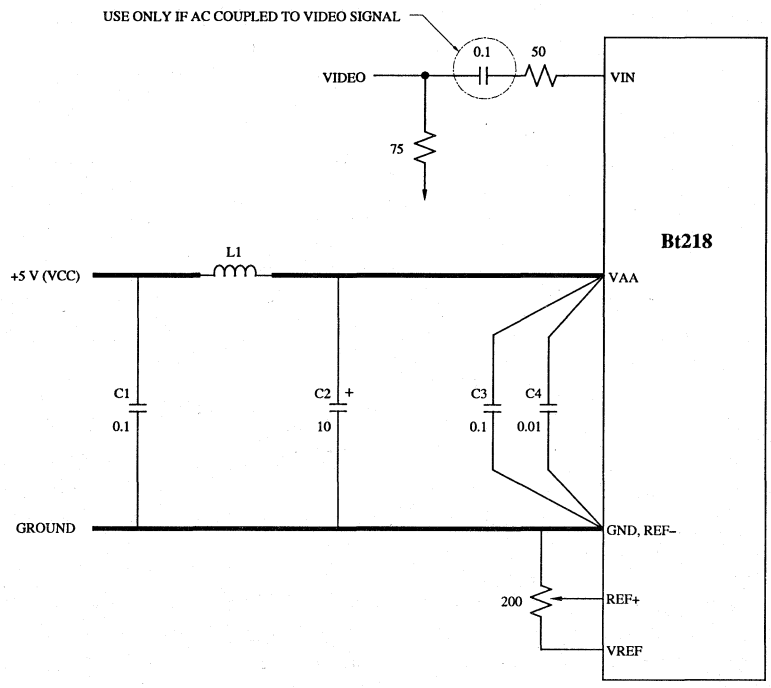
Each group of VAA and GND pins should have a 0.1 µF ceramic chip capacitor located as close as possible to the device pins. The capacitors should be connected directly to the VAA and GND pins with short, wide traces.

Signal Interconnect

The digital signals of the Bt218 must be isolated as much as possible from the analog inputs and other analog circuitry to prevent crosstalk. Also, these digital signals should not overlay the analog power plane.

Termination resistors for the digital signals should be connected to the digital PCB power and ground planes.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1, C3	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2	10 µF capacitor	Mallory CSR13G106KM
C4	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt218.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

Using the Internal Reference

The Bt218 has a 1.2 V on-chip reference available (VREF). VREF may be divided down and used to drive the REF+ input, as shown in Figure 2. The 200 Ω potentiometer serves three purposes: to allow adjustment for different video signal levels, to allow for video level tolerances, and to adjust for tolerance of the internal reference.

VREF should supply at least 6 mA of current to maintain voltage stability over temperature. Thus, VREF should drive a resistive load between 90 and 240 Ω.

Using An External Reference

Figure 3 illustrates the use of a 1.2 V LM385 and a TLC272 to generate a 0–1.2 V reference for applications that require a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that can operate from a single +5 V supply.

To prevent ringing in the TLC272 from clock kickback, a 100 Ω resistor is recommended, as shown in Figure 3. If an op-amp is chosen that has a better transient response than the TLC272, the resistor may not be needed. This circuit may also be used to drive the Ref– if a value other than ground is desired. Because single-supply op-amps are limited, Ref– may not be set below ~300 mV. To drive Ref– to true 0 V in the op-amp configuration, a dual supply must be used. *Extreme care must be used in power sequencing to ensure all positive supplies (op-amp and A/D) power on before the negative supply. This will prevent latchup of the A/D.*

AC-Coupled vs. DC-Coupled Input

The Bt218 may be either AC or DC coupled to the video signal, as shown in Figure 2. The 75 Ω resistor to ground provides the typical 75 Ω termination required by video signals. The 50 Ω resistor provides isolation from any clock kickback noise on VIN and prevents it from being coupled onto the video signal. If the Bt218 is DC coupled to the video signal, the 0.1 µF capacitor is not used and CLAMP should be grounded.

Zeroing

Unlike many CMOS A/D converters requiring the comparators to be zeroed every clock cycle, the comparators in the Bt218 are designed to be only periodically zeroed. It is convenient to assert ZERO during each horizontal blanking interval.

Before the Bt218 is used after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent because of the number of horizontal scan lines that will have occurred before the Bt218 was used.

While the recommended zeroing interval is maintained, the Bt218 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

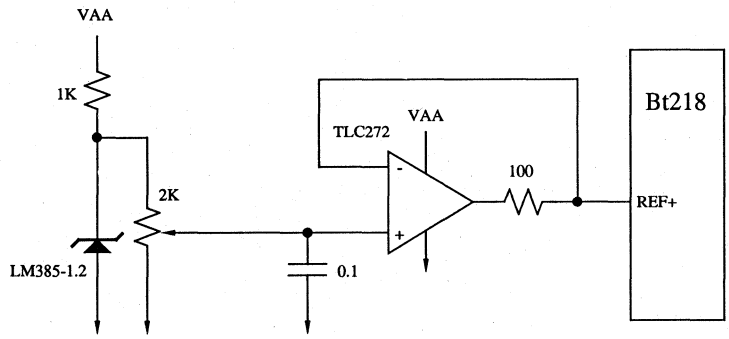


Figure 3. Using an External Reference.

Application Information *(continued)*

Input Ranges

Table 2 lists some common video signal amplitudes. If a signal may possibly exceed 1.2 V, it should be attenuated (with a resistor divider network) so as not to exceed the 1.2 V input range.

When a full-scale range less than 0.7 V is used to digitize, the Bt218's integral linearity errors are constant in terms of voltage, regardless of the value of the reference voltage. Lower reference voltages will, therefore, produce larger integral linearity errors in terms of LSBs.

For example, with a reference difference of 0.6 V, 0.6 V video signals may be digitized. However, the Integral Linearity (IL) error will increase to about ±1.8 LSB, and the SNR will be about 40 db. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB, and the SNR will be about 39 db.

Output Noise

Although the Bt218 does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth (see the AC Characteristics section). Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 641746–2 for the PLCC package.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors can cause a power supply time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 2. Video Signal Tolerances.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.00	5.5	V
Voltage References					
Top	REF+	0.7	1	2.0	V
Bottom	REF–	0	0	1.3	V
Difference (Top–Bottom)		0.7	1	1.2	V
Input Amplitude Range		0.7	1	1.2	V
Analog Input Range			REF– to REF+		V
LEVEL Input Voltage		GND–0.5	REF–	REF+	V
Time between Zeroing Intervals			60	150	µs
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Input Voltage		GND–0.5		VAA + 0.5	V
R/2 Output Current				25	µA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error (Note 1)	IL		±0.5	±1	LSB
Differential Linearity Error	DL		±0.25	±1	LSB
Output Noise (Note 2)			±1		LSB
Coding					
No Missing Codes			guaranteed		Binary
VIN Analog Inputs (Note 3)					
CLAMP = 0					
Input Current (Leakage)	IB			1	µA
Input Capacitance	CAIN		35		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
REF+ Reference Input					
Input Impedance	RREF+		500		Ω
Digital Inputs					
Input High Voltage	VIH	2.0			V
Input Low Voltage	VIL			0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = –50 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Three-State Current	IOZ			10	µA
Output Capacitance	COUT			10	pF
Internal Voltage Reference	VREF		1.2		V
Regulation (at 6 mA)			5		mV
Output Current	IREF			15	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, and LEVEL = float. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Using best-fit linearity (offset independent).
Note 2: Clock duty cycle adjusted for minimum output noise for a DC input. For a DC input, output noise may increase if clock duty cycle is not adjusted.
Note 3: LEVEL = GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			20	MHz
Clock Cycle Time (Figure 4)	1	50			ns
Clock Low Time	2	20			ns
Clock High Time	3	20			ns
Data Output Delay Time (Figure 5)	4			40	ns
Data Output Hold Time	5	9			ns
OE* Asserted to D0–D7 Valid	6			25	ns
OE* Negated to D0–D7 3-Stated	7			25	ns
ZERO Setup Time	8	0			ns
ZERO Hold Time	9	20			ns
ZERO, CLAMP High Time (Note 1)		1			Clock
Aperture Delay	10		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW			Fs/2	MHz
Transient Response (Note 2)			1		Clock
Overload Recovery (Note 3)			1		Clock
Zero Recovery Time (Note 4)			1		Clock
RMS Signal-to-Noise Ratio	SNR				
Fin = 4.20 MHz, Fs = 12.27 MHz			44		db
Fin = 4.20 MHz, Fs = 13.50 MHz			44		db
Fin = 4.20 MHz, Fs = 14.32 MHz			44		db
Fin = 5.75 MHz, Fs = 13.50 MHz			43		db
Fin = 5.75 MHz, Fs = 14.75 MHz			43		db
Fin = 5.75 MHz, Fs = 17.72 MHz			43		db
Fin = 10.0 MHz, Fs = 20.00 MHz			39		db
RMS Signal & Distortion-to-Noise Ratio	SINAD				
Fin = 4.20 MHz, Fs = 12.27 MHz			42		db
Fin = 4.20 MHz, Fs = 13.50 MHz			42		db
Fin = 4.20 MHz, Fs = 14.32 MHz			42		db
Fin = 5.75 MHz, Fs = 13.50 MHz			41		db
Fin = 5.75 MHz, Fs = 14.75 MHz			41		db
Fin = 5.75 MHz, Fs = 17.72 MHz			41		db
Fin = 10.0 MHz, Fs = 20.00 MHz			37		db
Total Harmonic Distortion	THD				
Fin = 4.20 MHz, Fs = 12.27 MHz			47		db
Fin = 4.20 MHz, Fs = 13.50 MHz			47		db
Fin = 4.20 MHz, Fs = 14.32 MHz			47		db
Fin = 5.75 MHz, Fs = 13.50 MHz			47		db
Fin = 5.75 MHz, Fs = 14.75 MHz			47		db
Fin = 5.75 MHz, Fs = 17.72 MHz			47		db
Fin = 10.0 MHz, Fs = 20.00 MHz			44		db

See test conditions and notes on next page.

AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Spurious Free Dynamic Range	SFDR				
Fin = 4.20 MHz, Fs = 12.27 MHz			50		db
Fin = 4.20 MHz, Fs = 13.50 MHz			50		db
Fin = 4.20 MHz, Fs = 14.32 MHz			50		db
Fin = 5.75 MHz, Fs = 13.50 MHz			50		db
Fin = 5.75 MHz, Fs = 14.75 MHz			50		db
Fin = 5.75 MHz, Fs = 17.72 MHz			50		db
Fin = 10.0 MHz, Fs = 20.00 MHz			47		db
Differential Gain Error (Note 5)	DG		2		%
Differential Phase Error (Note 5)	DP		1		Degree
Supply Current (Note 6) (Excluding REF+)	IAA		100	160	mA
Pipeline Delay (Note 7)		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF–≤ Vin≤ REF+ and, LEVEL = float. TTL input values are 0–3 V with input rise/fall times≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 1.5 V for digital inputs and outputs. D0–D7 and OVERFLOW output load ≤ 40 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, and Fs = 14.32 MHz, T_{CASE} = Ambient.
IAA (max) at VAA = 5.5 V, Fin = 10 MHz, and Fs = 20 MHz, T_{CASE} = 0° C.
Note 7: Pipeline delay is defined as discrete clock period delays in addition to the half-cycle analog sampling delay.

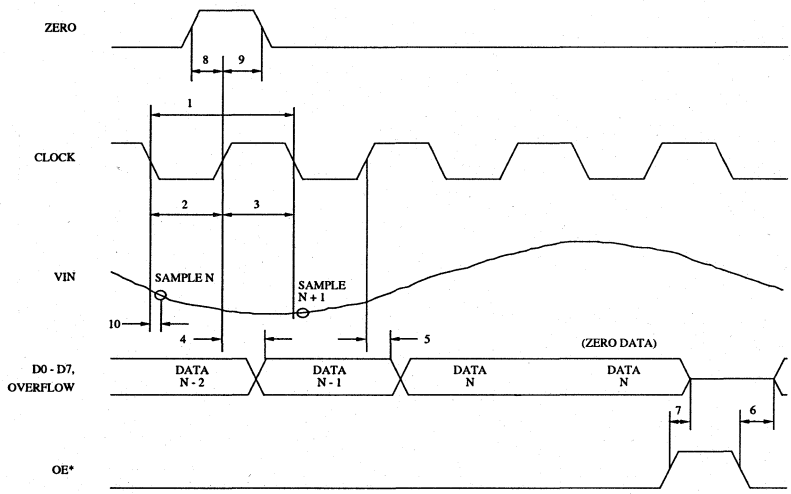
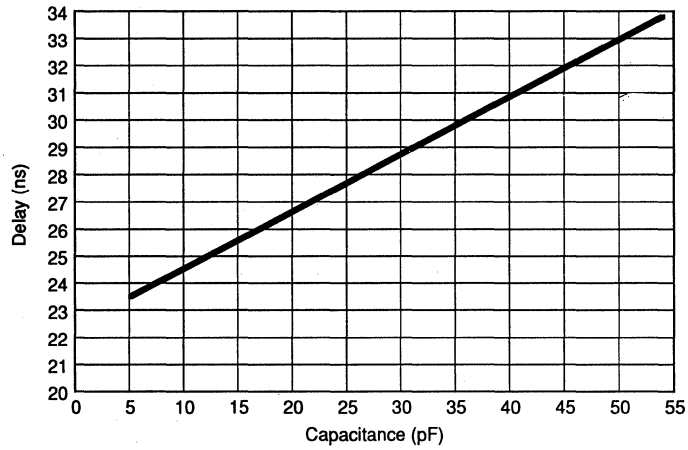


Figure 4. Input/Output Timing.

AC Characteristics *(continued)*



Note: Nominal device at ambient, timing reference points = 1.4 V

Figure 5. Bt218KPJ Output Delay vs. Capacitive Loading.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt218KP20	20 MHz	24-pin 0.3" Plastic DIP	0° to +70° C
Bt218KPJ20	20 MHz	28-pin Plastic J-Lead	0° to +70° C
Bt218EVM	Evaluation Board for the Bt218KP. Includes a Bt218KP30.		

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt252

3

20 MSPS Monolithic CMOS Single-Channel 8-bit Image Digitizer

Distinguishing Features

- 20 MSPS Operation
- Bt251 Pin Compatiblility
- Four Software-Selectable Analog Inputs
- DC- or AC-Coupled Video Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- 8-bit Flash A/D Converter
- R/2 Reference Ladder Tap
- 256 x 8 Lookup Table
- Standard MPU Interface
- TTL Compatiblility
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package

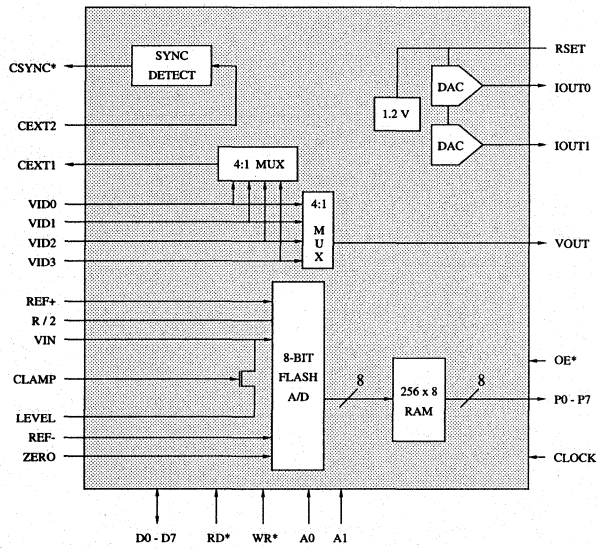
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt254
- Bt261

Functional Block Diagram



Product Description

The Bt252 Image Digitizer is designed to digitize standard video signals (NTSC or CCIR). The architecture of the Bt252 enables the addition of external circuitry for such functions as filtering and gain along the signal path. A standard MPU interface is provided to access various control functions.

Four analog inputs are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking independent of the video input being digitized. A TTL-compatible composite sync signal is output to interface to the genlock circuitry.

The output of the 8-bit A/D converter addresses a 256 x 8 lookup table RAM, enabling real-time image manipulation prior to data storage. This includes, for example, thresholding, contrast enhancement, video reversal, and implementation of a nonlinear A/D. The digitized data outputs may be three-stated asynchronously to clock with the OE* control.

Optional MPU-controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF– inputs to the A/D. The ZERO input is used to zero the comparators, while CLAMP allows DC restoration of an AC-coupled video signal (by forcing the VIN input to the voltage on the LEVEL pin).

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L252001 Rev. C

Brooktree®

General Operation

The Bt252 uses an 8-bit flash A/D converter to digitize the video signal. The A/D digitizes analog signals in the range of REF– ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF–) to $FF (Vin ≥ REF+).

The values of REF+ and REF– are flexible to enable various video signals to be digitized without requiring a video amplifier. Refer to the Recommended Operating Conditions and Application Information sections for suggested configurations.

Figure 1 shows the input/output timing of the Bt252. The sample is taken following the falling edge of CLOCK. Two positive CLOCK edges later, after the lookup table is addressed, the registered data is output on P0–P7.

MPU Interface

As shown in the functional block diagram, the Bt252 supports a standard MPU interface (D0–D7, RD*, WR*, A0, and A1). MPU operations are asynchronous to the clock.

An internal 8-bit address register, in conjunction with A0 and A1, is used to specify which control register or RAM location the MPU is accessing, as shown in Table 1. All registers and RAM locations may be written to or read by the MPU at any time; however, while digitizing a video signal, the MPU should not access the RAM, as this will corrupt the digitized data.

When the MPU accesses the RAM, the address register increments after each MPU access (read or write cycle). After writing to RAM location $FF, the address register resets to $00.

When the address register or control registers are accessed, the address register does not increment after an MPU read or write cycle. Data written to reserved locations is ignored; data read from reserved locations returns invalid data. ADDR0 corresponds to D0 and is the least significant bit.

Analog Input Selection

The Bt252 supports four analog input sources, VID0–VID3. The MPU specifies which of these is to be digitized through the command register.

The selected video signal is output onto VOUT. VOUT may be connected directly to VIN if no filtering or gain of the video signal is required.

If only the luminance information of a video signal containing color subcarrier information is being digitized, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low-pass filter, notch filter, or comb filter may be used to remove the chroma information.

Sync information (if present) will still be present on VOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

The 75 Ω resistors to ground (Figure 2) provide the typical 75 Ω termination required by video signals.

A1	A0	ADDR7–ADDR0	Addressed by MPU
0	0	xxxx xxxx	address register
0	1	0000 0000	RAM location $00
0	1	0000 0001	RAM location $01
:	:	:	:
0	1	1111 1111	RAM location $FF
1	0	xxxx xx00	command register
1	0	xxxx xx01	IOUT0 data register
1	0	xxxx xx10	IOUT1 data register
1	0	xxxx xx11	reserved
1	1	xxxx xxxx	reserved

Table 1. Address Register Operation.

Circuit Description *(continued)*

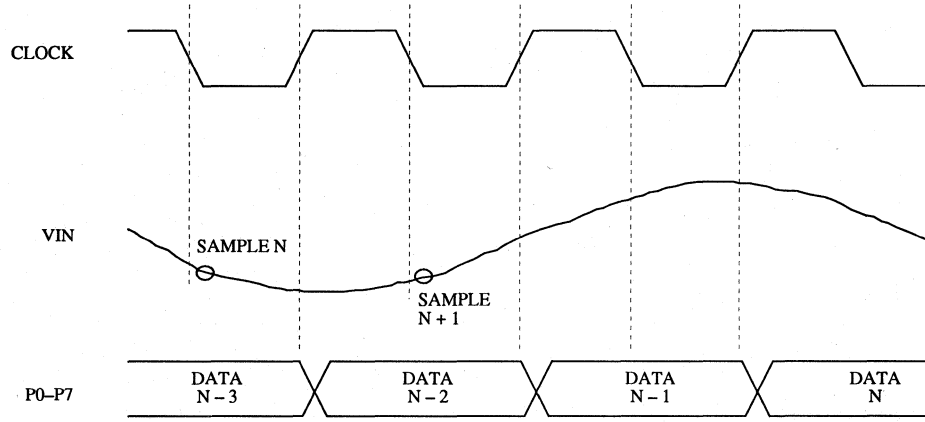
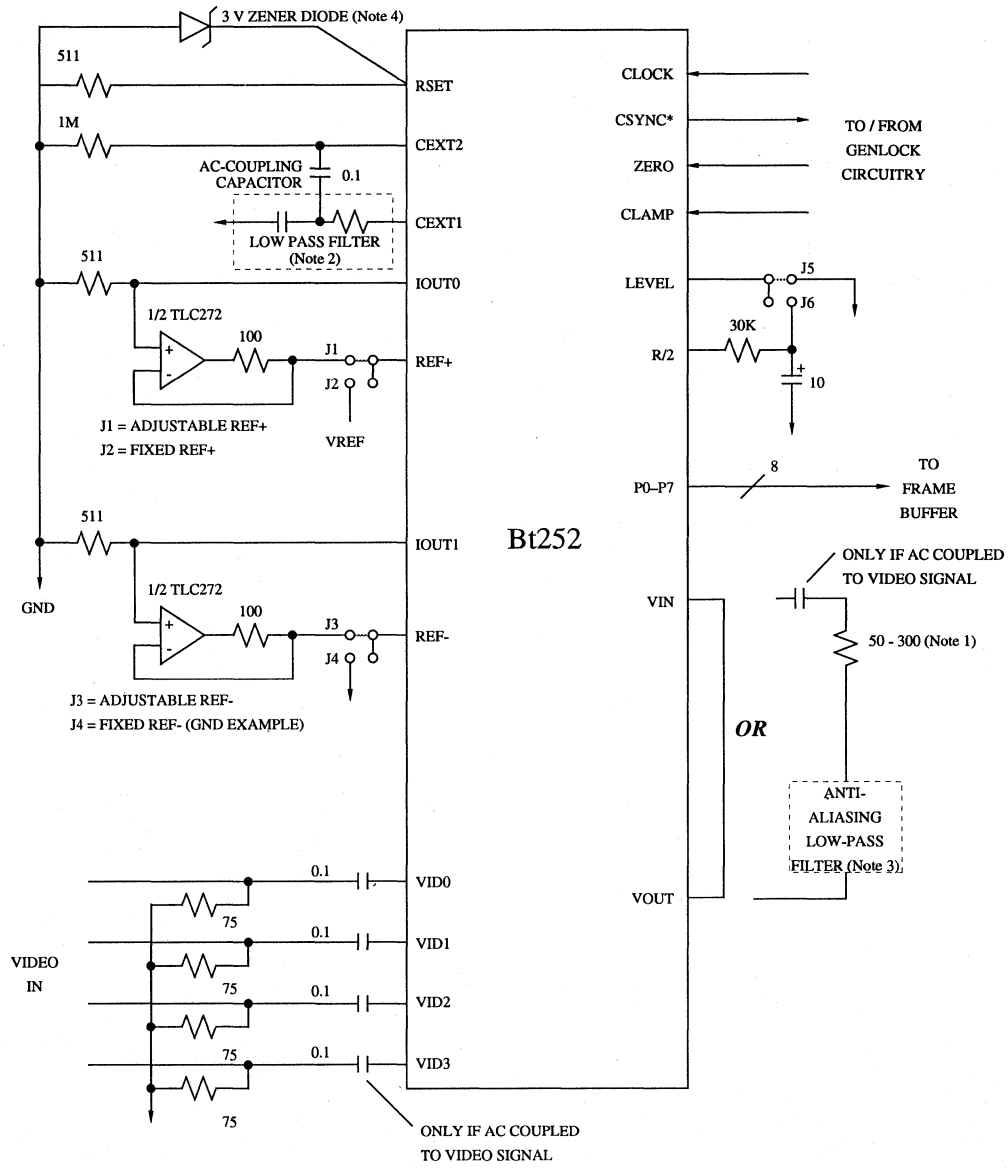


Figure 1. General Operation.

Circuit Description *(continued)*



J5 = DC restore to GND
J6 = Color Difference DC restore

Note 1: Needed only if active filter is used. Adjust for minimum clock kickback.
Note 2: Filter to remove colorburst, preventing false sync detection.
Note 3: If the antialiasing filter if located here, only the filter is required. Otherwise, each video input must have an antialiasing filter.
Note 4: See RSET pin name definition for discussion of zenor diode.

Figure 2. Typical Bt252 External Circuitry.

Circuit Description *(continued)*

A/D Reference Generation

As shown in Figure 2, the Bt252 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, REF+ is connected to a 0.7–1.2 V reference (VREF) and REF– is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7–1.2 V and no adjustment of gain or offset.

If jumpers J1 and J3 are selected, the MPU-adjustable outputs IOUT0 and IOUT1 may be used for gain and offset of the video signal. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations, such as contrast enhancement or level adjustments, may be implemented. The TLC272 dual CMOS op-amps can be used for single +5 V operation. However, because single-supply op-amps are limited, REF– may not be able to achieve a voltage below 300 mV with a single 5 V supply. Using an External Reference in the Application Information section contains further information.

IOUT0 and IOUT1 are current outputs (0–2.5 mA) generated by two 6-bit D/A converters. A 511 Ω RSET resistor generates a 2.35 mA full-scale output current. The 511 Ω resistors to GND generate a 0–1.2 V level that drives the REF+ and REF– inputs through voltage followers.

The DAC outputs should not drive the top of the reference ladder directly. The reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of REF– is desired, the DAC output must drive REF– with a voltage follower.

A/D Zeroing

The ZERO input is used to zero the comparators and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the P0–P7 outputs are not updated. They retain the data loaded before the ZERO cycle.

AC-coupled Video and A/D Input Clamping

When video is AC coupled, capacitors are required on all video inputs. A capacitor may also be needed between VIN and VOUT, depending on the filtering implementation (see to Figure 2). The video mux will DC adjust the input video to prevent channel- to-channel crosstalk through the video mux.

If VIN is AC coupled to the video signal, the CLAMP and LEVEL controls may be used to DC restore the video signal. While CLAMP is a logical one, the video signal is clamped to the voltage level present on the LEVEL pin. CLAMP should be asserted during static intervals and at least 200 ns before or after a video transition. During clamping, the resistances of the mux and clamp are approximately 100 and 50 Ω, respectively. Incorporation of the 0.1 µF clamp capacitor yields an RC time constant of 15 µs. On power-up or after a transition of the video input, approximately three to five time constants will be required to completely DC restore the video signal. When the clamp is asserted on the back porch for 0.5–1.5 µs, several lines of video will be required to properly DC restore the signal. For example, clamping the video signal for 1 µs during each line of video will require 75 lines of video for proper DC restoration. This is assuming five time constants are needed.

When RGB or luminance video signals are DC restored, LEVEL is typically connected to the same potential as REF–.

When color difference video signals are DC restored, LEVEL is typically at the midpoint between REF+ and REF–. The Bt252 provides an R/2 reference ladder tap that may be used to generate the proper DC voltage (jumper J6 in Figure 2). The R/2 tap should drive a high-impedance load while capturing an image to maintain optimum linearity of the A/D converter.

DC-Coupled Video

When video is DC coupled, the video levels must be within the digitization range of the A/D. To avoid channel-to-channel crosstalk through the video mux, nonsynchronized video sources must not drop more than 100 mV below ground. For example, if the black/blank level of the DC-coupled

video is at ground, an external sync clipper must be used to guarantee that the sync tip does not drop below –100 mV. If VIN is DC coupled to the video signal, the level should float or the clamp should be a logical zero.

Antialiasing Filtering and VIN Input Considerations

The input video must be passed through an antialiasing filter to meet Nyquist criteria. The filter can be placed between VIN and VOUT to filter all video sources or on each video input before the MUX.

The 50–300 Ω resistor, shown in Figure 2 after the low-pass filter, is required only if an active low-pass filter is used. The resistor provides isolation from any clock kickback noise on VIN, preventing it from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on VIN. If no filter or a passive low-pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

If DC restoration and low-pass filtering between VOUT and VIN are implemented, a 0.1 µF capacitor is required after the low-pass filter. If no filter between VOUT and VIN is used, the capacitor is not required, as the DC restoration can still be implemented with the 0.1 µF capacitors on the VIDx inputs.

Multiplexer Considerations

DC level maintenance within the rated compliance range is necessary to obtain the best linearity and crosstalk performance.

Lookup Table RAM

A 256 x 8 lookup table RAM is provided on-chip to implement simple imaging operations such as gamma manipulation, contrast enhancement, data inversion, or a nonlinear transfer function of the A/D converter. Data from the A/D is used to address the RAM; the addressed data is output onto P0–P7.

The RAM may be effectively bypassed by loading each location with its corresponding address. As the lookup table RAM is not dual ported, MPU accesses have priority over digitized data passing through the RAM. During MPU accesses to the RAM, P0–P7 are undefined.

Sync Detect Circuitry

The Bt252 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. CSYNC* is output asynchronously to the clock, and there are no pipeline delays. (The output delay from VIN to CSYNC* is approximately 25 ns.)

The MPU specifies from which analog input to detect sync (negative sync polarity). The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC couples the video signal to the sync detection circuit. The sync tip is internally clamped to a DC level. The sync detect value determines the threshold above this DC level where the Bt252 detects sync. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero. A low-pass filter removes the colorburst signal.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 2).

If the sync detection circuit is not used, CEXT2 should be connected to GND or VAA (CEXT1 may float), or an unused (grounded) video input should be selected for the sync detector.

External Sync Detection

CEXT1 may be connected to an external sync detector circuit. In this case, CEXT2 should be connected directly to GND or VAA, and the CSYNC* output should be left floating.

The sync analog multiplexer may still be used to select from which video source to detect sync information. As the multiplexer switches analog video signals, the selected video source will be output onto CEXT1.

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. D0 is the least significant bit.

D7, D6	Digitize select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify which analog input is to be digitized. The selected signal is output onto VOUT.
D5, D4	Sync detect select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify from which analog input sync information is to be detected. The selected signal is output onto CEXT1.
D3, D2	Sync detect level select (00) 50 mV (01) 75 mV (10) 100 mV (11) 125 mV	These bits specify the amount above the sync tip to slice CEXT2 for sync detection.
D1, D0	Reserved (logical zero)	The MPU must write a logical zero to these bits to ensure proper operation.

IOUT Data Registers

These two 6-bit registers specify the output current on the IOUT0 and IOUT1 outputs, from 0 mA ($00) to full scale ($FC). The 6 MSBs of data are used to drive the DACs. D0 and D1 (the 2 LSBs) must be programmed to be a logical zero.

These registers may be written to or read by the MPU at any time and are not initialized. D0 is the least significant bit.

Pin Descriptions

Pin Name	Description
General Reference Functions	
RSET	Full-scale adjust control. An external 511 Ω resistor must be connected between this pin and GND. RSET is used to provide reference information to the internal D/A converters (See Figure 2). At cold operating temperatures, the RSET pin might power up with a voltage of 4 V. (This is a threshold below the supply voltage.) A minimum of perturbation on the RSET pin or an increase in temperature will change states on the bandgap reference to the normal 1.2 V operating point. RSET can be forced to a power up with the correct voltage by adding a 3 V zener diode in parallel with the RSET resistor. If the Bt252 powers up in the wrong state, the zener will activate and toggle the bandgap reference voltage to the correct state. The alternative is to leave the part configured without the diode. This might necessitate resequencing the power for initial operation of the boards at cold temperatures.
IOUT0, IOUT1	Current outputs. The amount of output current is specified by the IOUT data registers. External 511 Ω resistors are typically connected between each pin and GND (See Figure 2). The relationship between full-scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (Ω)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC couple the video signal to the sync detect circuitry. A 1M Ω resistor must also be connected between CEXT2 and GND (See Figure 2).
A/D Functions	
REF+	Top of resistor ladder (voltage input). REF+ sets the VIN voltage level that corresponds to $FF from the A/D converter. For noise immunity reasons, a decoupling capacitor is *not* recommended on REF+.
REF–	Bottom of resistor ladder (voltage input). REF– sets the VIN voltage level that generates $00 from the A/D converter.
R/2	Reference ladder midpoint tap. If not used, this pin should remain floating. For noise immunity reasons, a decoupling capacitor is *not* recommended on R/2. External loading should be less than 1 µA to obtain the best linearity.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D are zeroed. ZERO is latched on the rising edge of CLOCK. During zeroing cycles, P0–P7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN input is forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. In applications where VIN is DC coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.
LEVEL	Level control input (voltage input). This input is used to specify the voltage level for DC restoration while CLAMP is a logical one. In applications where VIN is DC coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.
VIN	A/D converter input. The analog signal to be digitized should be connected to this analog input pin. It may be either DC or AC coupled to the video signal being digitized.
VID0–VID3, VOUT	Analog inputs and analog output. VID0–VID3 are connected to the video signals to be digitized. The signal selected to be digitized is output onto VOUT. Unused inputs should be connected to GND.

Pin Descriptions *(continued)*

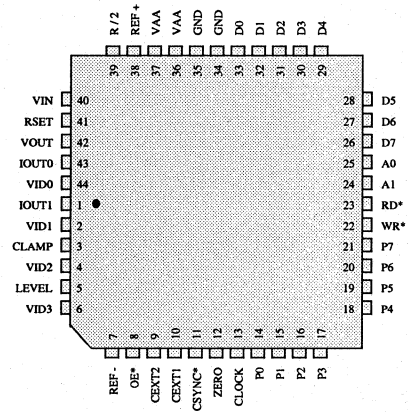
Pin Name	Description
CLOCK	Clock input (TTL compatible). CLOCK should be driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected on the VID0–VID3 input specified by the command register, converted to TTL levels, and output onto this pin. CSYNC* is output asynchronously to the clock, and there are no pipeline delays.

Digital Control Functions

P0–P7	Digitized video data outputs (TTL compatible). Digitized video data is output onto these pins following the second rising edge of CLOCK. P0 is the least significant bit. P0–P7are three-stated if OE* is a logical one.
OE*	Output enable control input (TTL compatible). A logical one three-states the P0–P7 outputs asynchronously to CLOCK.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device through D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0, A1	Address control inputs (TTL compatible). A0 and A1 are used to specify the operation the MPU is performing, as indicated in Table 1. They are latched on the falling edge of either RD* or WR*.

Power and Ground

VAA	+5 V power. All VAA pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup. A 0.1µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible. (Ceramic chip capacitors are preferred.)
GND	Ground. All GND pins must be connected together on the same PCB plane to prevent latchup.



PC Board Layout Considerations

PC Board Considerations

For optimum performance, before PCB layout is begun, the CMOS digitizer layout examples in the Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements, Application Notes AN-13, 14, and 15, respectively, should be studied. These Application Notes can be found in the Brooktree Applications Handbook.

The layout should be optimized for lowest noise on the Bt252 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

A single common ground plane covering both analog and digital logic should be used.

Power Planes

The Bt252 and any associated analog circuitry should have their own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt252.

The regular PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt252 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that the regular PCB power plane does not overlay the analog power plane.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

The VAA and GND pins should have a 0.1 µF ceramic chip capacitor located as close as possible to the device pins. The capacitors should be connected directly to the VAA and GND pins with short, wide traces.

Digital Signal Interconnect

The digital signals of the Bt252 must be isolated as much as possible from the analog signals and other analog circuitry to prevent crosstalk. Also, the digital signals should not overlay the analog power plane.

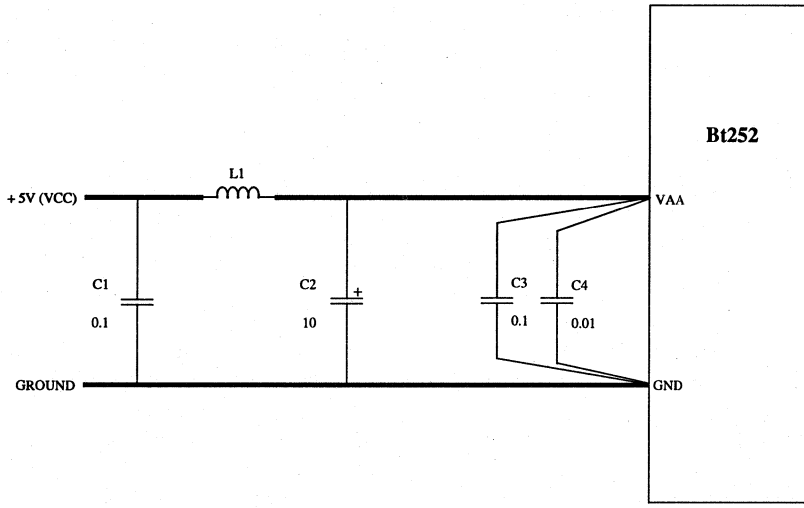
Termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs. Microstrip techniques should be employed to keep video trace impedance at 75 Ω, to match standard coax impedance.

Also, high-speed TTL signals should not be routed close to the analog signals, to minimize noise coupling.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1, C3	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2	10 µF tantalum capacitor	Mallory CSR13G106KM
C4	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt252.

Figure 3. Typical Power Supply Connection Diagram and Parts List.

Application Information

Zeroing

As the comparators on the Bt252 must be periodically zeroed, it is convenient to assert ZERO during each horizontal blanking interval.

Before the Bt252 is used after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications, this will be transparent because of the number of horizontal scan lines that will have occurred before the Bt252 was used.

While the recommended zeroing interval is maintained, the Bt252 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

Increasing the Resolution of DACs

With a 511 Ω resistor connected between each DAC output (IOUT0 and IOUT1) and GND, the resolution of the ladder adjustment is 19 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 4 shows a circuit that allows adjustment of the REF+ inputs from 0.714–1 V with 4.5 mV resolution. With the DAC data = $00, 0.714 V is output; if the DAC data = $FC, 1 V is output.

As the typical maximum DAC output current is 2.35 mA (RSET = 511 Ω), if a 0.286 V adjustable range is desired, R1 || R2 must equal 121 Ω. The minimum output voltage desired determines the ratio of R1 and R2 as follows:

$$Vmin = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF–) may be adjusted from 0–0.286 V with 1.125 mV resolution with a 121 Ω resistor to ground rather than a 511 Ω resistor. While the minimum range is 0 V, the resistor to ground may be used to adjust the total range and, thus, the resolution.

Using An External Reference

Figure 5 illustrates the use of a 1.2 V LM385 and a TLC272 to generate a 0–1.2 V reference for applications that require a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that can of operate from a single +5 V supply.

To prevent ringing in the TLC272 from clock kickback, a 100 Ω resistor as shown in Figure 5 is recommended. If an op-amp is chosen that has a better transient response than the TLC272, the resistor may not be needed. This circuit may also be used to drive the REF– if a value other than ground is desired. Because single-supply op-amps are limited, REF– may not be set below ~300 mV. To drive REF– to true 0 V in the op-amp configuration, a dual supply must be used. *Extreme care must be used in power sequencing to ensure all positive supplies (op-amp and A/D) power on before the negative supply. This will prevent latchup of the A/D.*

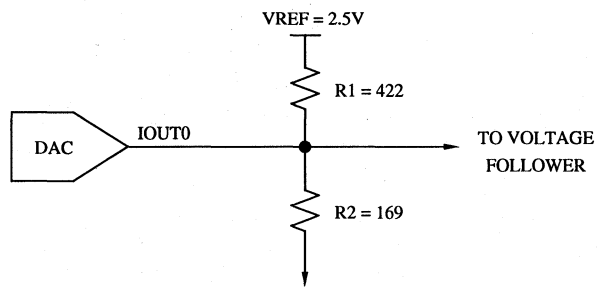


Figure 4. Increasing DAC Output Resolution.

Application Information *(continued)*

Input Ranges

Table 2 lists some common video signal amplitudes. Signals that exceed 1.2 V should be attenuated with a resistor divider network.

When a signal is digitized with a full-scale range less than 0.7 V, the Bt252's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will, therefore, produce larger integral linearity errors in terms of LSBs.

For example, when the reference difference is set to 0.6 V, 0.6 V video signals may be digitized. However, the integral linearity error will increase to about ±1.8 LSB, and the SNR will be about 40 db. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB and an SNR of about 39 db.

Output Noise

Although the A/D exhibits some output noise for a DC input, the output noise remains relatively constant for any input bandwidth (see AC Characteristics section). Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 641747-2.

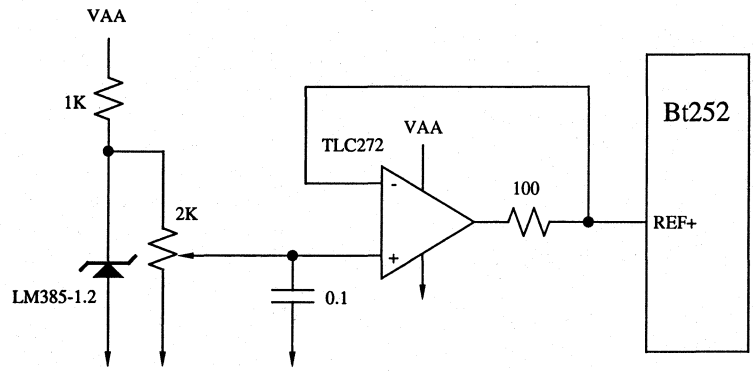


Figure 5. Using an External Reference.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 2. Video Signal Tolerances.

Application Information *(continued)*

Bt252 with Minimal External Circuitry

Figure 6 shows the Bt252 in an application requiring that 1 V video signals be digitized.

In this instance, the IOUT0 output is driving the top of the reference ladder (REF+) directly, without being buffered by a voltage follower. The internal 500 Ω resistor between IOUT0 and GND develops a 0–1.2 V reference voltage for the A/D (based on the contents of the IOUT0 data register). IOUT1 and REF– are connected to GND.

Although this implementation is not as temperature stable as that shown in Figure 2 (because of some variation in the reference ladder resistance over temperature), it will probably suffice for most applications.

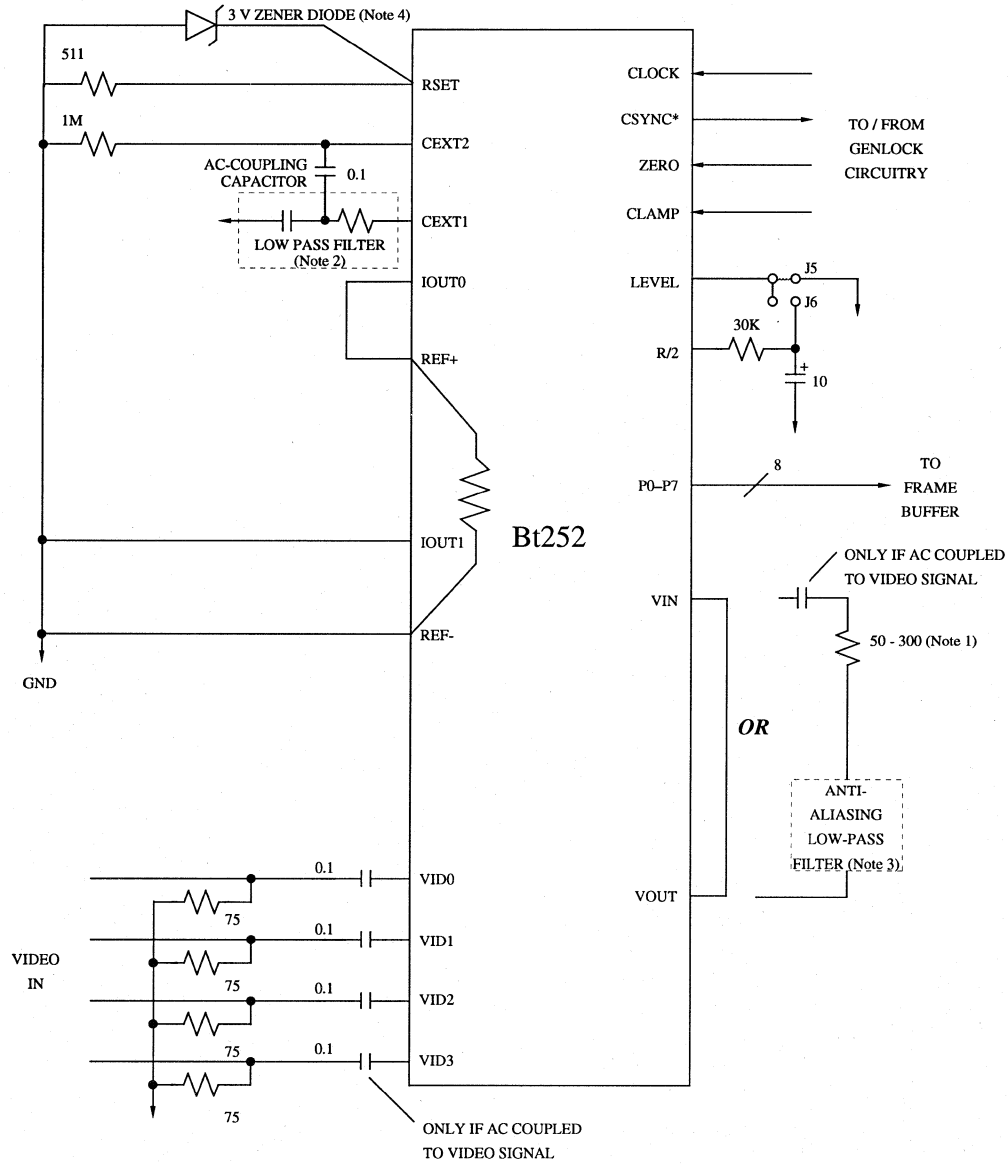
ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors can cause a power supply time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information *(continued)*



J5 = DC restore to GND
J6 = Color Difference DC restore

Note 1: Needed only if active filter is used. Adjust for minimum clock kickback.
Note 2: Filter to remove colorburst, preventing false sync detection.
Note 3: If the antialiasing filter if located here, only the filter is required. Otherwise, each video input must have an antialiasing filter.
Note 4: See RSET pin name definition for discussion of zener diode.

Figure 6. Bt252 Minimal External Circuitry.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Voltage References					
Top	REF+	0.7	1	2.0	V
Bottom	REF–	0	0	1.3	V
Difference (Top–Bottom)		0.7	1	1.2	V
VID0–VID3 Amplitude Range		0.5		VAA–0.5	V
Multiplexer Compliance (DC)		–0.2		+2.2	V
VIN Input Amplitude Range		0.7	1	1.2	V
VIN Input Range			REF– to REF+		V
CEXT AC Amplitude		0.2 Vp-p		2.0 Vp-p	V
LEVEL Input Voltage	TA	GND–0.5	REF–	REF+	V
Zeroing Interval			60	150	µs
Ambient Operating Temperature		0		+ 70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Input Voltage	VIN, VIDx	GND–0.5		VAA + 0.5	V
R/2 Output Current				25	µA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (Note 1)	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
A/D Coding (Table 3)					
No Missing Codes			guaranteed		Binary
VIN Analog Input (Note 2)					
CLAMP = 0					
Input Current Leakage	IB			1	µA
Input Capacitance	CAIN		35		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
VID0–VID3 Analog Inputs (Note 3)					
Input Impedance to VOUT					
Input Selected			100		Ω
Input Deselected (Leakage)			10		MΩ
Input Capacitance			15		pF
REF+ Reference Input					
Input Impedance			500		Ω
Digital Inputs					
Input High Voltage	VIH	2.0			V
Input Low Voltage	VIL			0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
P0–P7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
CSYNC* Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Output Capacitance	COUT		10		

See test conditions and notes on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0 and IOUT1 Outputs					
DAC Output Current		0		2.5	mA
DAC Output Impedance			100		kΩ
DAC Output Capacitance			20		pF
DAC Accuracy					
Differential Linearity Error	DL			±1	LSB
Integral Linearity Error	IL			±1	LSB
Monotonicity			guaranteed		

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Best-fit linearity. Linearity is tested with RAM transparent (data = address).
Note 2: LEVEL = GND.
Note 3: VOUT connected to GND.

Vin (V) (Note 1)	P0–P7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

Note 1: With REF+ = 1.000 V and REF– = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV. RAM transparent (data = address).

Table 3. A/D Coding.

AC Characteristics

Parameter	Symbo	Min	Typ	Max	Units
Conversion Rate	Fs			20	MHz
Multiplexer Switching Time	Tmux		100		ns
Clock Cycle Time	1	50			ns
Clock Low Time	2	20			ns
Clock High Time	3	20			ns
P0–P7 Output Delay Time (Figure 7)	4			40	ns
P0–P7 Output Hold Time	5	9			ns
OE* Asserted to P0–P7 Valid	6			20	ns
OE* Negated to P0–P7 3-Stated	7			20	ns
ZERO Setup Time	8	0			ns
ZERO Hold Time	9	20			ns
ZERO, CLAMP High Time (Note 1)		1			Clock
Aperture Delay	10		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW			Fs/2	MHz
Transient Response (Note 2)			1		Clock
Overload Recovery (Note 3)			1		Clock
Zero Recovery Time (Note 4)			1		Clock
RMS Signal-to-Noise Ratio	SNR				
Fin = 4.20 MHz, Fs = 12.27 MHz			44		db
Fin = 4.20 MHz, Fs = 13.50 MHz			44		db
Fin = 4.20 MHz, Fs = 14.32 MHz			44		db
Fin = 5.75 MHz, Fs = 13.50 MHz			43		db
Fin = 5.75 MHz, Fs = 14.75 MHz			43		db
Fin = 5.75 MHz, Fs = 17.72 MHz			43		db
Fin = 10.0 MHz, Fs = 20.00 MHz			39		db
RMS Signal & Distortion-to-Noise Ratio	SINAD				
Fin = 4.20 MHz, Fs = 12.27 MHz			42		db
Fin = 4.20 MHz, Fs = 13.50 MHz			42		db
Fin = 4.20 MHz, Fs = 14.32 MHz			42		db
Fin = 5.75 MHz, Fs = 13.50 MHz			41		db
Fin = 5.75 MHz, Fs = 14.75 MHz			41		db
Fin = 5.75 MHz, Fs = 17.72 MHz			41		db
Fin = 10.0 MHz, Fs = 20.00 MHz			37		db
Total Harmonic Distortion	THD				
Fin = 4.20 MHz, Fs = 12.27 MHz			47		db
Fin = 4.20 MHz, Fs = 13.50 MHz			47		db
Fin = 4.20 MHz, Fs = 14.32 MHz			47		db
Fin = 5.75 MHz, Fs = 13.50 MHz			47		db
Fin = 5.75 MHz, Fs = 14.75 MHz			47		db
Fin = 5.75 MHz, Fs = 17.72 MHz			47		db
Fin = 10.0 MHz, Fs = 20.00 MHz			44		db

See test conditions and notes on next page.

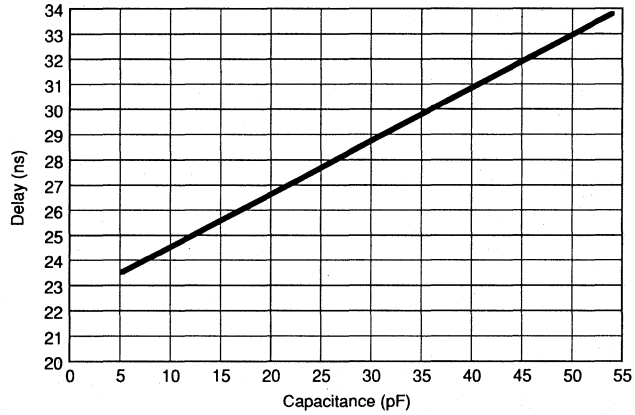
AC Characteristics *(continued)*

Parameter	Symbo	Min	Typ	Max	Units
Spurious Free Dynamic Range	SFDR				
Fin = 4.20 MHz, Fs = 12.27 MHz			50		db
Fin = 4.20 MHz, Fs = 13.50 MHz			50		db
Fin = 4.20 MHz, Fs = 14.32 MHz			50		db
Fin = 5.75 MHz, Fs = 13.50 MHz			50		db
Fin = 5.75 MHz, Fs = 14.75 MHz			50		db
Fin = 5.75 MHz, Fs = 17.72 MHz			50		db
Fin = 10.0 MHz, Fs = 20.00 MHz			47		db
Analog Multiplexer Crosstalk					
All-Hostile Crosstalk (Figure 8)			–50		db
Single-Channel Crosstalk (Figure 9)			–50		db
Adjacent-Input Crosstalk (Figure 10)			–50		db
Differential Gain Error (Note 5)	DG		2		%
Differential Phase Error (Note 5)	DP		1		Degree
Supply Current (Note 6) (Excluding REF+)	IAA		120	185	mA
A0, A1 Setup Time	11	10			ns
A0, A1 Hold Time	12	10			ns
RD*, WR* High Time	13	50			ns
RD* Asserted to Data Bus Driven	14	1			ns
RD* Asserted to Data Valid	15			40	ns
RD* Negated to Data Bus 3-Stated	16			20	ns
WR* Low Time	17	70			ns
Write Data Setup Time	18	10			ns
Write Data Hold Time	19	10			ns
Pipeline Delay (Note 7)		3	3	3	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 1.5 V for digital inputs and outputs. D0–D7, P0–P7, CSYNC* output load≤ 40 pF. VOUT, IOUT0, IOUT1 output load ≤ 40 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. See timing waveforms (Figures 11 and 12).

Note 1: The number of clock cycles that ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy is attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, and Fs = 14.32 MHz, T_{CASE} = Ambient. IAA (max) at VAA = 5.25 V, Fin = 10 MHz, and Fs = 20 MHz, T_{CASE} = 0° C.
Note 7: Pipeline delay is defined as discrete clock period delays in addition to the half-cycle analog sampling delay.

AC Characteristics *(continued)*



Note: Nominal device at ambient, timing reference points = 1.4 V

Figure 7. Bt252KPJ Output Delay vs. Capacitive Loading.

Test Circuits

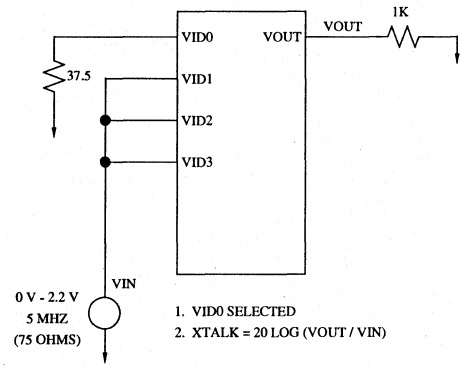


Figure 8. All-Hostile Crosstalk Test Circuit.

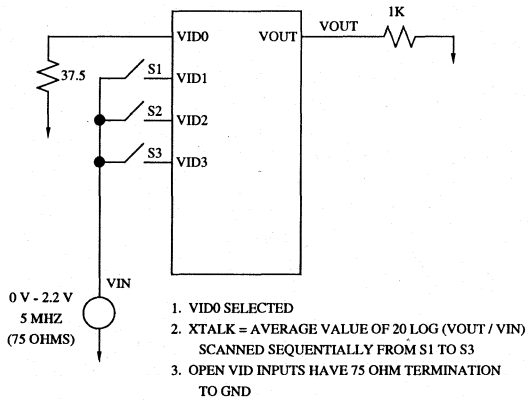


Figure 9. Single-Channel Crosstalk Test Circuit.

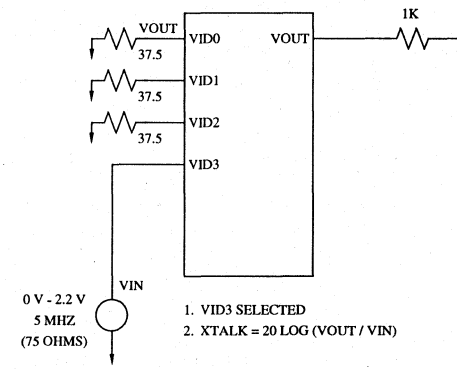


Figure 10. Adjacent-Input Crosstalk Test Circuit.

Timing Waveforms

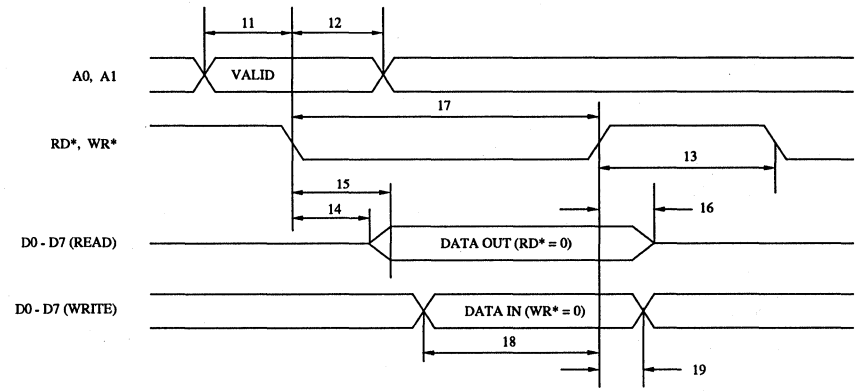


Figure 11. MPU Read/Write Timing.

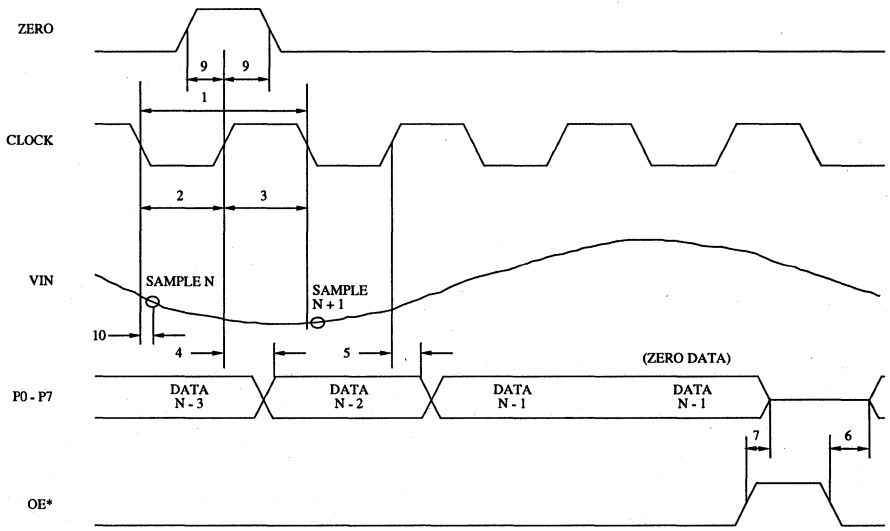
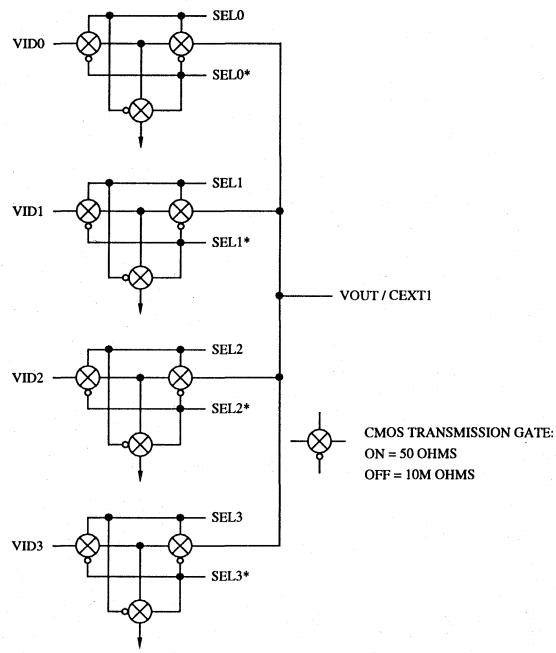


Figure 12. Video Input/Output Timing.

Analog Multiplexer Circuit



Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt252KPJ20	20 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt252EVM	Evaluation Board for the Bt252. Includes a Bt252KPJ30.		

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt254

20 MSPS
Monolithic CMOS
Triple-Channel
8-bit Image Digitizer

3

Distinguishing Features

- 20 MSPS Operation
- Bt253 Pin Compatiblility
- Three 8-bit Flash A/D Converters
- Two Sets Software-Selectable Analog Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- External Genlock Implementation
- Standard MPU Interface
- TTL Compatibility
- +5 V CMOS Monolithic Construction
- 84-pin PLCC Package
- Typical Power Dissipation: 1.5 W

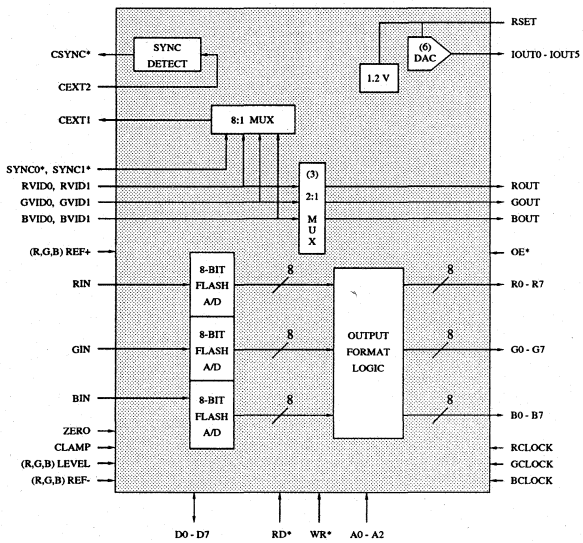
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt252
- Bt261

Functional Block Diagram



Product Description

The Bt254 Image Digitizer is designed to digitize three channels of video signals, such as RGB, YIQ, and YUV, generating up to 24 bits of color pixel information. The architecture also supports single-channel digitization of NTSC and CCIR video signals, generating 8 bits of gray-scale pixel information.

The Bt254 supports 24-bit true-color, 15-bit true-color, 8-bit true-color, and 8-bit pseudo- color modes. Its standard MPU interface can access various control functions.

Six analog inputs (two for each A/D) are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking. A TTL- compatible composite sync signal is output to interface to genlock circuitry. Two additional sync inputs support red, green, and blue sync video interfaces.

Optional MPU-controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF- inputs to the A/D converters. Zeroing and clamping signals are available to control the A/D timing for application-specific timing. The clamping levels are externally set through the red, green, and blue LEVEL pins.

Each A/D converter has its own clock input, top/bottom references, and LEVEL pin.

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L254001 Rev. C

Brooktree®

Circuit Description

General Operation

The Bt254 uses three 8-bit flash A/D converters to digitize the video signals. Each A/D digitizes analog signals in the range of REF– ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF–) to $FF (Vin ≥ REF+).

Each A/D converter has its own top and bottom reference: RREF+ and RREF– for the red A/D, GREF+ and GREF– for the green A/D, and BREF+ and BREF– for the blue A/D. Each A/D converter also has its own clock input: RCLOCK for the red A/D, GCLOCK for the green A/D, and BCLOCK for the blue A/D.

RIN, GIN, and BIN may be either DC or AC coupled to the video signals. If they are AC coupled, the CLAMP and (R,G,B) LEVEL controls may be used to DC restore the video signals.

Figure 1 shows the internal A/D architecture in detail. Figure 2 shows the input/output timing of each A/D on the Bt254. The samples are taken following the falling edge of (R,G,B) CLOCK. One positive CLOCK edge later, the registered data is output on (R,G,B) 0–7.

MPU Interface

As shown in the functional block diagram, the Bt254 supports a standard MPU interface (D0–D7, RD*, WR*, and A0–A2). MPU operations are asynchronous to the clocks.

A0–A2 address the internal registers, as itemized in Table 1.

Analog Signal Selection

The Bt254 supports two analog input sources for each A/D converter: RVID0 and RVID1, GVID0 and GVID1, and BVID0 and BVID1. The MPU specifies which are to be digitized through the command register.

The selected video signals are output onto ROUT, GOUT, and BOUT. ROUT, GOUT, and BOUT may be connected directly to RIN, GIN, and BIN, respectively, if no filtering or gain of the video signal is required.

If only the luminance information of a video signal that contains color subcarrier information is to be digitized, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low-pass filter, notch filter, or comb filter may be used to remove the chroma information.

Sync information (if present) will still be present on ROUT, GOUT, and BOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

A2, A1, A0	Addressed by MPU
000	command register
001	IOUT0 data register
010	IOUT1 data register
011	IOUT2 data register
100	IOUT3 data register
101	IOUT4 data register
110	IOUT5 data register
111	reserved

Table 1. Register Addressing.

Circuit Description *(continued)*

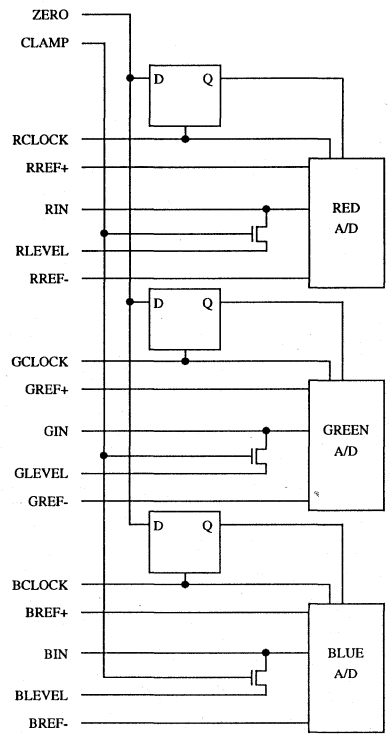


Figure 1. Internal A/D Architecture.

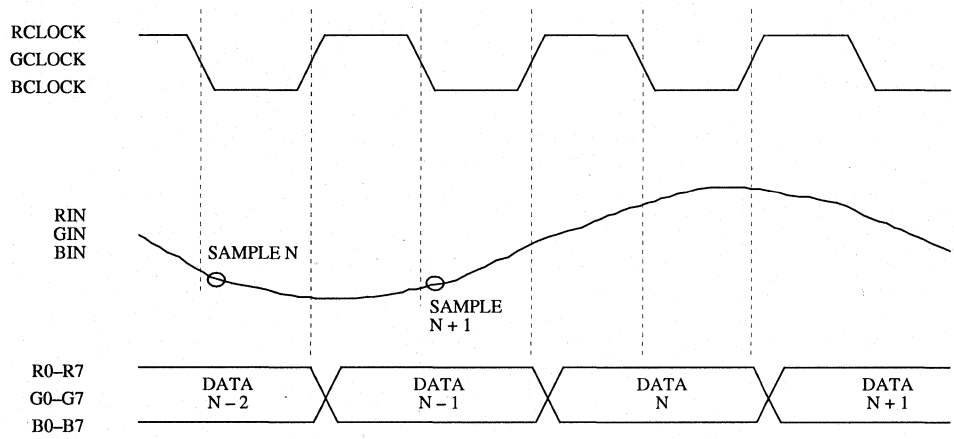


Figure 2. Input/Output Timing.

Circuit Description *(continued)*

A/D Reference Generation

As shown in Figure 3, the Bt254 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, RREF+ is connected to a 0.7–1.2 V reference (VREF), and RREF– is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7–1.2 V and no adjustment of gain or offset.

If jumpers J1 and J3 are selected, gain and offset of the video signal may be done through the MPU-adjustable outputs IOUT0 and IOUT1. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations, such as contrast enhancement or level adjustments, may be implemented. The TLC272 dual CMOS op-amps can be used for single +5 V operation. However, because single-supply op-amps have limitations, REF– may not be able to achieve a voltage below 300 mV with a single 5 V supply. Using an External Reference in the Application Information section contains further information.

GREF+, GREF–, BREF+, and BREF– may be similarly configured.

IOUT0–IOUT5 are current outputs (0–2.5 mA) generated by six 6-bit D/A converters. A 511 Ω RSET resistor generates a 2.35 mA full-scale output current. The 511 Ω resistors to GND generate a 0–1.2 V level that drives the (R,G,B)REF+ and (R,G,B)REF– inputs through voltage followers.

It is recommended that the DAC outputs do not drive the top of the reference ladders directly, as the reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of (R,G,B)REF– is desired, the DAC outputs must drive (R,G,B)REF– with a voltage follower.

A/D Zeroing

The ZERO input is used to zero the comparators and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the R0–R7, G0–G7, and B0–B7 outputs are not updated. They retain the data loaded before the ZERO cycle.

Each A/D converter uses its own clock to latch the ZERO signal. Thus, ZERO must be asserted for at least one clock cycle of the slowest clock.

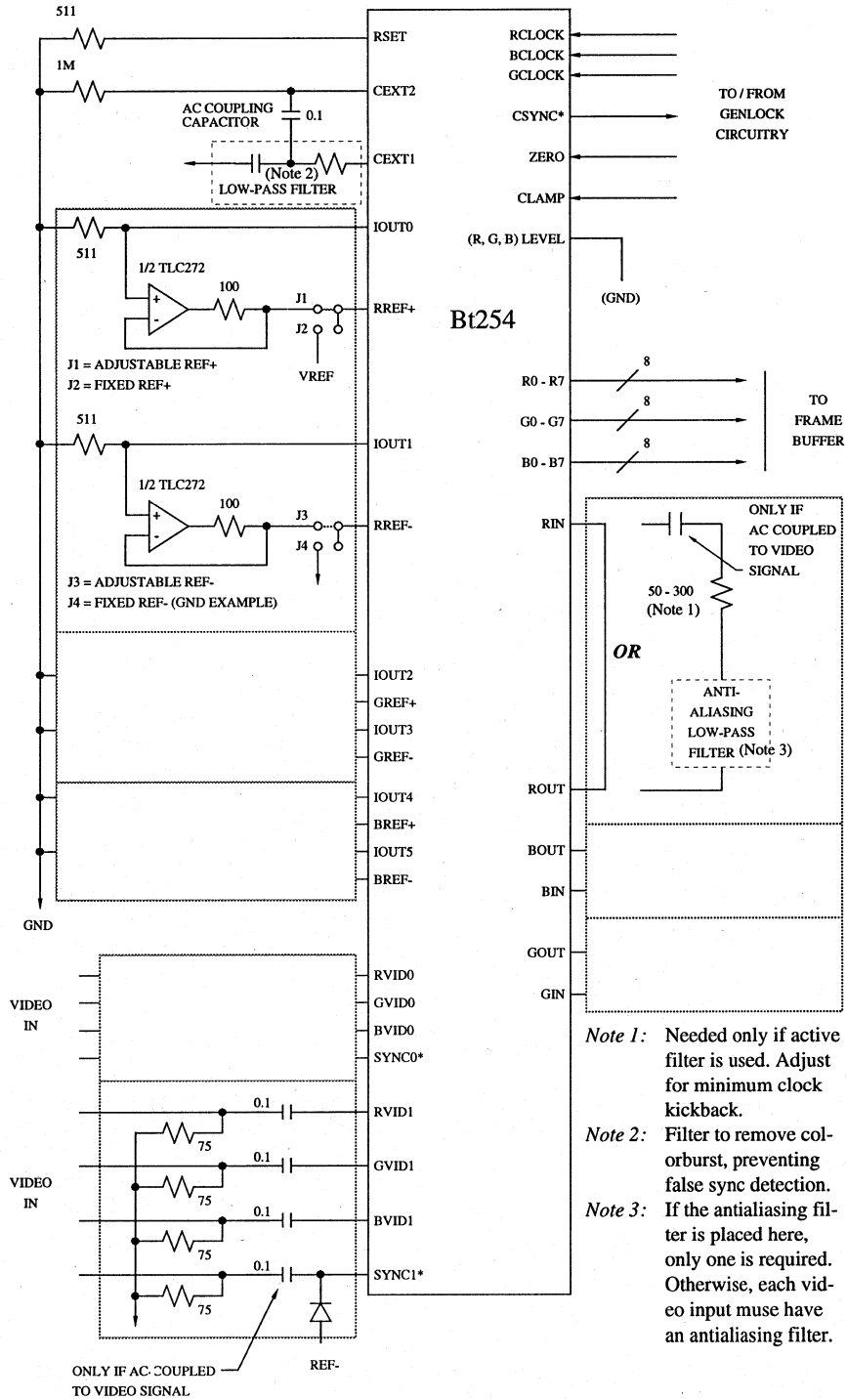
AC-Coupled Video and A/D Input Clamping

When video is AC coupled, capacitors are required on all video inputs. A capacitor may also be needed between (R,G,B)IN and (R,G,B)OUT, depending on the filtering implementation (see to Figure 3). The video mux will DC adjust the input video to prevent channel-to-channel crosstalk through the video mux.

During clamping, the resistances of the mux and clamp are approximately 100 and 50 Ω, respectively. Incorporation of the 0.1 µF clamp capacitor yields an RC time constant of 15 µs. On power-up or after a transition of the video input, the video signal will be completely DC restored in approximately three to five time constants. When the clamp is asserted on the back porch for 0.5–1.5 µs, it will take several lines of video will be required to properly DC restore the signal. For example, clamping the video signal for 1 µs during each line of video will require 75 lines of video for proper DC restoration. This is assuming five time constants are needed.

DC-Coupled Video

When video is DC coupled, the video levels must be within the digitization range of the A/D. To avoid channel-to-channel crosstalk through the video mux, nonsynchronized video sources must not drop more than 100 mV below ground. For example, if the black/blank level of the DC coupled video is at ground, an external sync clipper must be used to guarantee that the sync tip does not drop below –100 mV. If (R,G,B)IN is DC coupled to the video signal, all three level pins should float, or the clamp should be a logical zero.



Note 1: Needed only if active filter is used. Adjust for minimum clock kickback.

Note 2: Filter to remove colorburst, preventing false sync detection.

Note 3: If the antialiasing filter is placed here, only one is required. Otherwise, each video input muse have an antialiasing filter.

Figure 3. Typical Bt254 External Circuitry.

Circuit Description *(continued)*

Antialiasing Filtering and (R,G,B)IN Input Considerations

The input video must be passed through an antialiasing filter to meet Nyquist criteria. The filter can be placed between (R,G,B)IN and (R,G,B)OUT to filter all video sources or on each video input before the MUX. The 50–300 Ω resistor shown in Figure 3 after the low-pass filter is required only if an active low-pass filter is used. The resistor provides isolation from any clock kickback noise on (R,G,B)IN, preventing it from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on (R,G,B)IN. If no filter or a passive low-pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

If DC restoration and low-pass filtering are implemented, a 0.1 µF is required after the low-pass filter. If no filter or a passive low-pass filter is used, the capacitor is not required, as the DC restoration can still be implemented with the 0.1 µF capacitors on the (R,G,B)VID inputs.

Multiplexer Considerations

Maintaining DC levels within the rated compliance range is necessary to obtain the best linearity and crosstalk performance.

Sync Detect Circuitry

The Bt254 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. CSYNC* is output asynchronously to the clock, and there are no pipeline delays. (The output delay from Vin or SYNC* to CSYNC* is approximately 25 ns.)

The MPU specifies from which input to detect sync (negative sync polarity). The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC couples the video signal to the sync detection circuit. The sync tip is internally clamped to a DC level. The sync detect value determines the threshold above this DC level where the Bt254 detects sync. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero.

Two additional sync inputs (SYNC0* and SYNC1*) support red, green, and blue sync systems. SYNC0* and SYNC1* may be either TTL or normal video signal levels.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 3).

If the sync detection circuit is not used, CEXT2 should be connected to GND or VAA, and CEXT1 may float; or an unused (grounded) video input should be selected for the sync detector.

External Sync Detection

CEXT1 may be connected to an external sync detector circuit. In this case, CEXT2 should be connected directly to GND or VAA, and the CSYNC* output should be left floating.

The sync analog multiplexer may still be used to select from which video source to detect sync information. As the multiplexer switches analog video signals, the selected video source will be output onto CEXT1.

Color Output Modes

The Bt254 outputs several modes of color information, as specified in Table 2.

R0–R7, G0–G7, and B0–B7 are three-stated while OE* is a logical one.

Output Pins	24-Bit True Color Mode (00)	15-Bit True Color Mode (01)	8-Bit True Color Mode (10)	8-Bit Pseudo Color Mode (11)
R7	R7	0	R7	G7
R6	R6	R7	R6	G6
R5	R5	R6	R5	G5
R4	R4	R5	G7	G4
R3	R3	R4	G6	G3
R2	R2	R3	G5	G2
R1	R1	G7	B7	G1
R0	R0	G6	B6	G0
G7	G7	G5	R7	G7
G6	G6	G4	R6	G6
G5	G5	G3	R5	G5
G4	G4	B7	G7	G4
G3	G3	B6	G6	G3
G2	G2	B5	G5	G2
G1	G1	B4	B7	G1
G0	G0	B3	B6	G0
B7	B7	0	R7	G7
B6	B6	0	R6	G6
B5	B5	0	R5	G5
B4	B4	0	G7	G4
B3	B3	0	G6	G3
B2	B2	0	G5	G2
B1	B1	0	B7	G1
B0	B0	0	B6	G0

Table 2. Color Output Configurations.

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit.

D7	Digitize select (0) xVID0 (1) xVID1	This bit specifies which analog input is to be digitized. The selected signals are output onto ROUT, GOUT, and BOUT.
D6–D4	Sync detect select (000) RVID0 (001) RVID1 (010) GVID0 (011) GVID1 (100) BVID0 (101) BVID1 (110) SYNC0* (111) SYNC1*	These bits specify which input is to detect composite sync information. The sync information is output onto CSYNC*.
D3, D2	Color output select (00) 24-bit true color (01) 15-bit true color (10) 8-bit true color (11) 8-bit pseudo color	These bits specify color output mode select (see Table 2). In mode (11) the red and blue A/D converters are ignored.
D1	Reserved (logical zero)	A logical zero must be written to this bit when writing to the command register.
D0	Sync detect level select (0) 125 mV (1) 50 mV	This bit specifies the amount above the sync tip to slice CEXT2 for sync detection.

IOUT Data Registers

These six 6 bit registers specify the output current on the IOUT0–IOUT5 outputs, from 0 mA ($00) to full scale ($FC). The 6 bits of data are used to drive the DACs. D0 and D1 (the 2 LSBs) must be programmed to be logical zeros.

These registers may be written to or read by the MPU at any time and are not initialized. D0 is the least significant bit.

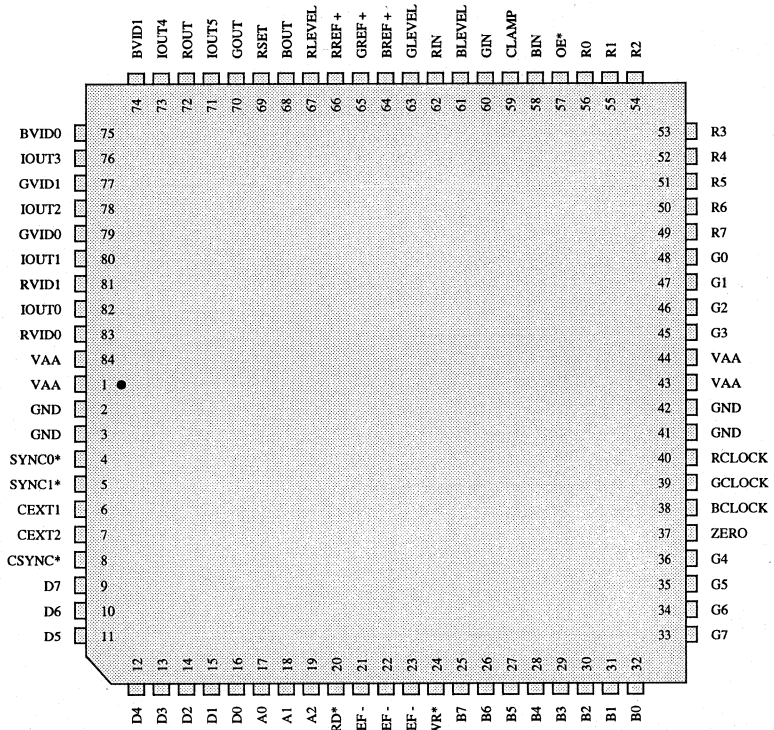
Pin Descriptions

Pin Name	Description
General Reference Functions	
RSET	Full-scale adjust control. An external 511 Ω resistor must be connected between this pin and GND. RSET is used to provide reference information to the internal D/A converters (see Figure 3).
IOUT0–IOUT5	Current outputs. The amount of output current is specified by the IOUT data registers. External 511 Ω resistors are typically connected between these pins and GND (see Figure 3). The relationship between full-scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (Ω)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC couple the video signal to the sync detect circuitry. A 1M Ω resistor must also be connected between CEXT2 and GND. If AC coupled, amplitude is < 2 Vp–p.
A/D Functions	
RREF+, GREF+, BREF+	Red, green, and blue top of resistor ladder (voltage input). These set the (R,G,B)IN voltage level that corresponds to $FF from the appropriate A/D converter. For noise immunity reasons, decoupling capacitors are *not* recommended for the REF+ pins.
RREF–, GREF–, BREF–	Red, green, and blue bottom of resistor ladder (voltage input). These set the Vin voltage level that generates $00 from the appropriate A/D converter.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D converters are zeroed. The red A/D converter latches ZERO on the rising edge of RCLOCK, the green A/D converter latches ZERO on the rising edge of GCLOCK, and the blue A/D converter latches ZERO on the rising edge of BCLOCK. During zeroing cycles, R0–R7, G0–G7, and B0–B7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the RIN, GIN, and BIN inputs are forced to the voltage level on the (R, G, B) LEVEL pins to DC restore the video signals. When RIN, GIN, and BIN are DC coupled to the video signals, the LEVEL pins should float, or CLAMP should be a logical zero. CLAMP is asynchronous to the clocks.
RLEVEL, GLEVEL, BLEVEL	Red-, green-, and blue-level control inputs (voltage inputs). These inputs specify what voltage level is to be used for DC restoration while CLAMP is a logical one. When RIN, GIN, and BIN are DC coupled to the signals, the LEVEL pins should float, or CLAMP should be a logical zero.
Input Selection Functions	
RIN, GIN, BIN	A/D converter inputs. The analog signals to be digitized should be connected to these analog input pins.
RVID0, RVID1, ROUT	Red channel analog inputs and analog output. RVID0 and RVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto ROUT. Unused inputs should be connected to GND.
GVID0, GVID1, GOUT	Green channel analog inputs and analog output. GVID0 and GVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto GOUT. Unused inputs should be connected to GND.
BVID0, BVID1, BOUT	Blue channel analog inputs and analog output. BVID0 and BVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto BOUT. Unused inputs should be connected to GND.

Pin Descriptions *(continued)*

Pin Name	Description
Timing Functions	
RCLOCK, GCLOCK, BCLOCK	Clock inputs (TTL compatible). It is recommended that these pins be connected together and driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected from the xVID0 or xVID1 input (as specified by the command register), converted to TTL levels, and output onto this pin. SYNC0* or SYNC1* may also be selected as inputs to the sync detector. CSYNC* is output asynchronously to the clocks, and there are no pipeline delays.
SYNC0*, SYNC1*	Sync inputs. Sync information may be input with these pins and output onto CSYNC*. SYNC0* and SYNC1* may be either TTL or normal video signal levels. Unused inputs should be connected to GND.
Digital Control Functions	
R0–R7, G0–G7, B0–B7	Digitized video data outputs (TTL compatible). R0–R7 are output following the rising edge of RCLOCK, G0–G7 are output following the rising edge of GCLOCK, and B0–B7 are output following the rising edge of BCLOCK. They are three-stated if OE* is a logical one. R0, G0, and B0 are the least significant bits.
OE*	Output enable control input (TTL compatible). A logical one three-states R0–R7, G0–G7, and B0–B7 asynchronously to the clocks.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device with D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0–A2	Address control inputs (TTL compatible). A0–A2 address the internal registers as itemised in Table 1. They are latched on the falling edge of RD* or WR*.
Power and Ground	
VAA	Analog power. All VAA pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND as close to the device as possible. (Ceramic chip capacitors are preferred.)
GND	Ground. All GND pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup.

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt254, the CMOS digitizer layout examples in the Bt 208, Bt251, or Bt253 Evaluation Module Operation and Measurements, Application Notes AN-13, 14, and 15, respectively, should be studied before PC board layout is begun. These application notes can be found in the *Brooktree Applications Handbook.*

The layout should be optimized for lowest noise on the Bt254 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

A single ground plane covering both digital and analog logic should be used.

Power Planes

The Bt254 and any associated analog circuitry should have their own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt254.

The regular PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt254 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that the regular PCB power plane does not overlay the analog power plane.

Supply Decoupling

The bypass capacitors should be installed with the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

The VAA and GND pins should have a 0.1 µF ceramic chip capacitor located as close as possible to the device pins. The capacitors should be connected directly to the VAA and GND pins with short, wide traces.

Digital Signal Interconnect

The digital signals of the Bt254 must be isolated as much as possible from the analog signals and other analog circuitry to prevent crosstalk. Also, the digital signals should not overlay the analog power plane.

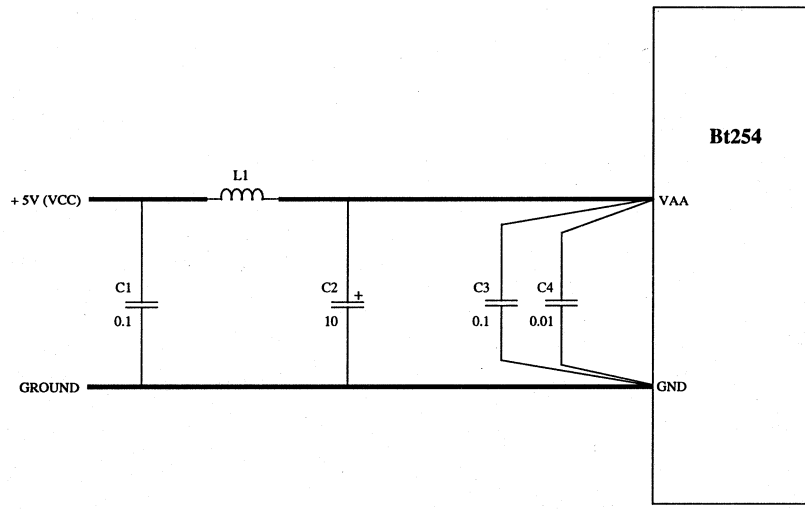
Termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs. Microstrip techniques should be employed to keep video trace impedance at 75 Ω, to match standard coax impedance.

Also, routing of high-speed TTL signals close to the analog signals should be avoided to minimize noise coupling.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1, C3	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2	10 µF tantalum capacitor	Mallory CSR13G106KM
C4	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt254.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

Zeroing

As the comparators on the Bt254 must be periodically zeroed, it is convenient to assert ZERO during each horizontal blanking interval.

Before the Bt254 is used after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications, this will be transparent because of the number of horizontal scan lines that will have occurred before the Bt254 is used.

While the recommended zeroing interval is maintained, the Bt254 will meet linearity specifications. *The longer the time between zeroing intervals, the more the linearity error increases.*

Increasing the Resolution of DACs

With a 511 Ω resistor connected between each DAC output (IOUT0–OUT5) and GND, the resolution of the ladder adjustment is 19 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 5 shows a circuit that allows adjustment of the REF+ inputs from 0.714–1 V with 4.5 mV resolution. With the DAC data = $00, 0.714 V is output; if the DAC data = $FC, 1 V is output.

As the typical maximum DAC output current is 2.35 mA (RSET = 511 Ω), if a 0.286 V adjustable range is desired, R1 || R2 must equal 121 Ω. The minimum output voltage desired determines the ratio of R1 and R2 as follows:

$$Vmin = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF–) may be adjusted from 0–0.286 V with 1.125 mV resolution by using a 121 Ω resistor to ground rather than a 511 Ω resistor. While the minimum range is 0 V, the resistor to ground may be used to adjust the total range and, thus, the resolution.

Using An External Reference

Figure 6 illustrates the use of a 1.2 V LM385 and a TLC272 to generate a 0–1.2 V reference for applications that require a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that can operate from a single +5 V supply.

A 100 Ω resistor is recommended to prevent the TLC272 from ringing caused by a clock kickback, as shown in Figure 6. If an op-amp is chosen that has a better transient response than the TLC272, the resistor may not be needed. This circuit may also be used to drive the Ref– if a value other than ground is desired. Because single-supply op-amps have limitations, Ref– may not be set below ~300 mV. To drive Ref– to true 0 V in the op-amp configuration, a dual supply must be used. *Extreme care must be used in power sequencing to ensure all positive supplies (op-amp and A/D) power on before the negative supply. This will prevent latchup of the A/D.*

Input Ranges

Table 3 lists some common video signal amplitudes. For signals that exceed 1.2 V, the signal should be attenuated with a resistor divider network.

When a full-scale range less than 0.7 V is used to digitize, the Bt254's integral linearity errors are constant in terms of voltage, regardless of the value of the reference voltage. Lower reference voltages will, therefore, produce larger integral linearity errors in terms of LSBs.

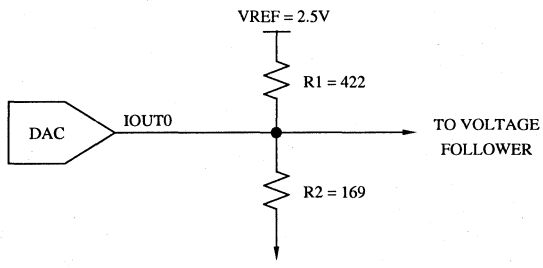


Figure 5. Increasing DAC Output Resolution.

Application Information *(continued)*

For example, when the reference difference is set to 0.6 V, 0.6 V video signals may be digitized. However, the integral linearity error will increase to about ±1.8 LSB, and the SNR will be about 40 db. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB and an SNR of about 39 db.

Output Noise

Although the A/D does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

The output noise of the A/D may be reduced by adjusting the duty cycle of the clock. This is especially true above 10 MHz clock operation. Uncorrelated noise less than 1 percent peak to peak will be perceived with the same quality as that of a consumer 1/2-inch VCR.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 643066-2.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. ADC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

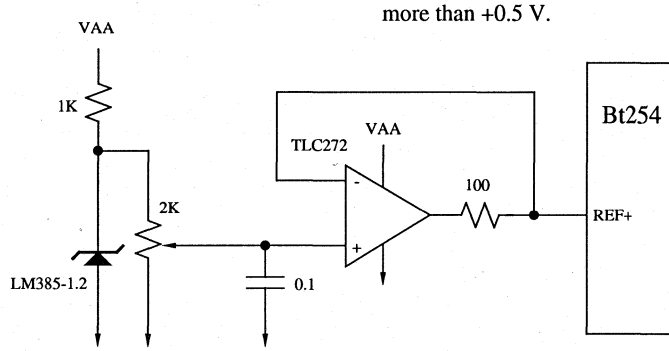


Figure 6. Using an External Reference.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/ sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 3. Video Signal Tolerances.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Voltage References					
Top	xREF+	0.7	1	2.0	V
Bottom	xREF–	0	0	1.3	V
Difference (Top–Bottom)		0.7	1	1.2	V
VID0–VID1 Amplitude Range		0.5		VAA–0.5	V
Multiplexer Compliance (DC)		–0.2		+2.2	V
(R,G,B) IN Amplitude Range		0.7	1	1.2	V
(R,G,B) IN Input Range			REF– to REF+		V
CEXT AC Amplitude		0.2 Vp–p		2.0 Vp–p	V
(R,G,B) LEVEL Input Voltage		GND–0.5	REF–	REF+	V
Zeroing Interval			60	150	µs
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Input Voltage	VIN, VIDx	GND–0.5		VAA + 0.5	V
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (Note 1)	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
A/D Coding (Table 4)					Binary
No Missing Codes			guaranteed		
(R,G,B) IN Inputs (Note 2)					
CLAMP = 0					
Input Current (Leakage)	IB			1	µA
Input Capacitance	CAIN		35		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
(R,G,B) VID0,1 Inputs (Note 3)					
Input Impedance to (R,G,B) OUT					
Input Selected			100		Ω
Input Deselected			10		MΩ
Input Capacitance			15		pF
(R,G,B) REF+ Reference Inputs					
Input Impedance			500		Ω
Digital Inputs					
Input High Voltage	VIH	2.0			V
Input Low Voltage	VIL			0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
RGB (0–7) Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
CSYNC* Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Output Capacitance	COUT		10		pF

See test conditions and notes on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0–IOUT5 Outputs					
DAC Output Current		0		2.5	mA
DAC Output Impedance			100		kΩ
DAC Output Capacitance			20		pF
DAC Accuracy					
Differential Linearity Error	DL			±1	LSB
Integral Linearity Error	IL			±1	LSB
Monotonicity			guaranteed		

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1 V and (R,G,B)REF– = GND. REF– ≤ Vin ≤ REF+ and (R,G,B) LEVEL = float. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: This is a best-fit linearity (offset independent).
Note 2: (R,G,B) LEVEL = GND.
Note 3: ROUT, GOUT, and BOUT connected to GND.

Vin (V) (Note 1)	(R,G,B) 0–7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

Note 1: With (R,G,B)REF+ = 1.000 V and (R,G,B)REF– = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV.

Table 4. A/D Coding Example.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			20	MHz
Multiplexer Switching Time	Tmux		100		ns
Clock Cycle Time	1	50			ns
Clock Low Time	2	20			ns
Clock High Time	3	20			ns
P0–P7 Output Delay Time (Figure 7)	4			40	ns
P0–P7 Output Hold Time	5	9			ns
OE* Asserted to P0–P7 Valid	6			20	ns
OE* Negated to P0–P7 3-Stated	7			20	ns
ZERO Setup Time	8	0			ns
ZERO Hold Time	9	20			ns
ZERO, CLAMP High Time (Note 1)		1			Clock
Aperture Delay	10		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW			Fs/2	MHz
Transient Response (Note 2)			1		Clock
Overload Recovery (Note 3)			1		Clock
Zero Recovery Time (Note 4)			1		Clock
RMS Signal-to-Noise Ratio	SNR				
Fin = 4.20 MHz, Fs = 12.27 MHz			44		db
Fin = 4.20 MHz, Fs = 13.50 MHz			44		db
Fin = 4.20 MHz, Fs = 14.32 MHz			44		db
Fin = 5.75 MHz, Fs = 13.50 MHz			43		db
Fin = 5.75 MHz, Fs = 14.75 MHz			43		db
Fin = 5.75 MHz, Fs = 17.72 MHz			43		db
Fin = 10.0 MHz, Fs = 20.00 MHz			39		db
RMS Signal & Distortion-to-Noise Ratio	SINAD				
Fin = 4.20 MHz, Fs = 12.27 MHz			42		db
Fin = 4.20 MHz, Fs = 13.50 MHz			42		db
Fin = 4.20 MHz, Fs = 14.32 MHz			42		db
Fin = 5.75 MHz, Fs = 13.50 MHz			41		db
Fin = 5.75 MHz, Fs = 14.75 MHz			41		db
Fin = 5.75 MHz, Fs = 17.72 MHz			41		db
Fin = 10.0 MHz, Fs = 20.00 MHz			37		db
Total Harmonic Distortion	THD				
Fin = 4.20 MHz, Fs = 12.27 MHz			47		db
Fin = 4.20 MHz, Fs = 13.50 MHz			47		db
Fin = 4.20 MHz, Fs = 14.32 MHz			47		db
Fin = 5.75 MHz, Fs = 13.50 MHz			47		db
Fin = 5.75 MHz, Fs = 14.75 MHz			47		db
Fin = 5.75 MHz, Fs = 17.72 MHz			47		db
Fin = 10.0 MHz, Fs = 20.00 MHz			44		db

See test conditions and notes on next page.

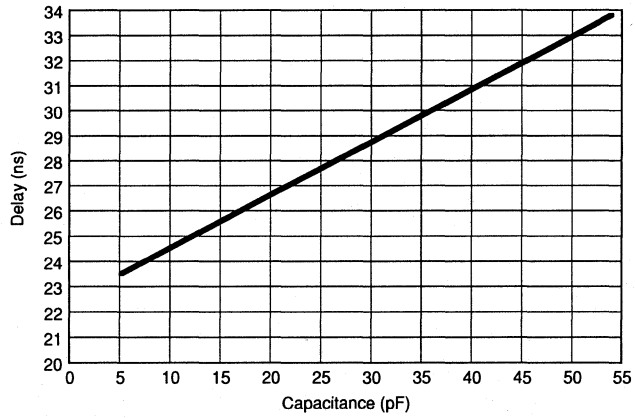
AC Characteristics *(continued)*

Parameter	Symbo	Min	Typ	Max	Units
Spurious Free Dynamic Range	SFDR				
Fin = 4.20 MHz, Fs = 12.27 MHz			50		db
Fin = 4.20 MHz, Fs = 13.50 MHz			50		db
Fin = 4.20 MHz, Fs = 14.32 MHz			50		db
Fin = 5.75 MHz, Fs = 13.50 MHz			50		db
Fin = 5.75 MHz, Fs = 14.75 MHz			50		db
Fin = 5.75 MHz, Fs = 17.72 MHz			50		db
Fin = 10.0 MHz, Fs = 20.00 MHz			47		db
Analog Multiplexer Crosstalk					
All-Hostile Crosstalk (Figure 8)			–50		db
Single-Channel Crosstalk (Figure 9)			–50		db
Adjacent-Input Crosstalk (Figure 10)			–50		db
Differential Gain Error (Note 5)	DG		2		%
Differential Phase Error (Note 5)	DP		1		Degree
Supply Current (Note 6) (Excluding REF+)	IAA		270	390	mA
A0, A1 Setup Time	11	10			ns
A0, A1 Hold Time	12	10			ns
RD*, WR* High Time	13	50			ns
RD* Asserted to Data Bus Driven	14	1			ns
RD* Asserted to Data Valid	15			40	ns
RD* Negated to Data Bus 3-Stated	16			20	ns
WR* Low Time	17	50			ns
Write Data Setup Time	18	10			ns
Write Data Hold Time	19	10			ns
Pipeline Delay (Note 7)		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1 V and (R,G,B)REF– = GND. REF– ≤ Vin ≤ REF+ and (R,G,B) LEVEL = float. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 1.5 V for digital inputs and outputs. D0–D7 output load ≤ 40 pF. CSYNC*, R0–R7, G0–G7, and B0–B7 output load ≤ 40 pF. ROUT, GOUT, BOUT, and IOUT0–IOUT5 output load ≤ 40 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. See timing waveforms (Figures 11 and 12).

Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, and Fs = 14.32 MHz, T_{CASE} = Ambient. IAA (max) at VAA = 5.25 V, Fin = 10 MHz, and Fs = 20 MHz, T_{CASE} = 0° C.
Note 7: Pipeline delay is defined as discrete clock-period delays in addition to the half-cycle sampling delays.

AC Characteristics *(continued)*



Note: Nominal device at ambient, timing reference points = 1.4 V

Figure 7. Bt254KPJ Output Delay versus Capacitive Loading.

Test Circuits

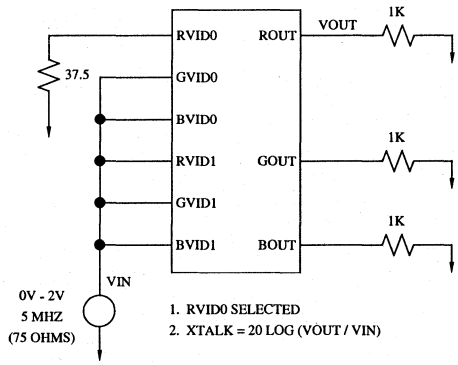


Figure 8. All-Hostile Crosstalk Test Circuit.

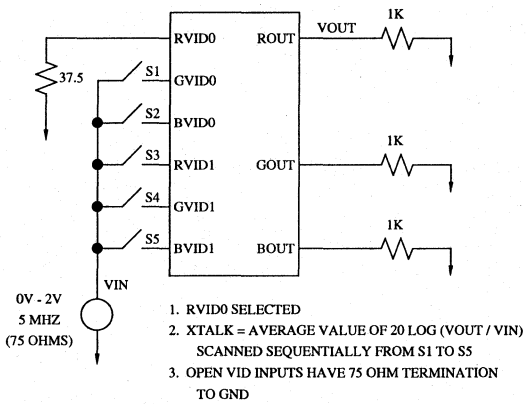


Figure 9. Single-Channel Crosstalk Test Circuit.

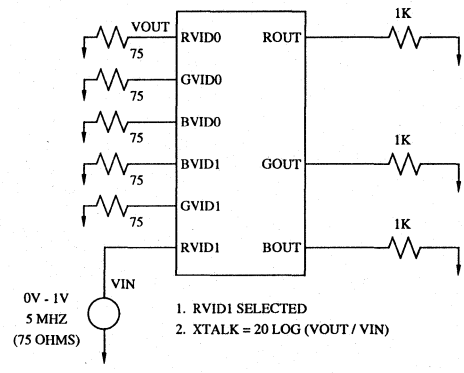


Figure 10. Adjacent-Input Crosstalk Test Circuit.

Timing Waveforms

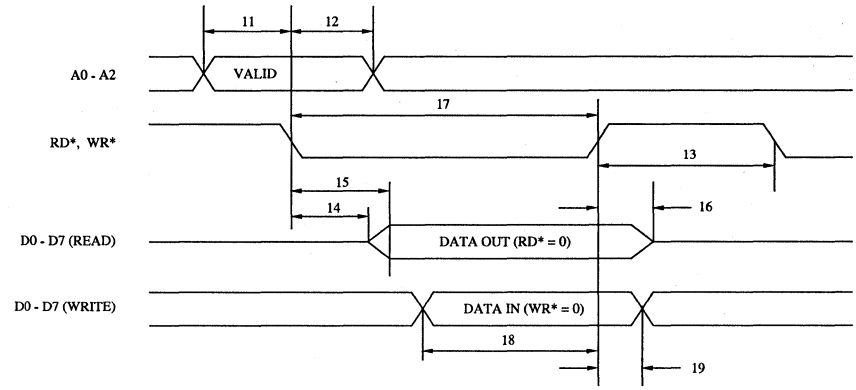


Figure 11. MPU Read/Write Timing.

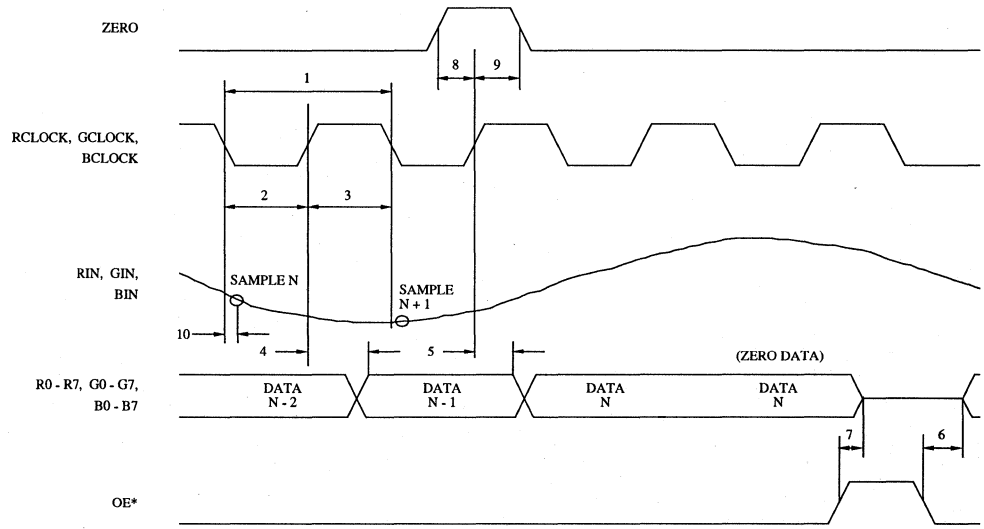
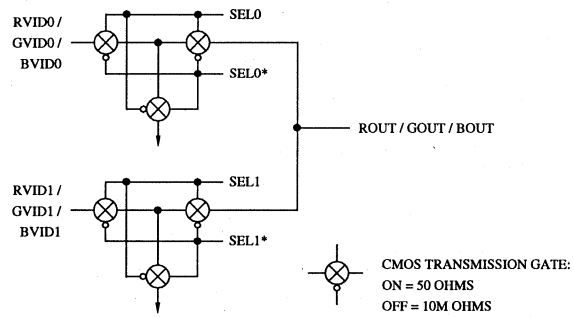


Figure 12. Video Input/Output Timing.

Analog Multiplexer Circuit



Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt254KPJ20	20 MHz	84-pin Plastic J-Lead	0° to +70° C
Bt254EVM	Evaluation Board for the Bt254. Includes a Bt254KPJ30.		

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt261

30 MHz Pixel Clock Monolithic CMOS HSYNC Line Lock Controller

3

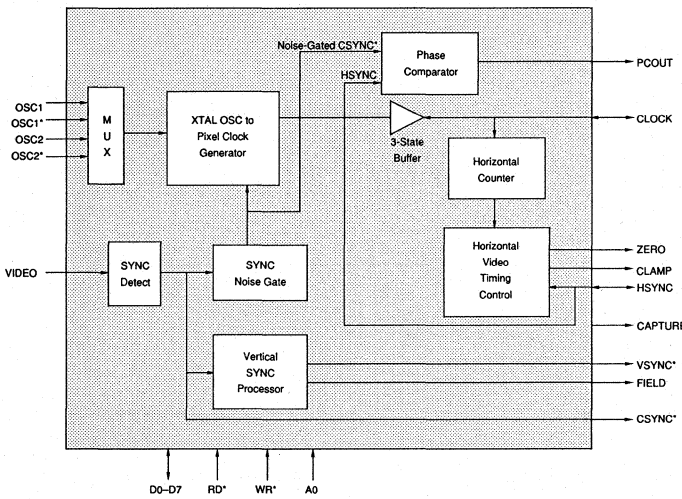
Distinguishing Features

- Programmable 12-bit Video Timing
- Bidirectional HSYNC and CLOCK Pins
- Horizontal Sync Noise Gating
- External VCO Support
- Standard MPU Interface
- TTL Compatible
- + 5 V Monolithic CMOS
- 28-pin PLCC Package
- Typical Power Dissipation: 300 mW

Applications

- Image Processing
- Video Digitizing
- Desktop Publishing
- Graphic Art Systems

Functional Block Diagram



Product Description

The Bt261 HSYNC Line Lock Controller is designed specifically for image capture applications.

Either composite video or TTL composite sync information is input via VIDEO. An internal sync separator separates horizontal and vertical sync information. Programmable horizontal and vertical video timing enables recovery of both standard and nonstandard timing information.

An external VCO may be used in conjunction with the on-chip phase comparator for implementation of clocks locked to the horizontal frequency.

Alternately, a high-speed clock (OSC) may be divided down to generate the pixel clock. The phase of the generated pixel clock is adjusted to align with the noise-gated CSYNC. The higher the OSC clock rate, the lower the pixel clock jitter (the maximum being one half the OSC clock period). The OSC inputs may be configured to be either TTL or ECL compatible. Thus, four TTL clocks, two TTL clocks and one differential ECL clock, or two differential ECL clocks may be used. The ECL clock inputs are designed to be driven by 10KH ECL using a single +5 V supply.

The CLAMP and ZERO outputs are programmed by the MPU to DC restore the video signal and to zero the Image Digitizer or A/D converter at the appropriate time.

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
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L261001 Rev. F

Brooktree®

MPU Interface

As seen in the functional block diagram, the Bt261 supports an MPU interface via (D0–D7, RD*, WR*, and A0). MPU operations are asynchronous to the clocks. Refer to the Timing Waveforms section for further information.

A0 is used to select either the internal 5-bit address register (A0 = logical zero) or the control register specified by the address register (A0 = logical one). ADDR5–ADDR7 are ignored during MPU write cycles, and are in an unknown state when read by the MPU. ADDR0 corresponds to D0 and is the least significant bit. ADDR0–ADDR4 increment following any MPU read or write cycle to a control register other than the address register. MPU write cycles to reserved addresses are ignored and MPU read cycles from reserved addresses return invalid data.

Table 1 shows the internal register addressing.

ADDR0 - ADDR4	Addressed by MPU
$00	command register_0
$01	command register_1
$02	command register_2
$03	command register_3
$04	VSYNC sample register
$05	OSC count low register
$06	OSC count high register
$07	status register
$08	HSYNC start low register
$09	HSYNC start high register
$0A	HSYNC stop low register
$0B	HSYNC stop high register
$0C	CLAMP start low register
$0D	CLAMP start high register
$0E	CLAMP stop low register
$0F	CLAMP stop high register
$10	ZERO start low register
$11	ZERO start high register
$12	ZERO stop low register
$13	ZERO stop high register
$14	FIELD gate start low register
$15	FIELD gate start high register
$16	FIELD gate stop low register
$17	FIELD gate stop high register
$18	noise gate start low register
$19	noise gate start high register
$1A	noise gate stop low register
$1B	noise gate stop high register
$1C	HCOUNT start low register
$1D	HCOUNT start high register
$1E	reserved
$1F	reserved

Table 1. Internal Register Addressing.

Video Input / Sync Detector

Either an AC-coupled video signal or a DC-coupled TTL-compatible composite sync signal may be input via the VIDEO input pin (negative-going sync polarity). When AC coupled, the clamping circuitry attempts to force the VIDEO pin voltage during sync tips to VCC/2.

Command register_0 specifies the threshold above the sync tip to use for sync detection. If the sync tip on VIDEO is below the selected threshold, composite sync information is detected and output onto CSYNC* with no pipeline delay and asynchronous to the pixel clock.

Typically, the VIDEO input will be connected to the TTL-compatible CSYNC* output of the Bt252/254 Image Digitizer, and the highest sync slicing level will be selected.

Horizontal Counter

The rising edge of pixel clock (CLOCK) increments a 12-bit horizontal counter used to generate horizontal video timing information. The value of the counter is compared to various registers to determine when signals are to be asserted (set high) and negated (set low). $000 corresponds to the falling edge of CSYNC*. When the part is used with an external high-speed oscillator and divided down to generate the pixel clock, there is no pipeline delay between CSYNC* and count zero. However, when the part is used in phase locked loop mode with an external VCO, there is a three-pixel-clock pipeline delay between CSYNC* and count zero.

Horizontal Sync Separation

The Bt261 separates horizontal sync information from CSYNC* by use of the horizontal noise gate register, which derives gated composite sync by removing equalization and serration pulses at half-line intervals.

Two 12-bit noise gate start and stop registers specify at what horizontal count (with pixel clock resolution) to respectively ignore or accept falling sync transitions on CSYNC*.

The sync noise gating is provided to filter incorrect horizontal sync information from noisy video signals. The noise gating also serves a second purpose: to filter serration and equalization pulses at half-line intervals from CSYNC* during the vertical retrace interval. This enables steady synchronization of horizontal sync information during vertical retrace intervals.

HSYNC Input/Output

The HSYNC output may be programmed to be either active high or active low. The start value sets the rising edge and the stop value sets the falling edge of HSYNC relative to count zero of the horizontal counter. The beginning or falling edge of HSYNC is typically programmed to be coincident with the beginning of the noise-gated CSYNC*.

The HSYNC output may be three-stated via the command register.

HSYNC may also be configured as an input, enabling external circuitry to generate HSYNC and drive the phase comparator.

VSYNC* Output

The VSYNC register defines the clock count from the falling edge of nongated CSYNC* at which point CSYNC* is sampled to determine if the video signal is in the vertical interval. Since nongated CSYNC is used to start the VSYNC counter, two samples per horizontal line are taken during the vertical interval because of equalization and serration pulses.

For each scan line that the sample is a logical zero, the VSYNC* output is a logical zero. Thus, the VSYNC sample register should be programmed so that the sample occurs well after the end of CSYNC* and before subsequent equalization/serration pulses. VSYNC is output on the rising edge of PCLK.

FIELD Output

The FIELD output is derived from the vertical sync information. By positioning the FIELD gate start/stop values a half-line interval apart, the half-line delay in vertical sync during the second field's vertical interval can provide a signal to distinguish the fields.

The FIELD output is clocked by VSYNC*. Therefore, FIELD start and stop values should not coincide with VSYNC or VSYNC + HCOUNT/2. The FIELD GATE start and stop values define the clock count, from the beginning of the horizontal counter, at which to set the input to a register high (start value) or low (stop value). This register is clocked by VSYNC, which occurs half a line later in the transition from field 1 to field 2. The FIELD start and stop values must be separated by, approximately, HCOUNT/2, so that opposite states are reported on subsequent fields. The polarity is such that, with the FIELD GATE start value programmed less than the stop value, FIELD output is toggled high to indicate the beginning of field 1 and toggled low to indicate the beginning of field 2. The polarity of the FIELD pin may be inverted by swapping the start and stop register values.

Figure 1 illustrates the operation of the FIELD gate and FIELD output.

CLAMP and ZERO Outputs

The CLAMP and ZERO outputs are provided to control the clamping and zero timing of the A/D converter or Image Digitizer. The start and stop timing is programmable by the MPU (in pixel clock cycles). ZERO is used to autocalibrate the comparators of the A/D converter or Image Digitizer. CLAMP is used to DC-restore the video signal. Both CLAMP and ZERO may be programmed to be either active high or active low.

Capture Output

The Bt261 outputs a CAPTURE signal, which is a command register bit (CR05) synchronized to the vertical sync or FIELD signals.

To capture a single frame of video in an interlaced system, the MPU resets the capture bit (CR5) low, then sets it high before the next rising edge of field. At the rising edge of FIELD, the CAPTURE output will be set to a logical zero until the next rising edge of FIELD (one frame time), when the CAPTURE output is set high.

In a non-interlaced system, the MPU resets the capture bit (CR5) low, then sets it high before the falling edge of VSYNC*. When the falling edge of VSYNC* occurs, the capture output will be set high until the next falling edge of VSYNC*.

Circuit Description *(continued)*

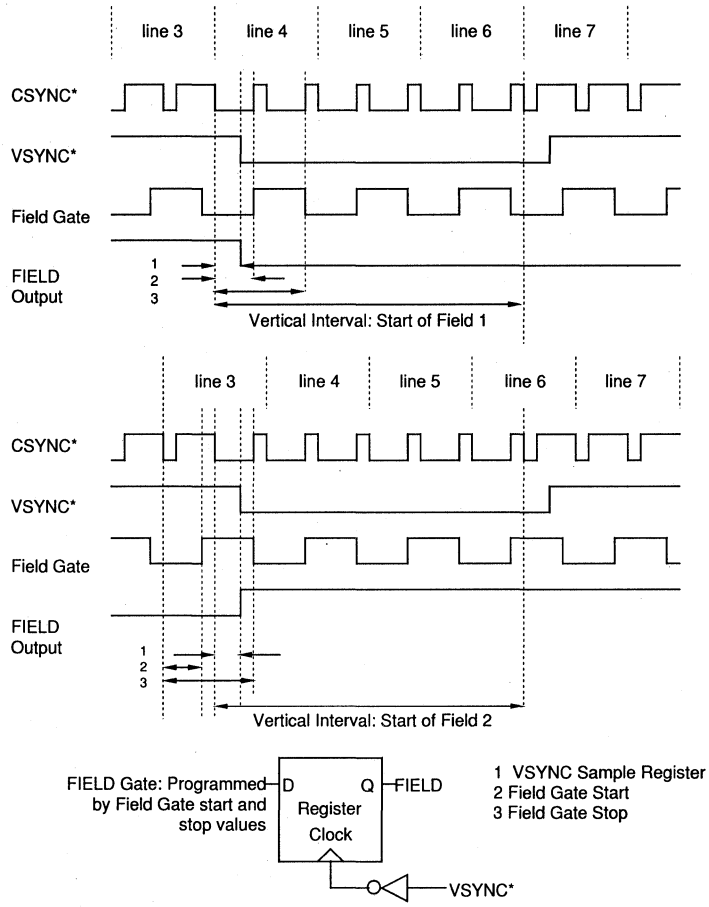


Figure 1. FIELD Gate and FIELD Output Operation.

External VCO Pixel Clock Generation

An external VCO or pixel clock may be used to drive the Bt261, as shown in Figure 2. The pixel clock signal (from the VCO if one is used) is connected to any one of the OSC input pins (the one used must be selected by command bits CR00–CR02). When the clock pin is configured as an input, it must also be driven by the pixel clock signal. The VCO must have positive control voltage (positive voltage forces a higher frequency).

An on-chip phase comparator is available to compare the phase of HSYNC and the falling edge of the noise-gated CSYNC*.

If the falling edge of the noise-gated CSYNC* occurs before the falling edge of HSYNC, the phase comparator "dumps" a charge onto an external capacitor, increasing the VCO frequency. If the falling edge of noise-gated CSYNC* occurs after the falling edge of HSYNC, the phase comparator "sinks" a charge from the external capacitor, decreasing the VCO frequency. Because of the internal delay elements, the phase comparison occurs approximately 500 ns after the falling edge of CSYNC*.

The output of the phase comparator is PCOUT and it is a TTL-compatible three-statable output, which assumes a high-impedance state outside the phase-comparison window. The width of the output pulse on PCOUT is equal to the phase difference with a gain of 4π/VCC.

The "divide-by-N" for the PLL loop is the 12-bit HCOUNT register. Command register bits CR07 and CR06 must be set to (1,0) for proper operation. This configures the horizontal counter to be reset to zero upon reaching the HCOUNT value, which should be set to the number of pixels per line, minus 1.

Circuit Description *(continued)*

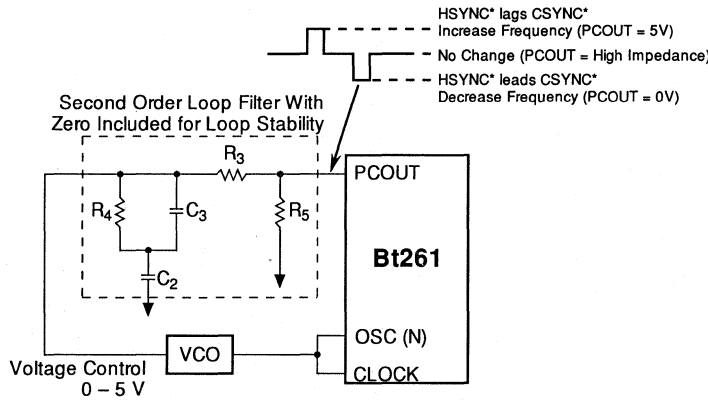


Figure 2. External VCO Configuration.

Phase/Frequency Detector Operation

The phase comparator compares the phase of the falling edge of the noise-gated CSYNC* and generated HSYNC. The HSYNC can be either internally generated (and optionally output onto the HSYNC pin) or an external HSYNC signal can be input via the HSYNC pin.

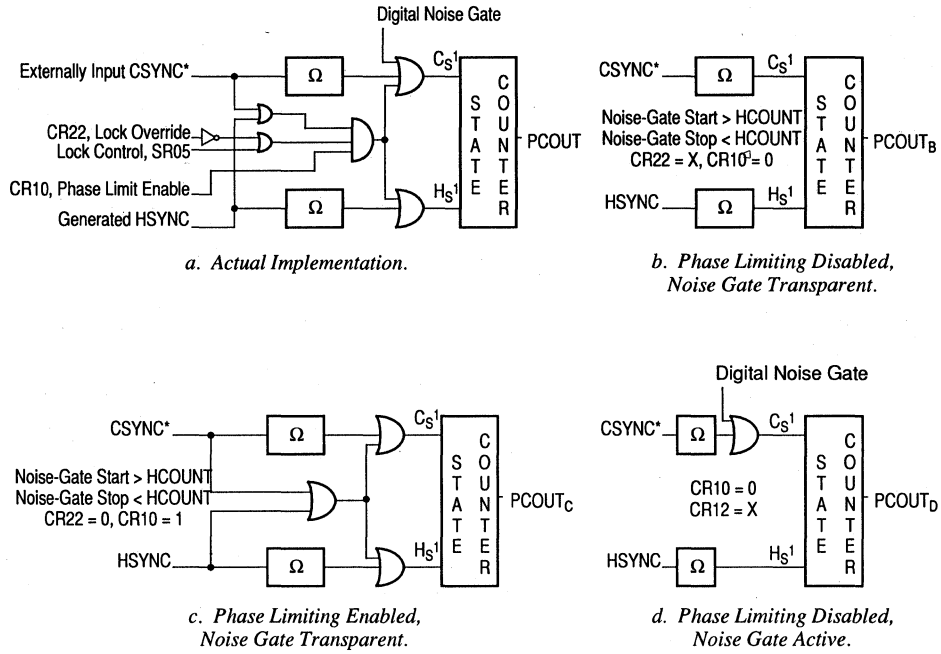
Two Forms of Noise Gating Available

The Bt261 offers two forms of noise gating to remove half-line serration and equalization pulses during the vertical interval, which can cause loop disturbances and wavering at the beginning of the displayed field. The first is a digital noise gate that is programmed in pixel clock events following the falling edge of composite sync. The noise-gate start must occur before the halfway point (HCOUNT/2). The noise-gate stop value must relate to a clock count a maximum distance from the end of line, defined as one half the minimum width of the serration pulse, less 500 ns. One half the equalization pulse provides the maximum error deviation for correct phase comparison. The 500 ns delay is required because of the offset used during phase limiting. Even when phase limiting is disabled, this delay is included in both the noise-gated CSYNC* and generated HSYNC* paths. Therefore, it must be accounted for in the noise-gate stop value (see Figure 3a–d). The earliest possible noise-gate stop value permits the widest phase-error tracking range. For an acquisition range greater than one half the minimum equalization pulse width (±2.3 µs or 3.6 percent of nominal RS170A), the noise gate should be set transparent by programming a start value greater than HCOUNT and a stop value less than HCOUNT until lock is verified in the active field. The status registers can be monitored to verify lock.

A second analog noise gate is activated through the phase-limit feature. This function limits the duration of phase correction to about 500 ns per coincidence of noise-gated CSYNC* and generated HSYNC. The Phase Frequency Detector (PFD) makes its comparison about 500 ns after each falling transition of either HSYNC or CSYNC*. However, with phase limiting enabled, the comparison occurs only for a 500 ns interval while both signals are low. Thus, by limiting phase comparison to a 500 ns window, transitions at half-line intervals are not detected. The phase truncation that occurs when this feature is used limits the instantaneous phase-error impulse to about 500 ns that the loop can track. This may not be adequate for some video signal sources, such as heterodyne VCRs (without time-base correction) or electronic still photography (e.g., floppy disk) cameras. If the Bt261 is programmed to permanently phase limit (CR22 set low), the phase-comparison duty is only ~0.8 percent and loop settling time is prolonged dramatically. Figures 3, 4, and 5 are block diagrams and examples demonstrating noise gating and phase limiting.

Both forms of noise gate can be used together for maximum acquisition range with phase-error impulse tracking up to ~3.6 percent of the line rate (the maximum depends upon the minimum width of serration pulses). For an acquisition range that exceeds ±2.3 µs, the digital noise gate must be set transparent by temporarily setting noise-gate start value greater than HCOUNT with a stop value less than HCOUNT. Acquisition can then be automatic and the phase-limit feature (CR10 = CR22 = 1) can be used with phase-lock pixel count (CR27–CR24) programmed for less than 500 ns and the phase-lock line count (CR37–CR30) programmed for less than the field line count, minus the closed-loop settling time. When phase lock is verified (by strobing CR10 low and reading back

Circuit Description *(continued)*



Ω = 350-650 ns delay
PCOUT = Phase-comparator output

Figure 3. (a) Actual Gate-Level Implementation of Phase Limiting and Noise Gating (b,c, and d) Minimized Block Diagrams Corresponding to Waveforms in Figure 5.

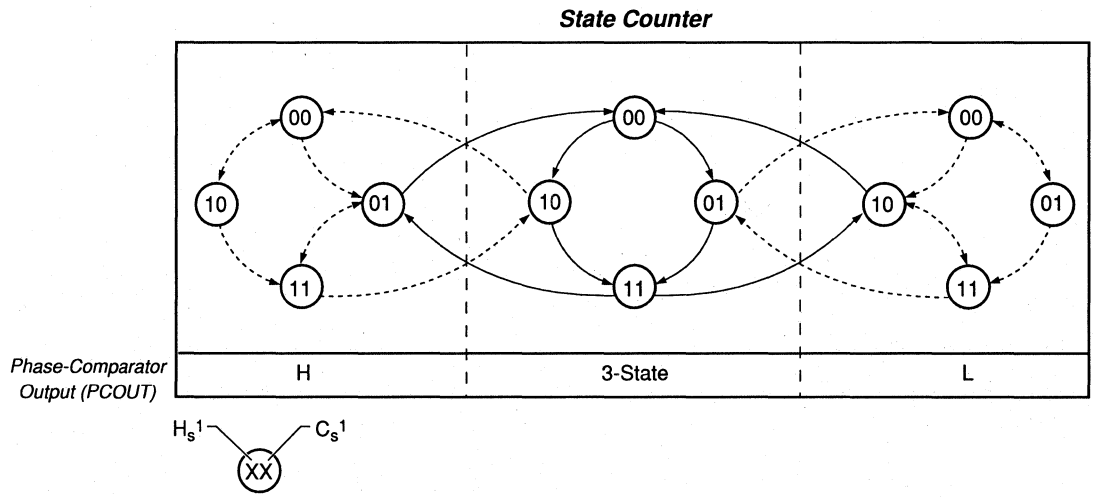
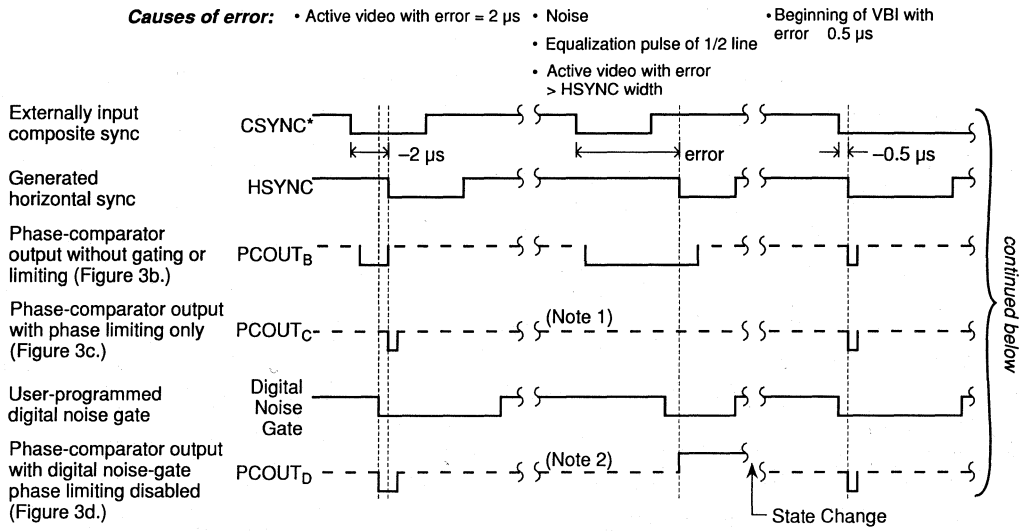
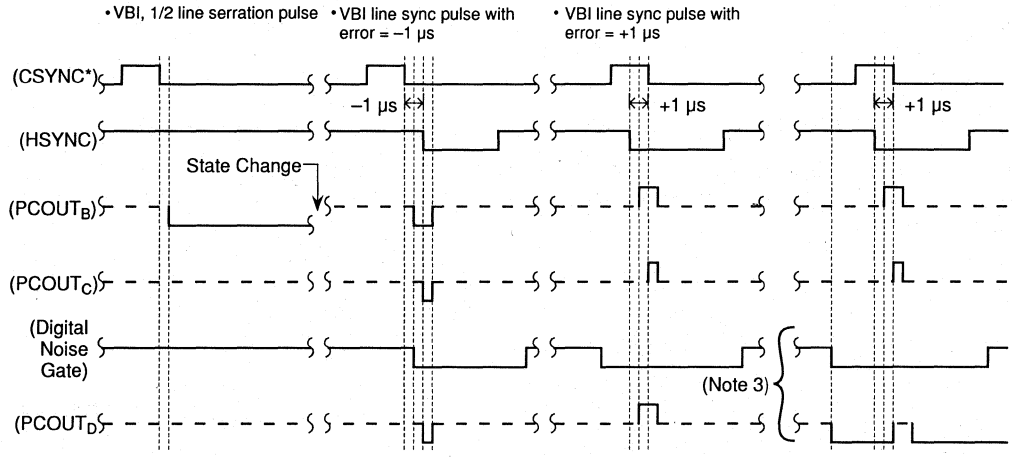


Figure 4. Phase-Comparator State Diagram.

Circuit Description *(continued)*





VBI = Vertical Blanking Interval

Note 1: Phase limiting will not adjust for errors greater than HSYNC width, correctly ignoring half-line equalization pulses.

Note 2: The digital noise gate will activate the phase comparator correctly but not deactivate, which would improperly set the VCO input voltage.

Note 3: This is an improperly programmed digital noise gate with erroneous phase-comparator output. Noise-gate stop value is not within 500 ns of the end of line.

In general, the digital noise gate will improperly activate the phase-comparator if the error in the VBI is greater than ± 1/2 serration pulse width.

Figure 5. Examples of Phase Comparator Operation With Different Types of Error and Different Implementations of Phase Limiting and Noise Gating.

SR0 = 1 or monitoring SR05), the digital noise-gate can be reactivated by restoring the noise-gate start value to less than HCOUNT/2. When the digital noise gate is active, the phase-limit feature should be disabled for maximum phase-error tracking range (determined by the phase-lock loop's closed-loop impulse response, but limited by one-half minimum serration pulse or noise-gate width). If instantaneous phase errors exceed phase-lock pixel count, the status register SR00 bit is forced to zero, even though the loop may be tracking the phase-error impulses. Since large phase errors usually occur in the vertical blanking interval, it is prudent to reset and monitor the lock status bit after the phase-lock line count has expired in the active field. A consistent zero in SR00 would dictate restarting the acquisition sequence outlined above to maintain phase lock. Similarly, SR05 may be monitored to determine locking status.

The Status Registers SR00 and SR05 Used in Automatic Phase Limiting

Bits 0 and 5 of the status register can be used to debug phase-locked-loop operation of the Bt261. Phase-lock *pixel-count* bits CR27–CR24 define a pixel count used by the Bt261 to determine if the part is in "Lock." The Bt261 compares the time during which the phase comparator is active (the PLL correction time) with the time defined in pixel count. If the compare time is less than phase-lock pixel count, the loop is considered locked and SR00 is not altered. If the compare time is greater than the phase-lock pixel count, SR00 is reset to zero. Previous to query, SR00 must be set to one by writing to command bit CR12.

CR37–CR30 contains the phase-lock line count. This register determines the number of lines that must have a phase error less than that defined in the CR27–CR24 phase-lock pixel count for the system to be considered continuously locked. SR05 is reset to zero if there have been phase-lock line-count number of continuous lines with phase error less than that defined in the phase-lock pixel count. SR05 cannot be altered by the MPU. SR05 is set to one if SR00 is set to zero on any line (indicating a phase error greater than that defined in phase-lock pixel count).

Bit 5 of the status register is used by the phase-limiting circuitry to determine if phase limiting should be enabled or disabled. If phase limiting is automatic, i.e., when phase limiting is enabled and lock is not overridden, (CR10 = CR22 = 1), SR05 determines whether phase limiting should be performed. SR05 is the lock control indicated in Figure 3a.

The active period compared with the value in CR27–CR24 is output directly from the phase comparator. Because of this, all digital noise-gate and phase-limit operation is included when the phase error is compared with the phase-lock pixel-count value. Therefore, the value in CR27–CR24 must be less than 500 ns in the typical case or 350 ns in the worst case commercial temperature range. This requirement ensures that a phase-limited line is not incorrectly interpreted as a locked line.

SR05 can be used as a PLL debug tool. If the status register is addressed and the RD* pin of the Bt261 is held low, then SR05 will indicate the lock status. This bit will set low when lock is held for the number of lines defined in the phase-lock line count. When this condition is observed while the phase-comparator output is viewed through two vertical intervals, the Bt261 response relative to the loop performance can be studied. Lock should be indicated well before the next vertical interval (see Figure 6). Phase-limit enable must be deactivated during this evaluation (CR10 = 0); otherwise, phase limiting will affect the ability to monitor the loop-acquisition time.

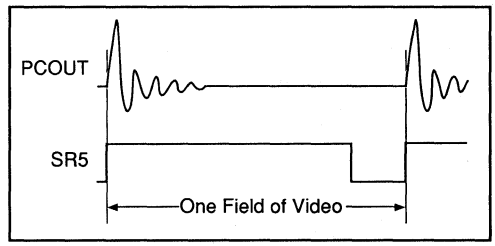


Figure 6. PLL Performance Can Be Monitored Using SR05.

Asynchronous (Unlocked) Pixel Clock Generation

Four oscillator clock inputs are provided (OSC), selectable by the MPU, configurable as either TTL or differential ECL inputs (designed to be driven by 10KH ECL using a single +5 V supply).

The selected OSC input is divided down to the desired pixel clock rate and duty cycle. The pixel clock low and high times are programmable by the MPU (as a function of OSC clock cycles) via the OSC count low and high registers. Note that both the rising and falling edge of the OSC inputs are used when specifying the OSC count (for example, values of 2 for the OSC count low and high registers will divide the OSC clock symmetrically by two).

Circuit Description *(continued)*

The generated pixel clock is synchronized to the falling edge of the noise-gated CSYNC* each scan line. Each time a horizontal sync is detected on the VIDEO input, the CLOCK output is resynchronized by the OSC clock so that the beginning of a pixel clock cycle and the falling edge of the noise-gated CSYNC* are coincident (see Figure 7) within one half the period of the OSC input. While there is some sampling jitter on CLOCK associated with the falling edge of CSYNC*, the residual jitter in the remaining line interval is strictly a function of the OSC clock source jitter, symmetry, and amplitude/slew rate jitter, at the OSC input. Differential OSC signals of fast edges will minimize the latter contribution.

There are three ways of controlling the horizontal counter, as determined by command bit CR07 and CR06.

CR07 and CR06 are (0,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter stops at the HCOUNT value and is held there until the next falling edge of the noise-gated CSYNC*, at which time it is reset to zero. CLOCK stops in the high state at the HCOUNT value, until the next falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero by the falling edge of the noise-gated CSYNC*. CLOCK will be continuous and is resynchronized to each falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is known and is a fixed number.

CR07 and CR06 are (1,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero upon reaching HCOUNT, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK is continuous and is resynchronized to each falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is cleared at the falling edge of the noise-gated CSYNC*, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK will be continuous and is resynchronized to the falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is not known or an arbitrary value is to be used.

CR07 and CR06 are (1,0): Resets H counter at HCOUNT only.

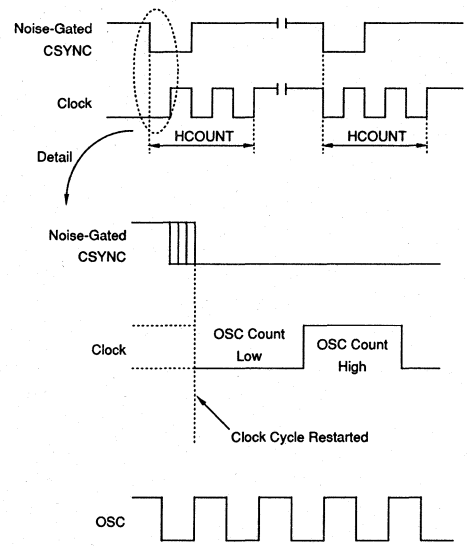


Figure 7. Pixel Clock Output Timing When Generated From Higher Speed Oscillator.

Horizontal Counter

The 12-bit horizontal counter is incremented on the rising edge of CLOCK. It is not accessible by the MPU.

Command Register_0

This command register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to D0 and is the least significant bit.

CR07, CR06 Horizontal counter control

- (00) reserved
- (01) reset each noise-gated CSYNC*
- (10) reset to zero upon reaching HCOUNT
- (11) use both modes (01) and (10)

A value of (01) forces the horizontal counter to be reset to zero at the beginning of every noise-gated CSYNC*. These modes should be selected when using a high–speed oscillator to divide down and generate the pixel clock.

A value of (10) specifies that the horizontal counter will be reset to zero upon reaching the HCOUNT value. This mode should be selected when using the horizontal counter as a simple divide-by-N circuit (such as when using an external VCO in a traditional phase-locked loop application). Mode 11 can be used to correct for missing sync pulses on the input video.

CR05 Capture strobe

This bit is synchronized to VSYNC* and FIELD and output onto the CAPTURE output pin.

CR04, CR03 Sync detect select

- (00) 25 mV
- (01) 50 mV
- (10) 100 mV
- (11) 125 mV

These bits specify how much above the sync tip to slice VIDEO for sync detection. If inputting TTL sync information, the highest slicing level should be selected.

CR02–CR00 Clock input select

- (000) TTL compatible OSC1
- (001) TTL compatible OSC1*
- (010) TTL compatible OSC2
- (011) TTL compatible OSC2*
- (100) ECL compatible OSC1, OSC1*
- (101) ECL compatible OSC2, OSC2*
- (110) reserved
- (111) reserved

These bits specify which OSC input is to be used to generate pixel clock information. ECL input selection is compatible with 10KH differential ECL driven by a single +5 V supply.

Note: When the clock pin is driven, the selected OSC pin(s) must also be driven.

Command Register_1

This command register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to D0 and is the least significant bit.

CR17	Interlaced or noninterlaced select (0) noninterlaced operation (1) interlaced operation	This bit specifies whether an interlaced or noninterlaced video signal is being digitized. The MPU must write a logical zero followed by a logical one to this bit to reset the status bit (SR00) to a logical one.
CR16	CLOCK output disable (0) drive CLOCK output (1) three-state CLOCK output	This bit specifies whether the CLOCK pin is three-stated (logical one) or is actively driven (logical zero). A logical one enables an external pixel clock to drive the internal counters.
CR15	CSYNC* output disable (0) drive CSYNC* output (1) three-state CSYNC* output	This bit specifies whether the CSYNC* output is three-stated (logical one) or is actively driven (logical zero).
CR14	VSYNC* output disable (0) drive VSYNC* output (1) three-state VSYNC* output	This bit specifies whether the VSYNC* output is three-stated (logical one) or is actively driven (logical zero).
CR13	HSYNC output disable (0) drive HSYNC output (1) three-state HSYNC output	This bit specifies whether the HSYNC output is three-stated (logical one) or is actively driven with the internally generated HSYNC signal (logical zero). If external circuitry is driving the HSYNC pin, this bit must be set to a logical one.
CR12	Reset lock loss status bit (0) set status bit SR00 (1) inactive	This bit sets SR00, which is used to indicate loss of lock. The MPU must write a logical zero to this bit to restart the process.
CR11	Phase comparator input select (0) HSYNC pin (1) internally generated HSYNC	One input to the phase comparator is recovered composite sync. The other input to the phase comparator is specified by this bit to be either the internally generated HSYNC or the HSYNC pin. When an external source is driving the HSYNC pin, this bit should be set to a logical zero.
CR10	Phase limit enable (0) inhibit phase limiting (1) enable phase limiting	If this bit is a logical one, both horizontal sync signals (recovered and either internally or externally generated) must be present to adjust the VCO frequency. If one is missing, the VCO frequency is not adjusted. If this bit is a logical zero, a missing horizontal sync signal will adjust the VCO frequency.

Command Register_2

This command register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to D0 and is the least significant bit.

CR27–CR24 Phase lock pixel count

(0001) 2 clock cycles
:
(1111) 16 clock cycles

These bits specify the maximum number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal (either internally or externally generated) to be considered locked.

If the number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal exceed this value, lock is considered to be lost for that scan line, and the lock loss status bit (SR00) is set to a logical zero.

CR23 Pixel clock mask enable

(0) continuous pixel clock
(1) stop pixel clock at HCOUNT

If this bit is a logical one, the CLOCK output is stopped in the logical one state when the horizontal counter reaches the HCOUNT value. This ensures a minimum pulse width when the noise-gated CSYNC* signal is asynchronously sampled. If it is a logical zero, the CLOCK output will continuously clock (if command bit CR16 is a logical zero). This bit is ignored if an external pixel clock is driving the CLOCK pin (command bit CR16 is a logical one).

CR22 Lock override

(1) normal operation
(0) tell phase comparator it's locked

If the Bt261 goes out of lock, the phase limiter is automatically disabled until it is back in lock. If this bit is a logical zero, this function is overridden.

CR21, CR20 Pixel clock select

(00) OSC inputs
(01) external pixel clock
(10) OSC drives CLOCK direct
(11) reserved

These bits specify whether to use the OSC-generated pixel clock or an external pixel clock (driving the CLOCK pin) to clock internal counters.

In mode (00), the selected OSC input(s) is divided down by the OSC count registers to generate the pixel clock (CLOCK).

If mode (01) is selected, an external pixel clock must drive the CLOCK pin and one of the OSC inputs. Command bit CR16 must be a logical one.

If mode (10) is selected, the OSC clock is output directly onto the CLOCK pin. The OSC count low and high registers are ignored.

Command Register_3

This command register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to D0 and is the least significant bit.

CR37–CR30 Phase lock line count

(0000 0000) 1 scan line
(0000 0001) 2 scan lines
:
(1111 1111) 256 scan lines

These bits specify the number of consecutive scan lines for which lock must be maintained. If lock is not maintained for the specified number of scan lines, the phase limiter is disabled only if command bit CR22 is a logical one. SR05 is set to zero if lock is maintained for the specified number of scan lines.

VSYNC Sample Register

This 8-bit register specifies the number of pixel clock cycles after the falling edge of nongated CSYNC* at which to sample the CSYNC* signal each scan line. By doing this, two samples per line will be taken during the vertical interval when half-line pulses are present. The FIELD gate is programmed with the horizontal counter values (which use only noise-gated CSYNC*); when sampling of the input sync occurs, VSYNC will toggle one half-line earlier at the beginning of field two as opposed to the beginning of field one. This register may be written to or read by the MPU at any time and is not initialized. Values from $00 (1) to $FF (256) may be specified. A value of 1/8 HCOUNT is recommended (~8 µs for the 15.75 KHz line-rate video). This is different from the 1/4 and 3/4 HCOUNT required for FIELD-gate start and stop values, and greater than the 5 µs maximum width of sync pulses. For a conventional video input with negative-going syncs, this produces a negative-going VSYNC* at the number of clock cycles specified after the falling CSYNC* edge. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, the output of this signal with respect to CSYNC* may be delayed (see Figure 8).

OSC Count Low and High Registers

These two 4-bit registers specify the number of rising and falling edges of an OSC input the pixel clock output (CLOCK) is to be low and high. Values from $02 (2) to $OE (15) may be specified. These registers may be written to or read by the MPU at any time and are not initialized. A value of $00 results in no pixel clock generation while the OSC inputs are used. The counters clock on both the rising and falling edge of the selected OSC input. For example, values of 4, 4 in OSC count low and high would result in a pixel clock with one fourth the frequency of the oscillator.

Status Register

This status register may be read by the MPU at any time and is not initialized. MPU write cycles to this register are ignored. SR00 corresponds to D0 and is the least significant bit.

SR00 Lock-loss status (pixel count related)

(0) lock loss detected
(1) reset or no lock loss

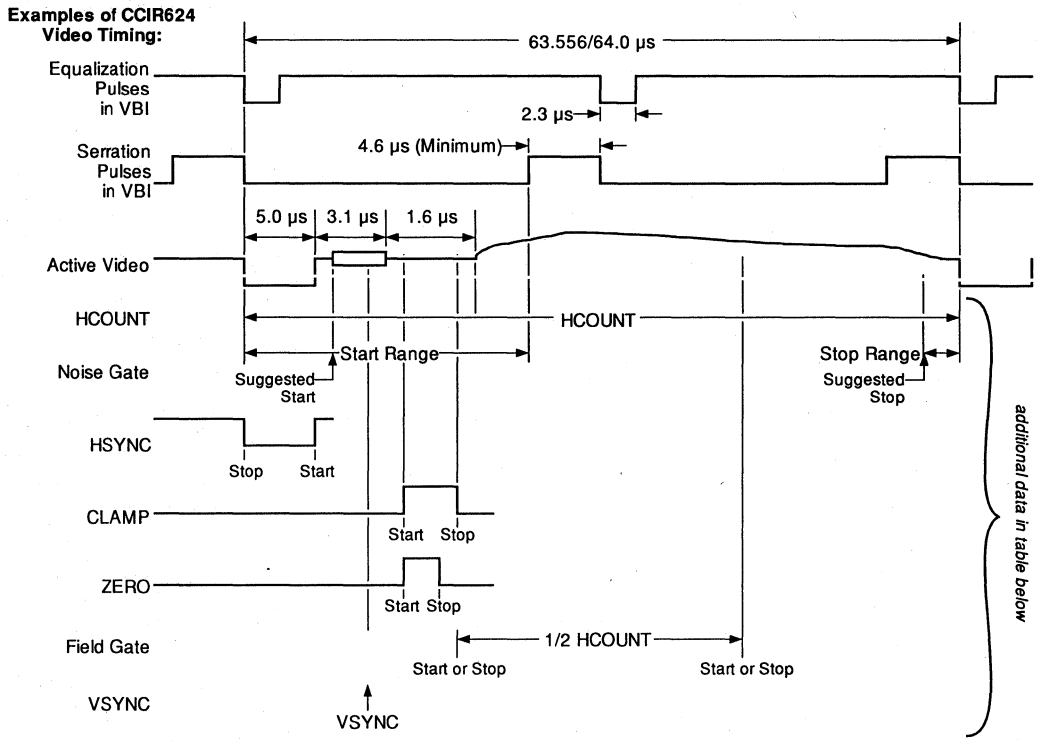
This bit reset if loss of lock is indicated. "Loss of lock" is defined as a greater phase error between noise-gated CSYNC* and generated HSYNC* than the phase-lock pixel count (CR27–CR24). It is reset by writing to command bit CR12.

SR05 Lock-loss bit (line-count related)

(1) lock loss detected
(0) lock detected for at least line-count number of lines

This bit is set if one line of video has a phase error between generated HSYNC and noise-gated CSYNC* greater than that defined by the phase-lock pixel count (CR24–CR27). This bit is reset if there have been phase-lock line count (CR37–CR30) consecutive lines with error less than that defined in the phase-lock pixel count.

Internal Registers *(continued)*



Pixel Clock Rate		NTSC(M) 12.2 MHz dec	hex	PAL (B, G, I) 14.75 MHz dec	hex
Line Rate		**63.556 µs**		**64.0 µs**	
(HCOUNT) Number of pixels minus 1		779	30B	943	3AF
(Noise Gate)	Start 7 µs Stop 61.76 µs	88 758	58 2F6	104 917	68 395
(HSYNC) Negative polarity, 4.7 µs wide	Start 4.7 µs Stop 0 µs	59 0	3B 0	70 0	46 0
(CLAMP) One may CLAMP on burst back porch or sync tip	Start 8.5 µs Stop 9 µs	107 113	6B 71	126 134	7E 86
(ZERO)	Start 8.5 µs Stop 8.75 µs	107 110	6B 6E	126 130	7E 82
(Field Gate)	Start 15 µs Stop 45 µs	189 566	BD 236	223 668	DF 29C
(VSYNC) This gives FIELD = 1, 0 for field one and two, respectively	8 µs	98	62	118	76

Figure 8. Bt261 Suggested Register Settings.

HSYNC Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the HSYNC output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set low. If [start value] = [stop value], HSYNC will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and HSYNC outputs. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, output of this signal with respect to CSYNC* may be delayed.

D4–D7 of HSYNC start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC start register is not updated until the write cycle to the HSYNC start high register. Thus, the writing sequence should be [HSYNC start low] [HSYNC start high].

D4–D7 of HSYNC stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC stop register is not updated until the write cycle to the HSYNC stop high register. Thus, the writing sequence should be [HSYNC stop low] [HSYNC stop high].

	HSYNC Start/Stop High				HSYNC Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

CLAMP Start and Stop Registers

These two 16-bit registers specify the horizontal count (in pixel clocks) at which to assert and negate the CLAMP output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set low. If [start value] = [stop value], CLAMP will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, output of this signal with respect to CSYNC* may be delayed.

D4–D7 of CLAMP start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP start register is not updated until the write cycle to the CLAMP start high register. Thus, the writing sequence should be [clamp start low] [clamp start high].

D4–D7 of CLAMP stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP stop register is not updated until the write cycle to the CLAMP stop high register. Thus, the writing sequence should be [clamp stop low] [clamp stop high].

	CLAMP Start/Stop High				CLAMP Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A value corresponding to 1 µs after the falling edge of CSYNC* is recommended for the [start] value, and a value of 1 µs before the rising edge of CSYNC* is recommended for the [stop] value if DC restoration is to occur during the horizontal sync interval. If DC restoration is to occur during the back porch interval, a value corresponding to 500 ns after the rising edge of CSYNC* is recommended for the [start] value and a value corresponding to 2.5 µs after the rising edge of CSYNC* is recommended for the [stop] value. For restoration of signals with subcarrier-encoded NTSC or PAL, the 7.8–9.4 µs interval (12–15 percent of HCOUNT) following the color burst may be better for clamping a luminance signal with residual burst.

ZERO Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the ZERO output. The [start value] sets this output high at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. The [stop value] sets this output low at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. If [start value] = [stop value], ZERO will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, output of this signal with respect to CSYNC* may be delayed.

D4–D7 of ZERO start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO start register is not updated until the write cycle to the ZERO start high register. Thus, the writing sequence should be [zero start low] [zero start high].

D4–D7 of ZERO stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO stop register is not updated until the write cycle to the ZERO stop high register. Thus, the writing sequence should be [zero stop low] [zero stop high].

	ZERO Start/Stop High				ZERO Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Since an active high signal is need for the Bt218, Bt252, and Bt254 during non-acquisition intervals, the ZERO output can be programmed to be within the horizontal retrace interval. In addition, these devices produce a significant impulse on their video input following the zero pulse, which can affect clamping stability. So, the pulse is best positioned within the active CLAMP pulse to divert this energy. Both CLAMP and ZERO pins may be driven with the same timing.

FIELD Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to start and stop the FIELD gate "window." With the noise gate properly programmed to ignore half-line vertical interval pulses, the VSYNC* transition will occur half a line later during the vertical sync interval between fields one and two (assuming a typical 2:1 interlaced video signal). By programming the FIELD start and stop values to have an interval exceeding half a line (e.g. starting at 1/4 line time and stopping at 3/4 line time), the FIELD output is low during field one if [start value] < [stop value] or high during field one if [start value] > [stop value], with transitions at every falling edge of VSYNC*. If [start value] = [stop value], FIELD will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. Field edge coincides with VSYNC* falling edge.

D4–D7 of FIELD gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate start register is not updated until the write cycle to the FIELD gate start high register. Thus, the writing sequence should be [field gate start low] [field gate start high].

D4–D7 of FIELD gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate stop register is not updated until the write cycle to the FIELD gate stop high register. Thus, the writing sequence should be [field gate stop low] [field gate stop high].

	FIELD Gate Start/Stop High				**FIELD Gate Start/Stop Low**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Values of one fourth HCOUNT and three fourths HCOUNT are recommended for start and stop values, resulting in an active high FIELD output (field one = 1, field two = 0).

Noise Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of CSYNC* at which to force the noise gate to be closed (start value) or open (stop value). If [start value] = [stop value], the noise gate will remain closed. The noise-gate start value should be activated no later than HCOUNT/2. The noise-gate stop value should be within one half the minimum serration pulse width minus 500 ns to the end of the horizontal line. This gating is required because of the state counter that is used to determine the phase comparison output and the 500 ns delay that is used for phase limiting. Because of this stop-value limitation, the digital noise gate can be used to track phase errors no greater than one half the minimum serration pulse width. This translates into 2.3 µs and 0.75 µs (3.6 percent and 1.2 percent of the line rate) for RS170A and RS343, respectively. For example:

Video Source	1/2 Minimum Serration Pulse	261 Gate Delay	Minimum Stop Value From End of Line	Minimum Noise-Gate Stop-Value Time
RS170A	2.3 µs	0.5 µs	1.8 µs	61.76 µs
RS343A	0.75 µs	0.5 µs	0.25 µs	63.31 µs

Note: The Brooktree *Applications Handbook* and the RS343A and RS170A specifications contain minimum serration pulse widths.

For wideband acquisition, the noise gate should be disabled by programming the start value greater and the stop value less than the number of pixels per line.

Values from $0000 (1) to $0FFF (4096) may be specified. This register should be initialized early to minimize indeterminate outputs during vertical retrace. This register must be properly programmed when the part is used in either phase-lock loop mode or when an external oscillator is resynchronized.

D4–D7 of noise gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit noise gate start register is not updated until the write cycle to the noise gate start high register. Thus, the writing sequence should be [noise gate start low] [noise gate start high].

D4–D7 of noise gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit noise gate stop register is not updated until the write cycle to the noise gate stop high register. Thus, the writing sequence should be [noise gate stop low] [noise gate stop high].

	Noise Gate Start/Stop High				Noise Gate Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Internal Registers *(continued)*

HCOUNT Register

This 16-bit register specifies the maximum number of pixel clocks to generate per horizontal line. In phase-locked applications, HCOUNT is the critical register that is resolution dependent. It should be programmed with the number of pixels per line required, minus 1. The other timing-dependent registers, including noise gate, ZERO, CLAMP, and HSYNC, will now all be programmed in terms of clock events, based upon the number of clocks per line defined in HCOUNT. For example, the HSYNC stop register is programmed to set output low at count zero, signifying the falling edge of HSYNC or the beginning of the line. The HSYNC start value is programmed to toggle high at 4.75 µs into the horizontal line, signifying the beginning of the back porch, for RS170A. The HSYNC start value in terms of a 12.27 MHz clock (square pixels NTSC) would be 59 clocks, or ~4.7 µs (see Figure 8).

The HCOUNT low and high registers are cascaded to form a 16-bit HCOUNT register. D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HCOUNT register is not updated until the write cycle to the HCOUNT high register. Thus, the writing sequence should be [HCOUNT low] [HCOUNT high]. Values from $0000 (1) to $0FFF (4096) may be specified. This register should be written first during initialization to minimize indeterminate output activity.

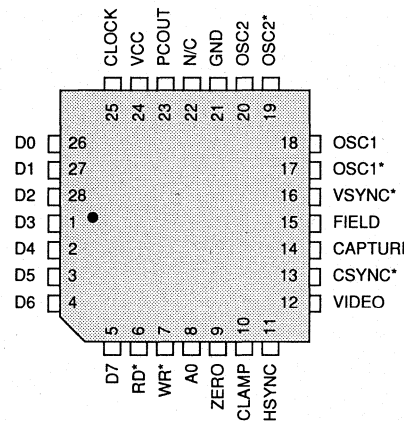
	HCOUNT High				HCOUNT Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Pin Descriptions

Pin Name	Description
HSYNC	Horizontal sync input/output (TTL compatible). As an output, HSYNC is programmed to be either a logical zero or logical one during the desired horizontal sync interval. It is output following the rising edge of CLOCK. As an input, it is input into the phase comparator asynchronously to the clocks with no pipeline delays.
VSYNC*	Vertical sync output (TTL compatible) with a negative composite sync output. VSYNC* is a logical zero for scan lines during detected vertical sync intervals on the VIDEO input. It is output following the rising edge of CLOCK.
CSYNC*	Composite sync output (TTL compatible). CSYNC* is a logical zero during negative composite sync intervals detected on the VIDEO input. It is output asynchronous to the clocks with no pipeline delays.
ZERO	Zero output (TTL compatible). This output is used to control the ZERO input of the image digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
CLAMP	Clamp output (TTL compatible). This output is used to control the CLAMP input of the image digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
FIELD	Even/odd field output (TTL compatible). For interlaced operation, this output (with transitions coincident with the VSYNC* output) indicates whether the current field is even or odd; the polarity is programmable. For noninterlaced operation, this output is always either a logical one or a logical zero, depending on whether it is programmed to be active high or low. It is output on the falling edge of VSYNC*.
PCOUT	Phase comparator output (TTL compatible). This three-state output indicates the phase difference in time between the generated horizontal sync signal (either the internally generated HSYNC or the HSYNC pin) and the recovered horizontal sync signal. High = lags, Low = leads.
VIDEO	Video and composite sync input. Either a DC-coupled TTL composite sync information or an AC-coupled analog video signal (less than 2 V peak-to-peak) may be input via this pin for detection of sync information. Sync information must be of negative polarity.
CLOCK	Pixel clock input/output (TTL compatible). The device may either drive this pin with a generated clock or an external pixel clock may drive this pin. When the CLOCK pin is externally driven, the selected OSC pin must also be driven.
OSC1, OSC1*, OSC2, OSC2*	External clock inputs (TTL or ECL compatible). These inputs are programmed to be either TTL or ECL compatible (10KH differential ECL driven by a single +5 V supply).
CAPTURE	Active video output (TTL compatible). This output is active high for a frame duration and is synchronized to the vertical sync interval and FIELD signal. It is output following the rising edge of FIELD for interlaced, or the falling edge of VSYNC* if non-interlaced.

Pin Descriptions *(continued)*

Pin Name	Description
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. If RD* is a logical one, D0–D7 are three-stated.
A0	Address control inputs (TTL compatible). A0 specifies whether the MPU is accessing the address register (A0 = 0) or the control register specified by the address register (A0 = 1).
VCC	Power.
GND	Ground.



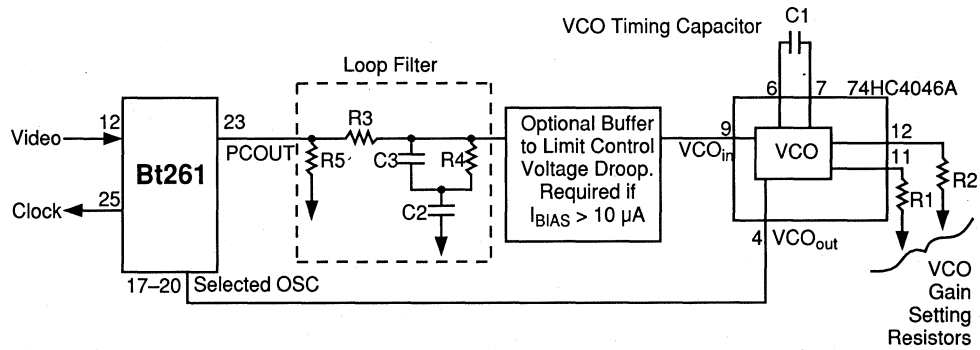
Phase Locking With the 74HC4046

Applications that call for multiple resolutions with clock rates in the 9–18 MHz range may employ the circuit (Figure 9) shown with a 74HC4046 and a passive loop filter. Residual jitter can be less than 30 ns, which is subpixel but not as good as can be achieved with LC-tuned VCOs or VCXOs. These have narrower tuning ranges. The loop parameters were obtained from a design program provided for the 74HC4046 with the Bt261's phase comparator emulating the type 2 phase detector with 4π/VCC gain (Note 1). The type 1 second-order loop is designed for 10 dB ripple suppression in closed-loop response with a critically damped response and a tracking range of 4 percent, which is adequate for most stable sources (e.g., broadcast, camera, and videodisc). Nonstandard video sources (e.g., heterodyne VCRs or floppy disk ESP cameras) may require a prefilter PLL for adequate tracking. Third-order loop filters may yield faster loop response rolloff, which reduces jitter but can prolong loop settling time.

Note 1: For further information, refer to the specific VCO datasheet or *Phase-Locked Loop Circuit Design* by Dan H. Wolaver, Prentice-Hall, 1991.

The same circuit can be extended to 26 MHz for genlocking to higher raster frequency sources (such as noninterlaced VGA) or adapted to crystal-based operation up to 10 MHz. The VCO timing-capacitor value must be reduced to 40 pF for the former higher frequency case or replaced with a parallel resonant crystal in the latter case. Loop filter values will vary slightly in conjunction with modification of R1 and R2 VCO gain-setting resistors.

In general, VCO capture range must be limited to one octave to prevent harmonic lockup. With the low-input bias current of the 74HC4046, passive filters are simpler than active filters and can better accommodate large-value polarized capacitors. Bipolar VC(X)O implementations that use the MC4024, 74LS624, or MN3106 require active buffers with bias currents less than 10 µA to limit control voltage droop across the 64 µs interval between phase-comparison pulses. Low-absorption Mylar or Teflon capacitors in the loop filter can minimize jitter caused by capacitance modulation.



Tracking Range	Oscillator Jitter	R_1	R_2	R_3	R_4	R_5	C_1	C_2	C_3	W_n	Damping (3)
9–18 MHz	<40 ns	3.9 kΩ	10 kΩ	470 Ω	86 Ω	500 kΩ	100 pF	10 µF	1 µF	290 Hz	0.74
17–26 MHz	<40 ns	3.9 kΩ	10 kΩ	470 Ω	86 Ω	500 kΩ	40 pF	10 µF	1 µF	290 Hz	0.74
±200 ppm of crystal center frequency	<10 ns	46 kΩ	46 kΩ	470 Ω	290 Ω	500 kΩ	≤10 MHz Resonant Crystal	3.3 nF	300 pF	290 Hz	0.74

Figure 9. Operation of the Bt261 with the 74HC4046A.

Application Information *(continued)*

Interfacing to the Bt218

Figure 10 illustrates the interface of the Bt261 to the Bt218 Flash A/D Converter. The VIDEO input of the Bt261 connects to the VIN input of the Bt218 through a 0.1 µF ceramic capacitor. The sync slicing level of the Bt261 should be selected for optimum performance.

The Bt261 provides the ZERO and CLAMP signals required by the Bt218, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

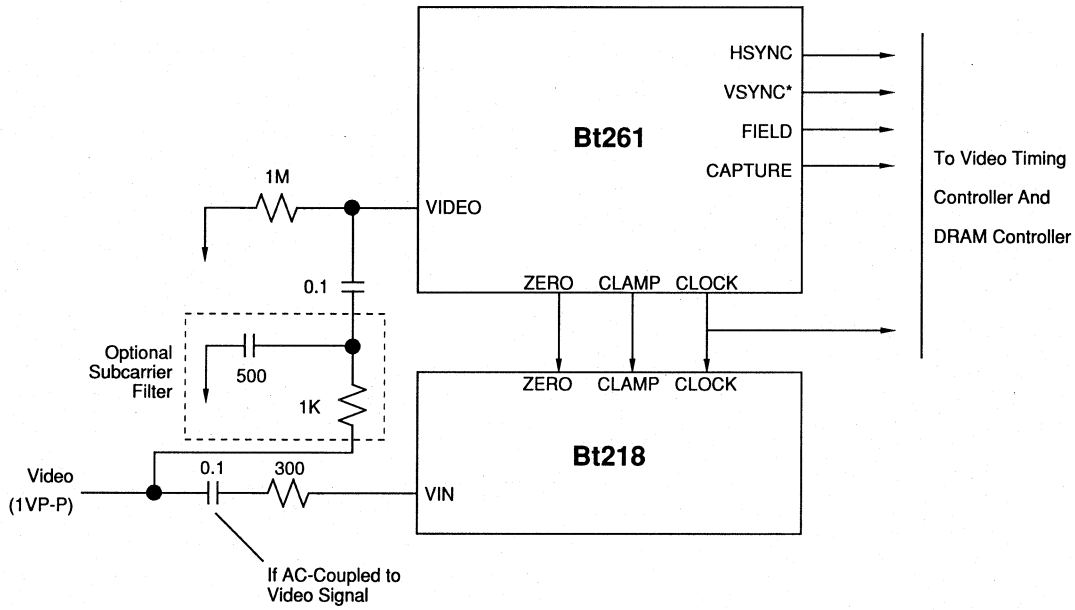


Figure 10. Interfacing to the Bt218.

Interfacing to the Bt252

Figure 11 illustrates the interface of the Bt261 to the Bt252 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt252. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt252, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

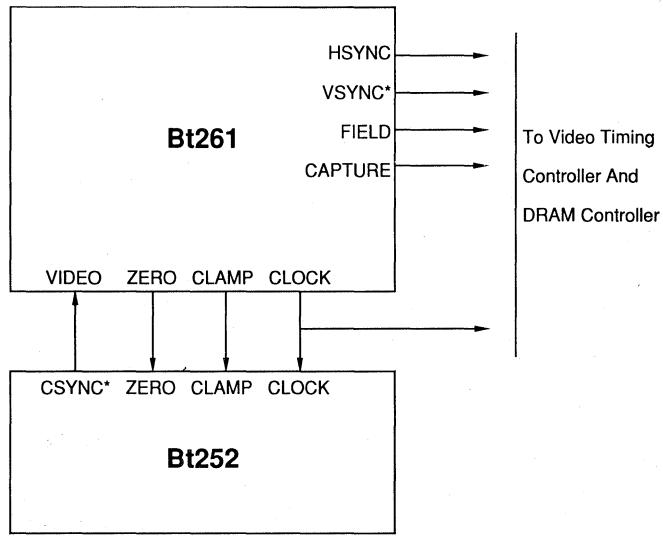


Figure 11. Interfacing to the Bt252.

Application Information *(continued)*

Interfacing to the Bt254

Figure 12 illustrates the interface of the Bt261 to the Bt254 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt254. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt254, in addition to the (R,G,B) CLOCK inputs of the Bt254.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

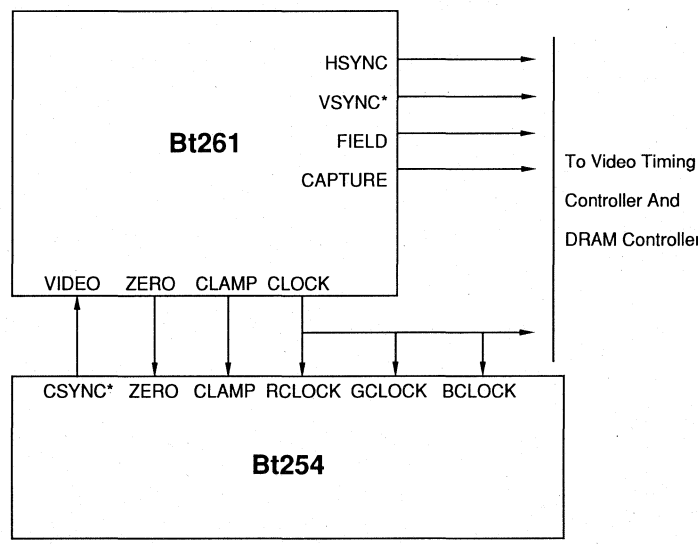


Figure 12. Interfacing to the Bt254.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Video Input					
DC-coupled				5	V
AC-coupled (Note 1)		0.2		2	V_{pp}

Note 1: Video input DC quiescent about (VCC/2) volts.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VCC + 0.5	V
Ambient Operating Temperature	TA	–55		+ 125	°C
Storage Temperature	TS	–65		+ 150	°C
Junction Temperature	TJ			+ 150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input High Voltage (Note 1) HSYNC Pin	VIH	2.2		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input Low Voltage (Note 1) RD* Pin	VIL			0.4	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Low Current (Vin = 0.4 V) VIDEO Pin	IIL			–1.5	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
OSC Digital Inputs					
TTL Mode					
Input High Voltage (Note 1)	VIH	2.2		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
ECL Mode					
Input High Voltage	VIH	VCC–1.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		VCC–1.6	V
Input High Current (Vin = 4.0 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
D0 - D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			0.5	µA
Output Capacitance	COUT		20		pF
PCOUT Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			400	nA
Output Capacitance	COUT		20		pF
Other Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			0.5	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: VIH, VIL for RD*, HSYNC, and OSC inputs are tested at 3 and 0 V but guaranteed by characterization.

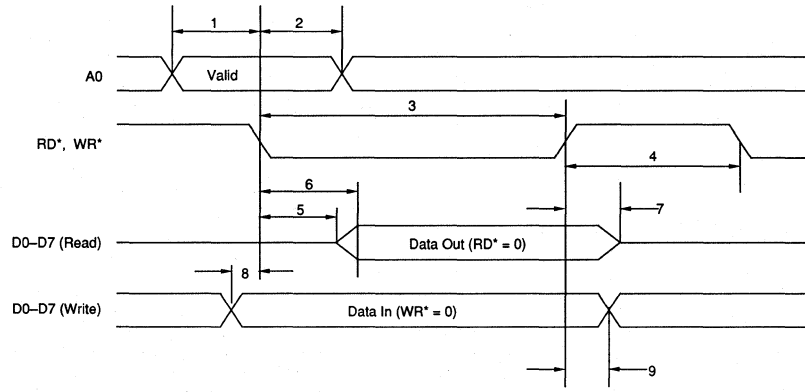
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC Cycle Time	OSCmax				ns
TTL mode		13.3			ns
ECL mode		12.5			ns
CLOCK Cycle Time (Note 1)	Fmax	33.33			ns
A0 Setup Time	1	10			ns
A0 Hold Time	2	10			ns
RD*/WR* Low Time	3	40			ns
RD*/WR* High Time	4	40			ns
RD* Asserted to Data Bus Driven	5	1			ns
RD* Asserted to Data Valid	6			30	ns
RD* Negated to Data Bus 3-Stated	7			30	ns
Write Data Setup Time	8	10			ns
Write Data Hold Time	9	10			ns
OSC High Time	10	6			ns
OSC Low Time	11	6			ns
OSC to CLOCK Output Delay	14			35	ns
VIDEO to CSYNC* Output Delay	15			35	ns
HSYNC, ZERO, CLAMP Output Delay	16			10	ns
VSYNC*, FIELD Output Delay	17			10	ns
PCOUT Output Delay	18	380		650	ns
Minimum Compare Differential	19		5	13	ns
VCC Supply Current (Note 2)	ICC		60	90	mA

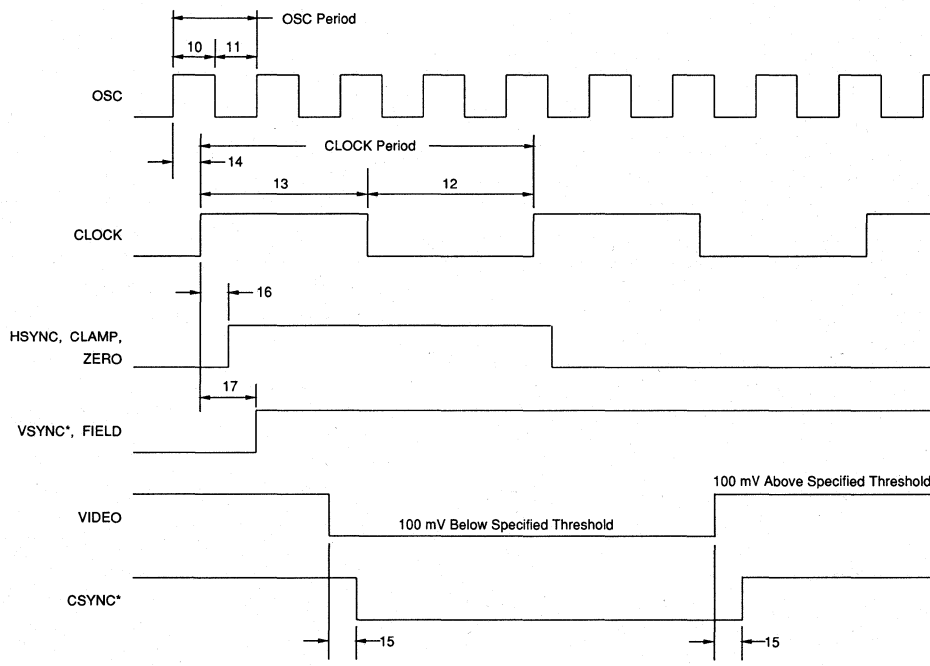
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50-percent for inputs and outputs. CLOCK, HSYNC, CLAMP, ZERO, VSYNC*, FIELD, CAPTURE, and CSYNC* output load ≤ 50 pF, D0–D7 output load ≤ 130 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Maximum load of 20 pf.
Note 2: At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC = 5.25 V. OSC/PCLOCK = 2, CLOCK/HSYNC ≥100.

Timing Waveforms

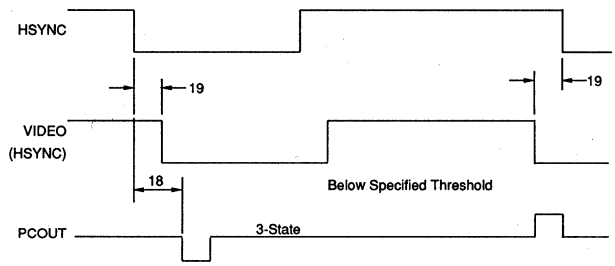


MPU Read/Write Timing.



Video Input/Output Timing.

Timing Waveforms *(continued)*



Video Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt261KPJ	28-pin Plastic J-Lead	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt281

27 MHz Programmable Color Space Converter and Color Corrector

3

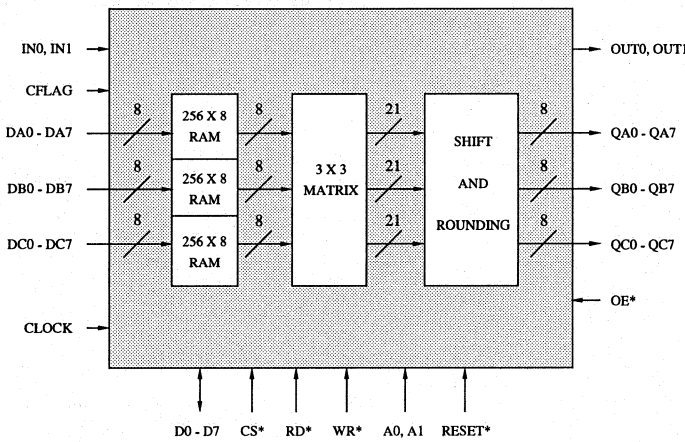
Distinguishing Features

- Real-Time Color Space Conversion
- Pseudo-Color Mode
- Programmable Matrix Coefficients
- Three 256 x 8 Input Lookup Table RAMs
- Standard MPU Interface
- TTL Compatibility
- +5 V Monolithic CMOS
- 84-pin PLCC Package
- Typical Power Dissipation: 1.1 W

Applications

- Image Processing
- Image Capture
- Color Correction

Functional Block Diagram



Product Description

The Bt281 Color Space Converter is designed specifically for image capture and processing applications. It provides real-time conversion of the color space during the image capture process or during the CRT display process. Thus, the color space of the frame buffer may be optimized for image processing applications regardless of the type of video signal being digitized or the requirement that RGB information be generated to drive the CRT.

Twenty-four bits of color information are input with the DAx, DBx, and DCx inputs; converted to a new color space by the 3 x 3 matrix multiplier; and output onto QAx, QBx, and QCx.

Three independent 256 x 8 input lookup tables enable the addition or removal of gamma correction or gain control prior to conversion to another color space.

The QAx, QBx, and QCx outputs may be three-stated asynchronously to CLOCK with the OE* control input.

Two sets of matching delay lines are included to maintain synchronization of control signals.

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L281001 Rev. G

Brooktree®

Circuit Description

MPU Interface

As shown in the functional block diagram and in Figure 1, the Bt281 supports a standard MPU interface (D0–D7, CS*, RD*, WR*, A0, and A1). MPU operations are asynchronous to clock.

A0 and A1 are used to select address register, RAM location, or control register specified by the address register, as indicated in Table 1. The 11-bit address register specifies which control register or RAM location the MPU is accessing, as listed in Table 1. The address register resets to $000 following a read or write cycle to location $7FF. Write cycles to reserved addresses are ignored, and read cycles from reserved addresses return invalid data. ADDR11–ADDR15 are always logical zeros.

The address register increments after each MPU read or write cycle and is not initialized. ADDR0 and ADDR8 correspond to data bus bit D0, and ADDR0 is the least significant bit. The address register is not initialized following a reset or power-up condition.

The lookup table RAMs are not dual ported, so MPU accesses have priority over pixel accesses. During MPU access to the color palette RAMs, the QAx, QBx, and QCx outputs are undefined and invalid. Thus, lookup table updates should occur only during blanking intervals.

Matrix Multiplier

DA0–DA7, DB0–DB7, and DC0–DC7 are latched on the rising edge of CLOCK and address the three color lookup table RAMs. The outputs of the RAMs are input to the 3 x 3 matrix multiplier.

The 3 x 3 matrix multiplier performs the fundamental color space conversion as follows:

$$\begin{bmatrix} QA \\ QB \\ QC \end{bmatrix} = \begin{bmatrix} m1 & m2 & m3 \\ m4 & m5 & m6 \\ m7 & m8 & m9 \end{bmatrix} \begin{bmatrix} DA \\ DB \\ DC \end{bmatrix}$$

The MPU loads m1–m9 to perform the color space conversion desired. The values of m1–m9 are programmable over the range of –4.000 to +3.996 when 2's complement notation is used.

The 3 x 3 matrix multiplier generates three 21-bit (including sign) values (one for each of the three channels). As only 8 bits per channel may be output, command bits CR17–CR15 are used to select which 8 bits (or 7 bits + sign) of these 21 bits are output, as specified in Table 2.

The fractional data indicated in Table 2 is used to round to 8 bits as follows: The number should be rounded up if the fractional data = 0.5 and the rounded result will be an even number (LSB = 0), or if the fractional data is > 0.5. If the fractional data is < 0.5, the number should be rounded down. Circuitry is included to avoid wrapping around on overflow or underflow conditions; rather, the data is saturated at the minimum and maximum allowable values.

QA0–QA7, QB0–QB7, and QC0–QC7 are output following the rising edge of CLOCK.

The QAx, QBx, and QCx outputs may be three-stated asynchronously to the output clock with the OE* control input and command bit CR10.

Bypassing

The Bt281 may be entirely bypassed with no change in the pipeline delay through the command register. Following a reset condition, the Bt281 is initialized to be in the bypass mode. For further information, see the Timing Waveforms section.

I/O Delay Lines

The IN0 and IN1 inputs are latched on the rising edge of CLOCK, pipelined to maintain synchronization with the color data, and output onto OUT0 and OUT1.

The delay lines may be used for control signals, such as sync and blank. They should have the same pipeline delay as the pixel data.

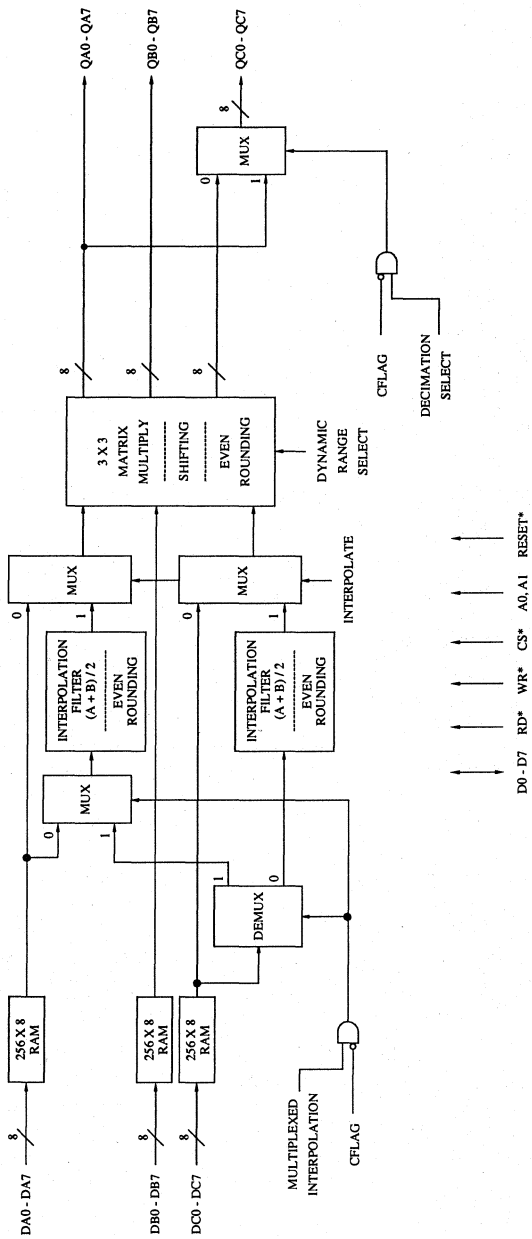


Figure 1. Detailed Block Diagram.

A1, A0	ADDR0–ADDR10	Accessed by MPU
00	$xxx	address register low (ADDR0–ADDR7)
01	$xxx	address register high (ADDR8–ADDR10)
10	$000	DA RAM location $00
10	$001	DA RAM location $01
:	:	:
10	$0FF	DA RAM location $FF
10	$100	DB RAM location $00
10	$101	DB RAM location $01
:	:	:
10	$1FF	DB RAM location $FF
10	$200	DC RAM location $00
10	$201	DC RAM location $01
:	:	:
10	$2FF	DC RAM location $FF
10	$300	m1 register low
10	$301	m1 register high
10	$302	m2 register low
10	$303	m2 register high
10	$304	m3 register low
10	$305	m3 register high
10	$306	m4 register low
10	$307	m4 register high
10	$308	m5 register low
10	$309	m5 register high
10	$30A	m6 register low
10	$30B	m6 register high
10	$30C	m7 register low
10	$30D	m7 register high
10	$30E	m8 register low
10	$30F	m8 register high
10	$310	m9 register low
10	$311	m9 register high
10	$312	command register_0
10	$313	command register_1
10	$314	reserved
:	:	:
10	$7FF	reserved
11	$xxx	reserved

Table 1. Control Register Addressing.

Circuit Description *(continued)*

Matrix Multiplication Operation

8-bit pixel input: DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0
11-bit coefficient: C10 C9 C8 . C7 C6 C5 C4 C3 C2 C1 C0

19-bit total: S T17 T16 T15 T14 T13 T12 T11 T10 T9 T8 . T7 T6 T5 T4 T3 T2 T1 T0

Three of these 19-bit totals (since there are three coefficients per channel) must be added together, resulting in 21 bits per channel (S = sign bit):

S R19 R18 R17 R16 R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0

CR17–CR15	QA7	QA6	QA5	QA4	QA3	QA2	QA1	QA0	Used for Rounding
unsigned magnitude format									
100	R19	R18	R17	R16	R15	R14	R13	R12	R11–R0
011	R18	R17	R16	R15	R14	R13	R12	R11	R10–R0
010	R17	R16	R15	R14	R13	R12	R11	R10	R9–R0
001	R16	R15	R14	R13	R12	R11	R10	R9	R8–R0
000	R15	R14	R13	R12	R11	R10	R9	R8	R7–R0
other two formats									
100	S	R18	R17	R16	R15	R14	R13	R12	R11–R0
011	S	R17	R16	R15	R14	R13	R12	R11	R10–R0
010	S	R16	R15	R14	R13	R12	R11	R10	R9–R0
001	S	R15	R14	R13	R12	R11	R10	R9	R8–R0
000	S	R14	R13	R12	R11	R10	R9	R8	R7–R0

Table 2. Example Dynamic Output Range Selections (QAx Channel).

Circuit Description *(continued)*

Number Representations

The Bt281 accommodates analog sign magnitude, unsigned magnitude, and 2's complement formats to ease interface to A/D and D/A converters, frame buffers, and processing circuits. (See Table 3.)

Offset Binary Representation

Only the DAx and DCx inputs, and the QAx and QCx outputs can be configured for this representation of processing color difference signals (Cr/Cb, I/Q, U/V, R-Y/B-Y, etc.). The DBx inputs and QBx outputs are always configured for 8-bit unsigned magnitude representation (0–255) for luminance processing.

Offset binary representation should be used if A/D converters drive the DAx and DCx inputs (with the A/D midscale corresponding to zero).

Offset binary representation should be used at the output if the QAx and QCx outputs drive D/A converters (with the D/A midscale corresponding to zero).

2's Complement Representation

Frame buffers and image processors commonly use 2's complement representation to simplify sign-bit handling.

Only the DAx and DCx inputs, and the QAx and QCx outputs can be configured for this representation of processing color difference signals (Cr/Cb, I/Q, U/V, R-Y/B-Y, etc.). The DBx inputs and QBx outputs are always configured for 8-bit unsigned magnitude representation (0–255) for luminance processing.

If a frame buffer is driving the DAx and DCx inputs, 2's complement may be used at the input to ease interface to other image processing circuitry. If the QAx and QCx inputs are interfaced to a frame buffer, 2's complement may be used at the output to ease interface to image processing circuitry.

Unsigned Magnitude Representation

This 0–255 range input/output format is used when the Bt281 is inputting or outputting RGB video signals.

	Offset Binary Representation		2's Complement Representation		Unsigned Magnitude Representation	
DAx, DCx, QAx, QCx	DA7–DA0, DC7–DC0	Number Represented	DA7–DA0, DC7–DC0	Number Represented	DA7–DA0, DC7–DC0	Number Represented
$FF	1111 1111	+127	1111 1111	–1	1111 1111	255
$FE	1111 1110	+126	1111 1110	–2	1111 1110	254
:	:	:	:	:	:	:
$81	1000 0001	+1	1000 0001	–127	1000 0001	129
$80	1000 0000	0	1000 0000	–128	1000 0000	128
$7F	0111 1111	–1	0111 1111	+127	0111 1111	127
:	:	:	:	:	:	:
$01	0000 0001	–127	0000 0001	+1	0000 0001	1
$00	0000 0000	–128	0000 0000	0	0000 0000	0

Table 3. Numbering Representations.

Circuit Description *(continued)*

Input Interpolation Circuitry

The Bt281 may be configured to input 8 bits of luminance on the DBx inputs and 8 bits of multiplexed color difference signals on the DCx inputs. The multiplexed color difference signals are demultiplexed, and the missing values are interpolated with linear interpolation filters. The resultant 24 bits of luminance and color difference data are input to the 3 x 3 matrix multiplier for processing. For further information, see the Timing Waveforms section. The DAx inputs are ignored. Figure 2 illustrates the input interpolation circuitry.

With YCrCb processing, and with Y input via the DBx inputs and multiplexed Cr/Cb input via the DCx inputs,

The 16-bit input sequence is:

DBx =	Y (n)	Y (n + 1)	Y (n + 2)	Y (n + 3)
DCx =	Cb (n)	Cr (n)	Cb (n + 2)	Cr (n + 2)

The 24-bit output after the interpolation filters is:

DBx '=	Y (n)	Y (n + 1)	Y (n + 2)	Y (n + 3)
DCx '=	Cb (n)	Cb (n + 1)	Cb (n + 2)	Cb (n + 3)
DAx '=	Cr (n)	Cr (n + 1)	Cr (n + 2)	Cr (n + 3)

The CFLAG input indicates whether the multiplexed DCx inputs contain Cb (CFLAG = 1) or Cr (CFLAG = 0) information. The demultiplexer, controlled by CFLAG, demultiplexes the Cr and Cb information. Alternately, nonmultiplexed color difference signals may be input with the DAx and DCx inputs, at a data rate of one half the DBx inputs (see Figure 11 in the Timing Waveforms section). The interpolation filter generates the missing values by averaging successive data points.

With YCrCb processing, and with Y input via the DBx inputs, Cr input via the DAx inputs, and Cb input via the DCx inputs,

The 24-bit input sequence is:

DAx =	Cr (n)	Cr (n)	Cr (n + 2)	Cr (n + 2)
DBx =	Y (n)	Y (n + 1)	Y (n + 2)	Y (n + 3)
DCx =	Cb (n)	Cb (n)	Cb (n + 2)	Cb (n + 2)

The 24-bit output after the interpolation filters is:

DBx '=	Y (n)	Y (n + 1)	Y (n + 2)	Y (n + 3)
DCx' =	Cb (n)	Cb (n + 1)	Cb (n + 2)	Cb (n + 3)
DAx' =	Cr (n)	Cr (n + 1)	Cr (n + 2)	Cr (n + 3)

In either case, the DBx inputs are configured for an unsigned magnitude representation, while the DAx and DCx inputs are configured for either offset binary or 2's complement numbering representation.

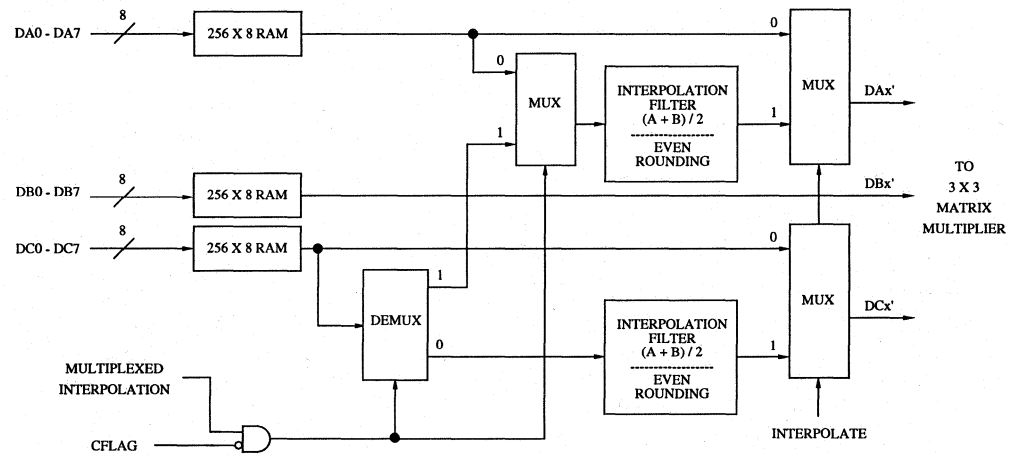


Figure 2. Input Interpolation Circuitry.

Circuit Description *(continued)*

The output of the interpolation filters is 9 bits (including sign). The output is rounded to 8 bits as follows: The number should be rounded up if the fractional data = 0.5 and the result will round to an even number (LSB = 0), or if the fractional data is > 0.5. If the fractional data is < 0.5, the number should be rounded down.

Output Decimation Circuitry

The Bt281 may be configured to output 8 bits of luminance on the QBx outputs and 8 bits of multiplexed color difference signals on the QCx outputs. The color difference signals from the matrix multiplier are decimated and multiplexed onto the QCx outputs. For further information, see the Timing Waveforms section.

The QBx outputs are configured for an unsigned magnitude representation, while the QAx and QCx outputs are configured for either offset binary or 2's complement representation.

The CFLAG input is used to specify whether Cr or Cb data is to be output onto the QCx bus. If CFLAG is a logical zero, Cb data is output during the next clock cycle. If CFLAG is a logical one, Cr data is output during the next clock cycle. This timing enables the CFLAG status to match the data present on the QCx outputs.

The multiplexer decimates by removing every other sample of color information.

Figure 3 illustrates the output decimation circuitry.

With YCrCb processing, and with Y output via the QBx outputs and multiplexed CrCb output via the QCx outputs,

The 24-bit input to the decimation circuit is:

QAx' =	Cr (n)	Cr (n + 1)	Cr (n + 2)	Cr (n + 3)
QBx' =	Y (n)	Y (n + 1)	Y (n + 2)	Y (n + 3)
QCx' =	Cb (n)	Cb (n + 1)	Cb (n + 2)	Cb (n + 3)

The output sequence is:

QBx =	Y (n)	Y (n + 1)	Y (n + 2)	Y (n + 3)
QCx =	Cb (n)	Cr (n)	Cb (n + 2)	Cr (n + 2)
QAx =	Cr (n)	Cr (n + 1)	Cr (n + 2)	Cr (n + 3)

The QAx outputs contain normal output data.

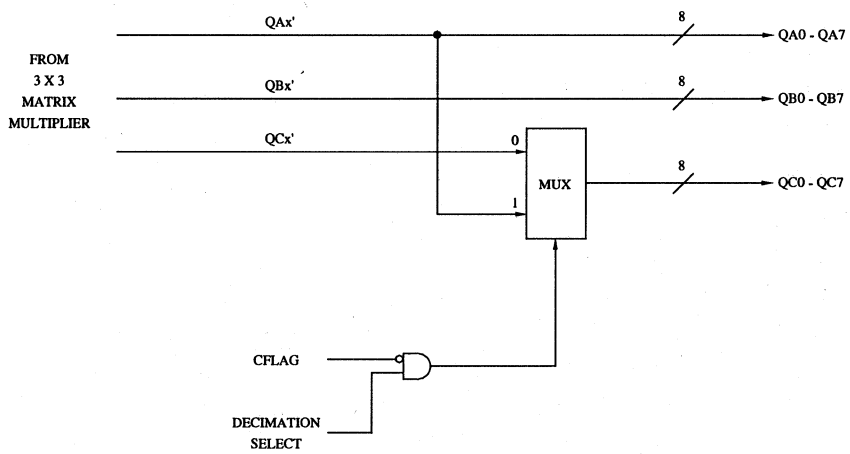


Figure 3. Output Decimation Circuitry.

Circuit Description *(continued)*

Typical Applications

Figure 4 shows two common applications of the Bt281. Figure 4a shows the Bt281 used when the color space of the analog video signal to be digitized may be one of several formats. The Bt281 ensures that the video data is converted into the color space of the frame buffer.

In Figure 4b, the Bt281 is used to convert a frame buffer that is using a color space other than RGB (e.g., YIQ or YUV) into the RGB color space to drive the CRT display.

The Bt281 enables these color space transformations to take place in real time, simplifying the system design.

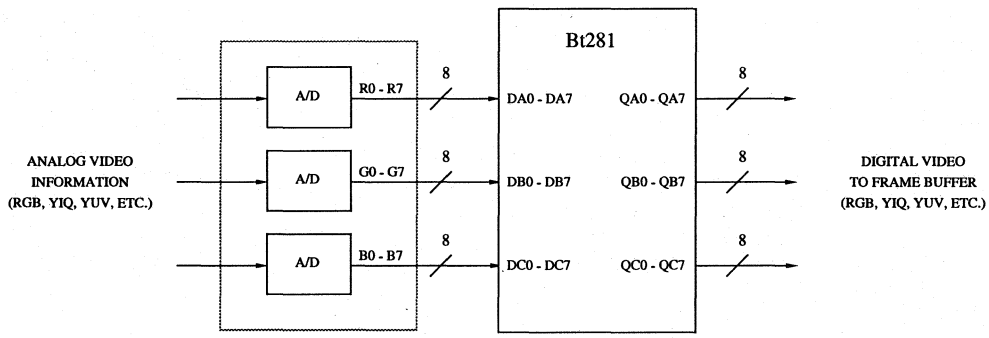


Figure 4a. Typical Application.

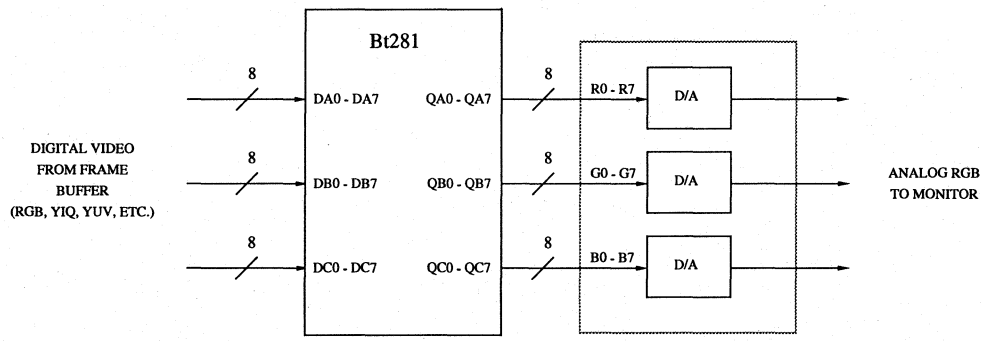


Figure 4b. Typical Application.

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR00 is the least significant bit and corresponds to data bus bit D0. The pipeline delay is constant regardless of the input/output configuration.

CR07–CR05 DAx, DCx input format select

(000) unsigned magnitude (nonmultiplexed, no interpolation)
(001) offset binary (nonmultiplexed, no interpolation)
(010) offset binary (nonmultiplexed, interpolated)
(011) offset binary (multiplexed, interpolated)

(100) 2's complement (nonmultiplexed, no interpolation)
(101) 2's complement (nonmultiplexed, interpolated)
(110) 2's complement (multiplexed, interpolated)
(111) pseudo-color mode (unsigned magnitude, nonmultiplexed, no interpolation)

These bits are ignored in bypass mode. They specify the input format and range for the DAx and DCx inputs. The DBx inputs are configured for unsigned magnitude operation.

If pseudo-color mode is selected, the DBx inputs address all three lookup table RAMs simultaneously, generating 24 bits of color information. The DAx and DCx inputs are ignored.

CR04–CR02 QAx, QCx output format select

(000) unsigned magnitude (nonmultiplexed, no decimation)
(001) offset binary (nonmultiplexed, no decimation)
(010) offset binary (multiplexed, decimated)
(011) reserved

(100) 2's complement (nonmultiplexed, no decimation)
(101) 2's complement (multiplexed, decimated)
(110) reserved
(111) reserved

CR01 These bits specify the output format and range for the QAx and QCx outputs. The QBx outputs are always configured for unsigned magnitude operation. These bits are ignored in bypass mode.

Error flag

(0) reset by MPU
(1) set by device

This bit is set by the device if a negative number is detected on the QAx, QBx, or QCx outputs while they are outputting an unsigned magnitude number (which should always be positive). To reset the bit to a logical zero, the MPU must write a logical zero to this bit. The error flag may be set if the MPU accesses the lookup table RAMs or while the command registers are being programmed if the operating mode is changed.

Internal Registers *(continued)*

Command Register_0 (continued)

CR00 Overflow/underflow error flag

(0) reset by MPU
(1) set by device

This bit is set by the device if an overflow or underflow condition is detected on the 3 x 3 matrix multiplier outputs (prior to the saturation circuitry). To reset the bit to a logical zero, the MPU must write a logical zero to this bit. The overflow/underflow flag may be set if the MPU accesses the lookup table RAMs or while the command registers are being programmed if the operating mode is changed.

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to $E1 following a reset sequence. CR10 is the least significant bit and corresponds to data bus bit D0. The pipeline delay is constant regardless of the input/output configuration.

CR17–CR15 Matrix dynamic output range select

(000) R8–R15 for unsigned magnitude output format; R9–R14 + sign for other formats
(001) R9–R16 for unsigned magnitude output format; R10–R15 + sign for other formats
(010) R10–R17 for unsigned magnitude output format; R11–R16 + sign for other formats
(011) R11–R18 for unsigned magnitude output format; R12–R17 + sign for other formats
(100) R12–R19 for unsigned magnitude output format; R13–R18 + sign for other formats
(101) reserved
(110) reserved
(111) bypass device

Mode (111) specifies that the entire device must be bypassed with no change in pipeline delay. (See Table 2.)

CR14–CR11 reserved

CR10 QAx, QBx, QCx output disable

(0) enable QAx, QBx, and QCx outputs
(1) disable QAx, QBx, and QCx outputs

This bit is logically gated with the OE* input pin, and the resulting value is used to control three-state of the QAx, QBx, and QCx outputs.

Internal Registers *(continued)*

m1–m9 Low/High Registers

For the m1–m9 values, the 8-bit low and high registers are cascaded to form an 11-bit register. D0–D7 comprise the low register, while D8–D10 comprise the high register. (D8 corresponds to data bus bit D0.) D3–D7 of m1–m9 high registers are always logical zeros.

The m1–m9 low/high registers may be written to or read by the MPU at any time and are not initialized following a reset sequence. D0 is the least significant bit.

These registers specify the matrix operators from –4.000 to +3.996 (using 2's complement notation) as follows:

D10–D0	Value
111 . 1111 1111	–0.004
111 . 1111 1110	–0.008
:	:
100 . 0000 0001	–3.996
100 . 0000 0000	–4.000
011 . 1111 1111	+3.996
:	:
000 . 0000 0001	+0.004
000 . 0000 0000	+0.000

Pin Descriptions

Pin Name	Description
DA0–DA7, DB0–DB7, DC0–DC7	Color inputs (TTL compatible). These inputs are latched on the rising edge of CLOCK. DA0, DB0, and DC0 are the least significant bits.
QA0–QA7, QB0–QB7, QC0–QC7	Color outputs (TTL compatible). These signals are output following the rising edge of CLOCK. QA0, QB0, and QC0 are the least significant bits.
IN0, IN1, OUT0, OUT1	Input/output delay line (TTL compatible). IN0 and IN1 are latched on the rising edge of CLOCK, pipelined to maintain synchronization with the color data, and output onto OUT0 and OUT1 following the rising edge of CLOCK.
CFLAG	Multiplex control input (TTL compatible). If the DAx/DCx inputs are multiplexed, CFLAG indicates when DCx data is present (CFLAG = 1). If the QAx/QCx outputs are multiplexed, CFLAG indicates when QCx data is to be output (CFLAG = 1). CFLAG is latched on the rising edge of CLOCK. This input is ignored when in the bypass mode.
OE*	Output enable control input (TTL compatible). This input is logically gated with command bit CR10, and the result controls three-state of the QAx, QBx, and QCx outputs. OUT0 and OUT1 are not three-statable.

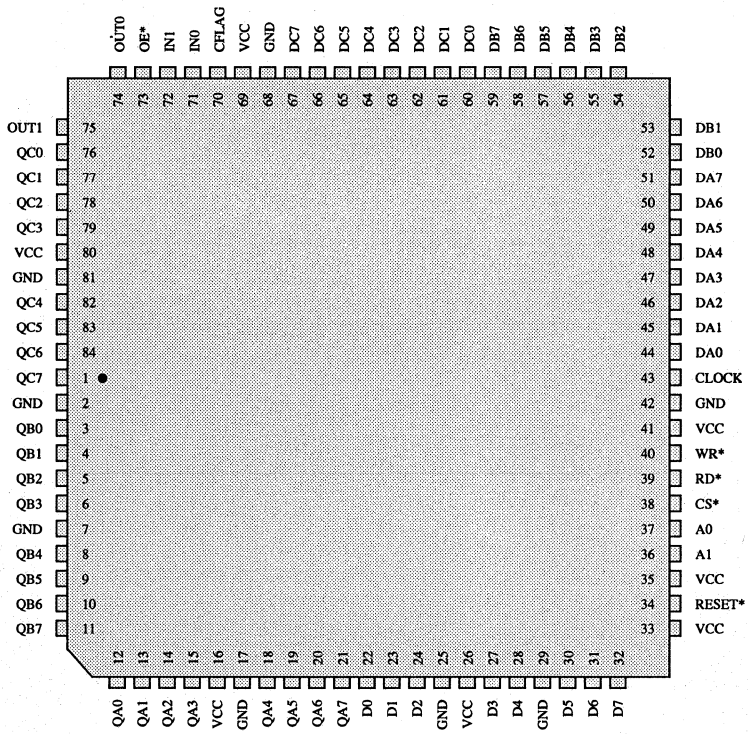
CR10	OE*	QAx, QBx, QCx Outputs
0	0	enabled
0	1	three-stated
1	0	three-stated
1	1	three-stated

CLOCK	Clock input (TTL compatible).
D0–D7	Bidirectional MPU data bus (TTL compatible). MPU data is input to and output from the device with this 8-bit data bus. D0 is the least significant bit.
CS*	Chip select control input (TTL compatible). CS* is latched on the falling edge of either RD* or WR*. An internally latched logical zero enables data to be written to or read from the device by the MPU. CS* should be connected to GND if not used.
RD*	Read control input (TTL compatible). A logical zero enables the MPU to read data from the device. Both RD* and WR* should not be asserted simultaneously. For further information, see the Timing Waveforms section.
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*. Both RD* and WR* should not be asserted simultaneously. For further information, see the Timing Waveforms section.

Latched CS*	RD*	WR*	MPU Operation
0	0	0	invalid operation
0	0	1	read data onto D0–D7
0	1	0	write D0–D7 data
0	1	1	D0–D7 three-stated
1	x	x	D0–D7 three-stated

Pin Descriptions *(continued)*

Pin Name	Description
A0, A1	Register select inputs (TTL compatible). A0 and A1 are latched on the falling edge of either RD* or WR*.
RESET*	Reset control input (TTL compatible). RESET* must be a logical zero for a minimum of three consecutive clock cycles to reset the device. RESET* must be a logical one for normal operation.
$\overline{VCC}$	Power. All $\overline{VCC}$ pins must be connected together.
GND	Ground. All GND pins must be connected together.



RGB-to-Y, R-Y, B-Y Conversion

The matrix for converting analog RGB to Y, R-Y, B-Y is as follows. The RGB inputs are normalized to have a range of 0–1 and are gamma-corrected RGB data.

$$\begin{bmatrix} Y \\ R-Y \\ B-Y \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.701 & -0.587 & -0.114 \\ -0.299 & -0.587 & 0.886 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The analog (R – Y) and (B – Y) terms have an output range of ±0.701 and ±0.886, respectively, while Y has a range of 0–1.

The conversion of digital RGB to normalized digital Y, (R – Y)', (B – Y)' (' indicating normalized notation) is slightly different in order to compress the (R – Y)' and (B – Y)' output range to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = R_0–R_7
DB0–DB7 = G_0–G_7
DC0–DC7 = B_0–B_7

QA0–QA7 = $(R-Y)'_0$–$(R-Y)'_7$
QB0–QB7 = Y_0–Y_7
QC0–QC7 = $(B-Y)'_0$–$(B-Y)'_7$

The RGB inputs to the matrix can have a range of 0–255; the lookup table RAMs on the Bt281 may be used to gamma correct the RGB data if necessary. The Y output of the matrix can have a range of 0–255, while the (R – Y)' and (B – Y)' outputs can have a range of –128 to +127. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} Y \\ (R-Y)' \\ (B-Y)' \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.500 & -0.419 & -0.081 \\ -0.169 & -0.331 & 0.500 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} (R-Y)' \\ Y \\ (B-Y)' \end{bmatrix} = \begin{bmatrix} \$0.80 & \$7.95 & \$7.EC \\ \$0.4C & \$0.96 & \$0.1D \\ \$7.D5 & \$7.AC & \$0.80 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the DAx and DCx inputs, and either offset binary or 2's complement representation for the QAx and QCx outputs. Command bits CR17–CR15 should be 000.

Application Information *(continued)*

RGB-to-YUV Conversion

The matrix for converting analog RGB to YUV is as follows. The RGB inputs are normalized to have a range of 0–1 and are gamma-corrected RGB data.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.147 & -0.289 & 0.436 \\ 0.615 & -0.515 & -0.100 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The analog U and V terms have an output range of ±0.436 and ±0.615, respectively, while Y has a range of 0–1.

U and V may also be defined as:

$$U = (B - Y) / 2.03 = 0.4926(B - Y)$$

$$V = (R - Y) / 1.14 = 0.8772(R - Y)$$

The conversion of digital RGB to normalized digital YU'V' (' indicating normalized notation) is slightly different in order to compress the V' output range to ±0.5 and to expand the U' output range to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = R_0–R_7
DB0–DB7 = G_0–G_7
DC0–DC7 = B_0–B_7

QA0–QA7 = V'_0–V'_7
QB0–QB7 = Y_0–Y_7
QC0–QC7 = U'_0–U'_7

The RGB inputs to the matrix can have a range of 0–255; the lookup table RAMs on the Bt281 may be used to gamma correct the RGB data if necessary. The Y output of the matrix can have a range of 0–255, while the U' and V' outputs can have a range of –128 to +127. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} Y \\ U' \\ V' \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.169 & -0.331 & 0.500 \\ 0.500 & -0.419 & -0.081 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping:

$$\begin{bmatrix} V' \\ Y \\ U' \end{bmatrix} = \begin{bmatrix} \$0.80 & \$7.95 & \$7.EC \\ \$0.4C & \$0.96 & \$0.1D \\ \$7.D5 & \$7.AC & \$0.80 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the DAx and DCx inputs, and either offset binary or 2's complement representation for the QAx and QCx outputs. Command bits CR17–CR15 should be 000.

Application Information *(continued)*

RGB-to-YIQ Conversion

The matrix for converting analog RGB to YIQ is as follows. The RGB inputs are normalized to have a range of 0–1 and are gamma-corrected RGB data.

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.596 & -0.275 & -0.321 \\ 0.212 & -0.523 & 0.311 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The analog I and Q terms have an output range of ±0.596 and ±0.525, respectively, while Y has a range of 0–1.

I and Q may also be defined as follows:

$$I = V\cos 33^\circ - U\sin 33^\circ$$

$$Q = V\sin 33^\circ + U\cos 33^\circ$$

or

$$I = 0.839V - 0.545U$$

$$Q = 0.545V + 0.839U$$

or

$$I = 0.736(R - Y) - 0.268(B - Y)$$

$$Q = 0.478(R - Y) + 0.413(B - Y)$$

The conversion of digital RGB to normalized digital YI'Q' (' indicating normalized notation) is slightly different in order to compress the I' and Q' output range to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = R_0–R_7
DB0–DB7 = G_0–G_7
DC0–DC7 = B_0–B_7

QA0–QA7 = I'_0–I'_7
QB0–QB7 = Y_0–Y_7
QC0–QC7 = Q'_0–Q'_7

The RGB inputs to the matrix can have a range of 0–255; the lookup table RAMs on the Bt281 may be used to gamma correct the RGB data if necessary. The Y output of the matrix can have a range of 0–255, while the I' and Q' outputs can have a range of –128 to +127. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} Y \\ I' \\ Q' \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.500 & -0.231 & -0.269 \\ 0.203 & -0.500 & 0.297 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} I' \\ Y \\ Q' \end{bmatrix} = \begin{bmatrix} \$0.80 & \$7.C5 & \$7.BC \\ \$0.4C & \$0.96 & \$0.1D \\ \$0.33 & \$7.80 & \$0.4C \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the DAx and DCx inputs, and either offset binary or 2's complement representation for the QAx and QCx outputs. Command bits CR17–CR15 should be 000.

Application Information *(continued)*

Y/R-Y/B-Y-to-RGB Conversion

The matrix for converting analog Y/R-Y/B-Y to RGB is as follows. The Y, R-Y, B-Y inputs are not normalized and generate gamma-corrected RGB data.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 1 & -0.509 & -0.194 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} Y \\ R-Y \\ B-Y \end{bmatrix}$$

The analog (R – Y) and (B – Y) terms have an input range of ±0.701 and ±0.886, respectively, while Y has a range of 0–1.

The conversion of normalized digital Y,(R – Y)',(B – Y)' (' indicating normalized notation) to digital RGB is slightly different, as the (R – Y)' and (B – Y)' input range has probably been compressed to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = $(R-Y)'_0$–$(R-Y)'_7$
DB0–DB7 = Y_0–Y_7
DC0–DC7 = $(B-Y)'_0$–$(B-Y)'_7$

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0–255 for Y, while the (R – Y)' and (B – Y)' inputs can have an input range of –128 to +127. The gamma-corrected RGB outputs of the matrix can have a range of 0–255. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.402 & 0 \\ 1 & -0.714 & -0.344 \\ 1 & 0 & 1.772 \end{bmatrix} \begin{bmatrix} Y \\ (R-Y)' \\ (B-Y)' \end{bmatrix}$$

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.66 & \$1.00 & \$0.00 \\ \$7.4A & \$1.00 & \$7.A8 \\ \$0.00 & \$1.00 & \$1.C5 \end{bmatrix} \begin{bmatrix} (R-Y)' \\ Y \\ (B-Y)' \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR17–CR15 should be 000.

Application Information *(continued)*

YUV-to-RGB Conversion

The matrix for converting analog YUV to RGB is as follows. The YUV inputs are not normalized and generate gamma-corrected RGB data.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.140 \\ 1 & -0.395 & -0.581 \\ 1 & 2.032 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

The analog U and V terms have an input range of ±0.436 and ±0.615, respectively, while Y has a range of 0–1.

The conversion of normalized digital YU'V' (' indicating normalized notation) to RGB is slightly different, as the V' input range has probably been compressed to ±0.5 while the U' input range has probably been expanded to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = V'_0–V'_7
DB0–DB7 = Y_0–Y_7
DC0–DC7 = U'_0–U'_7

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0–255, while the U' and V' inputs can have an input range of –128 to +127. The gamma-corrected RGB outputs of the matrix can have a range of 0–255. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.402 \\ 1 & -0.344 & -0.714 \\ 1 & 1.772 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U' \\ V' \end{bmatrix}$$

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output assignment, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.66 & \$1.00 & \$0.00 \\ \$7.4A & \$1.00 & \$7.A8 \\ \$0.00 & \$1.00 & \$1.C5 \end{bmatrix} \begin{bmatrix} V' \\ Y \\ U' \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR1– CR15 should be 000.

Application Information *(continued)*

YIQ-to-RGB Conversion

The matrix for converting analog YIQ to RGB is as follows. The YIQ inputs are not normalized and generate gamma-corrected RGB data.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0.956 & 0.620 \\ 1 & -0.272 & -0.647 \\ 1 & -1.108 & 1.705 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

The analog I and Q terms have an input range of ±0.596 and ±0.525, respectively, while Y has a range of 0–1.

The conversion of normalized digital YI'Q' (' indicating normalized notation) to RGB is slightly different, as the I' and Q' input range has probably been compressed to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = I_0–I_7
DB0–DB7 = Y_0–Y_7
DC0–DC7 = Q_0–Q_7

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0–255, while the I' and Q' inputs can have an input range of –128 to +127. The gamma-corrected RGB outputs of the matrix can have a range of 0–255. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.139 & 0.648 \\ 1 & -0.324 & -0.677 \\ 1 & -1.321 & 1.783 \end{bmatrix} \begin{bmatrix} Y \\ I' \\ Q' \end{bmatrix}$$

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output assignment, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.23 & \$1.00 & \$0.A5 \\ \$7.AE & \$1.00 & \$7.53 \\ \$6.AE & \$1.00 & \$1.C8 \end{bmatrix} \begin{bmatrix} I' \\ Y \\ Q' \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR17–CR15 should be 000.

Application Information *(continued)*

YIQ (D2 Format)-to-RGB Conversion

The digital composite video format digitizes the entire composite color video signal, including sync information. Thus, after digitally separating the Y, I, and Q information, the Y information has a range of 0 to 130, I has a range of 0 to ±78, and Q has a range of 0 to ±68.

The matrix for converting digital YIQ (derived from digital composite video format) to RGB is as follows.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1.972 & 1.875 & 1.223 \\ 1.972 & -0.538 & -1.267 \\ 1.972 & -2.187 & 3.361 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = I_0–I_7
DB0–DB7 = Y_0–Y_7
DC0–DC7 = Q_0–Q_7

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0 to 130, while the I input can have a range of 0 to ±78 and Q can have a range of 0 to ±68. The gamma-corrected RGB outputs of the matrix have a range of 0 to 255.

Given that the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output assignment, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.E0 & \$1.F9 & \$1.39 \\ \$7.77 & \$1.F9 & \$6.BC \\ \$5.D1 & \$1.F9 & \$3.5C \end{bmatrix} \begin{bmatrix} I \\ Y \\ Q \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR17–CR15 should be 100.

Application Information *(continued)*

Concatenating Matrices

When matrices are concatenated, conversions such as YIQ to YUV may be implemented. The formula for concatenating matrices is as follows:

$$\begin{bmatrix} aj + bm + cp & ak + bn + cq & al + bo + cr \\ dj + em + fp & dk + en + fq & dl + eo + fr \\ gj + hm + ip & gk + hn + iq & gl + ho + ir \end{bmatrix} = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \begin{bmatrix} j & k & l \\ m & n & o \\ p & q & r \end{bmatrix}$$

Implementing RGB to HSV

RGB may be converted to HSV by configuring the Bt281 to implement RGB-to-Y/R-Y/B-Y conversion.

The V value is equivalent to the Y (luminance) output onto QB0–QB7.

$$\text{Saturation (S)} = \text{SQRT}(R - Y^{2)} + (B - Y)$$

$$\text{Hue (H)} = \tan^{-1}(B - Y) / (R - Y)$$

When the 16 bits (8 bits each) of (R – Y) and (B – Y) data generated by the Bt281 are used to address a 64K x 8 ROM, the ROM may be programmed to generate 8 bits of saturation data with the equation above. [A 16K x 8 ROM may be used, addressed by the 6 MSBs of the (R – Y) and (B – Y) data.] An output register on the ROM data outputs may be needed to meet setup and hold times for any circuitry after the ROM.

When the same 16 bits of (R – Y) and (B – Y) data generated by the Bt281 are to address another 64K x 8 ROM, this ROM is programmed to generate 8 bits of hue data with the equation above. [A 16K x 8 ROM may be addressed by the 6 MSBs of the (R – Y) and (B – Y) data.] An output register on the ROM data outputs may be needed to meet setup and hold times for any circuitry after the ROM.

A single 64K x 16 ROM may be used rather than two 64K x 8 ROMs.

Implementing HSV to RGB

HSV may be converted to RGB by configuring the Bt281 to implement Y/R-Y/B-to-RGB conversion.

The V value is equivalent to the Y (luminance) input to DB0–DB7.

$$R - Y = S * \cos(H)$$

$$B - Y = S * \sin(H)$$

When the 16 bits (8 bits each) of saturation (S) and hue (H) data are used to address a 64K x 8 ROM, the ROM may be programmed to generate 8 bits of (R – Y) data to input to the Bt281 with the equation above. (A 16K x 8 ROM may be used, addressed by the 6 MSBs of the S and H data.) An input register on the ROM data inputs may be needed to meet setup and hold times to the ROM.

The same 16 bits (8 bits each) of saturation (S) and hue (H) data to address a 64K x 8 ROM (a 16K x 8 ROM may be used addressed by the six MSBs of the S and H data), the ROM is programmed to generate 8 bits of (B – Y) data to input to the Bt281 using the equation above. An input register on the ROM data inputs may be needed to meet setup and hold times.

A single 64K x 16 ROM may be used rather than two 64K x 8 ROMs.

Application Information *(continued)*

Matrix Coefficient Considerations

The example matrices are only typical; adjustment of the matrix coefficients may be required to minimize rounding errors, especially when multiple devices are cascaded.

Also, the matrix coefficients may be multiplied (left shifted) by 2 or 4; and the M1–M8 (2x) or M2–M9 (4x) outputs may be selected, rather than the M0–M7 outputs. This may reduce rounding errors, especially when multiple devices are used.

Color Correction of Cameras

The color response of a video camera is never exactly that specified by the standards, which require negative responses to certain portions of the light spectrum. In practice, this is achieved by matrixing the three color signals of the form:

$$R_{correct} = aR_{cam} + bG_{cam} + cB_{cam}$$

$$G_{correct} = dR_{cam} + eG_{cam} + fB_{cam}$$

$$B_{correct} = gR_{cam} + gG_{cam} + iB_{cam}$$

where the constants a, e, and i are positive values near unity, and the other constants are small in comparison with unity and usually negative.

Since it is usually desired to keep the color balance of the camera constant:

$$a + b + c = 1$$

$$d + e + f = 1$$

$$g + h + i = 1$$

Rather than implement the color correction with differential amplifiers, the Bt281 makes it feasible to use a digital architecture involving matrix multiplication.

Adjusting Contrast and Saturation

By scaling the matrix or lookup table RAM values, the contrast and saturation of a video signal may be adjusted while simultaneously converting to another color space.

Typical Applications

Figures 5 and 6 show typical applications of the Bt281 in an image-capture-and-display environment.

The Bt281 may also be placed between the frame buffer memory and MPU. Thus, the MPU may operate in a single color space while many color spaces may reside in the frame buffer. The CLOCK of the Bt281 will typically be connected to the video system clock.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information *(continued)*

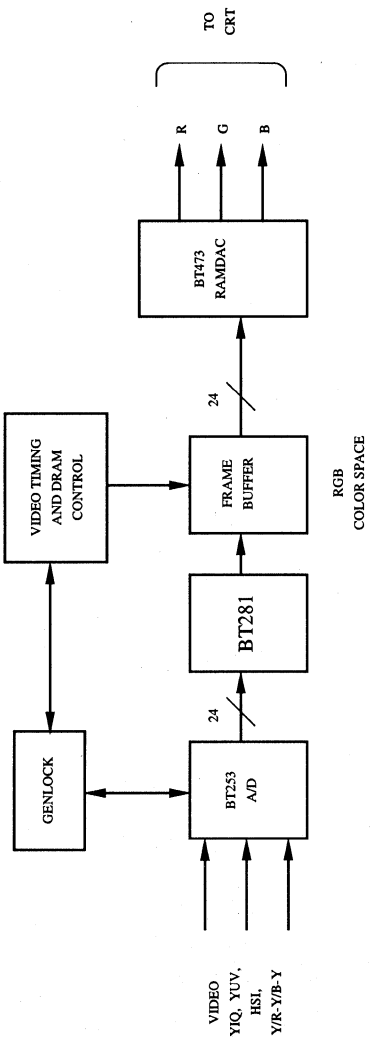


Figure 5. Typical Application.

Application Information *(continued)*

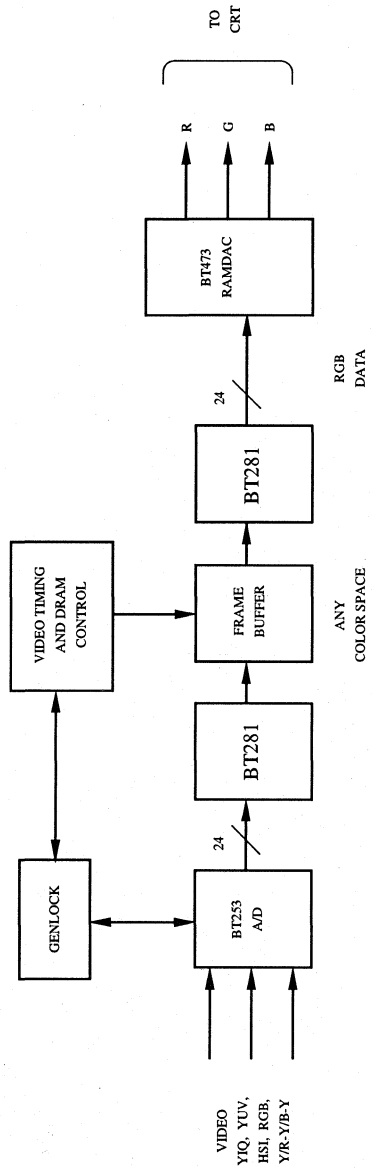


Figure 6. Typical Application.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND– 0.5		VCC + 0.5	V
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	COUT		10		pF
QAx, QBx, QCx Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	COUT		10		pF
Other Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
Output Capacitance	COUT		10		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			27	MHz
A0, A1, CS* Setup Time	1	10			ns
A0, A1, CS* Hold Time	2	10			ns
RD*, WR* Low Time	3	70			ns
RD*, WR* High Time	4	15			ns
RD* Asserted to Data Bus Driven	5	1			ns
RD* Asserted to Data Valid	6			70	ns
RD* Negated to Data Bus 3-Stated	7			20	ns
Write Data Setup Time	8	10			ns
Write Data Hold Time	9	10			ns
Pixel and Control Setup Time	10				
DAx, DBx, DCx, IN0, IN1, CFLAG		5			ns
Pixel and Control Hold Time	11				
DAx, DBx, DCx, IN0, IN1, CFLAG		4			ns
Clock Cycle Time	12	37			ns
Clock Pulse Width High	13	10			ns
Clock Pulse Width Low	14	10			ns
Pipeline Delay		14	14	14	Clocks
Output Delay	15	tbd		16	ns
Three-State Disable Time	16			15	ns
Three-State Enable Time	17			15	ns
VCC Supply Current (Note 1)	ICC		220	250	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. See Figures 7–11. QAx, QBx, QCx, OUT0, and OUT1 output load ≤ 75 pF, and D0–D7 output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC (max).

Timing Waveforms

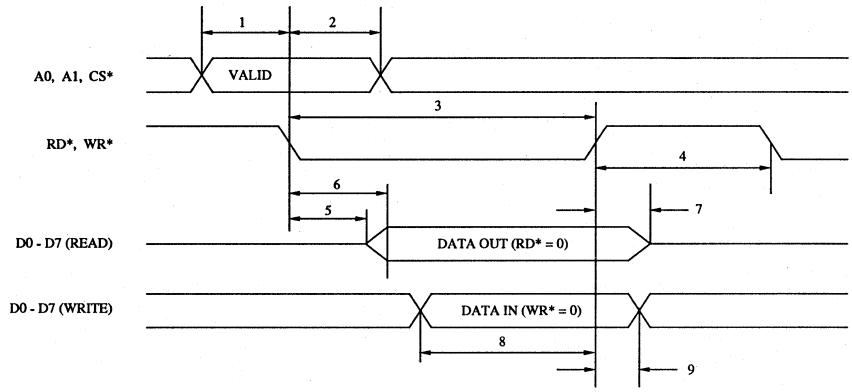


Figure 7. MPU Read/Write Timing.

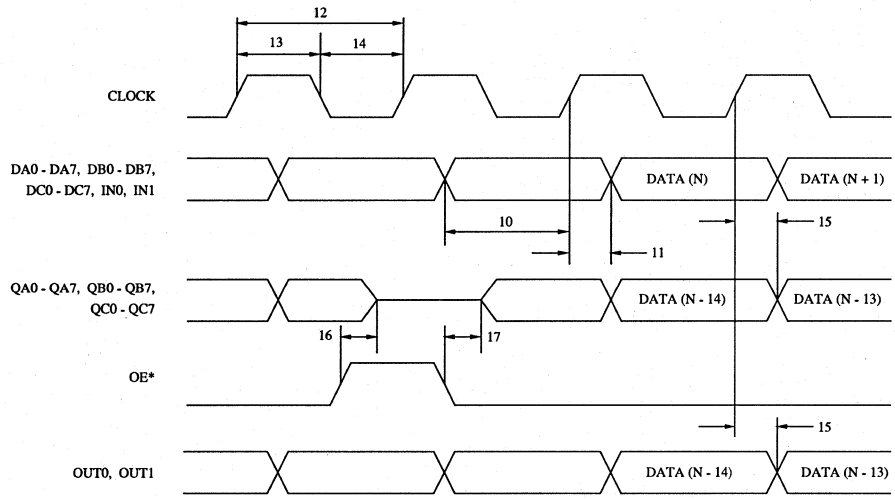


Figure 8. Video Input/Output Timing
(Bypass or Noninterpolated and Nonmultiplexed 24-bit I/O).

Timing Waveforms *(continued)*

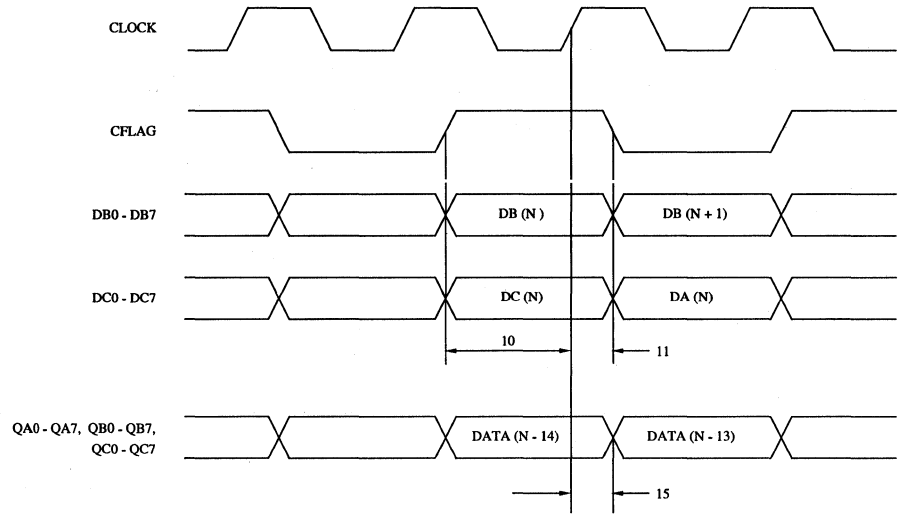


Figure 9. Video Input/Output Timing (Multiplexed and Interpolated 16-bit Input, and 24-bit Output).

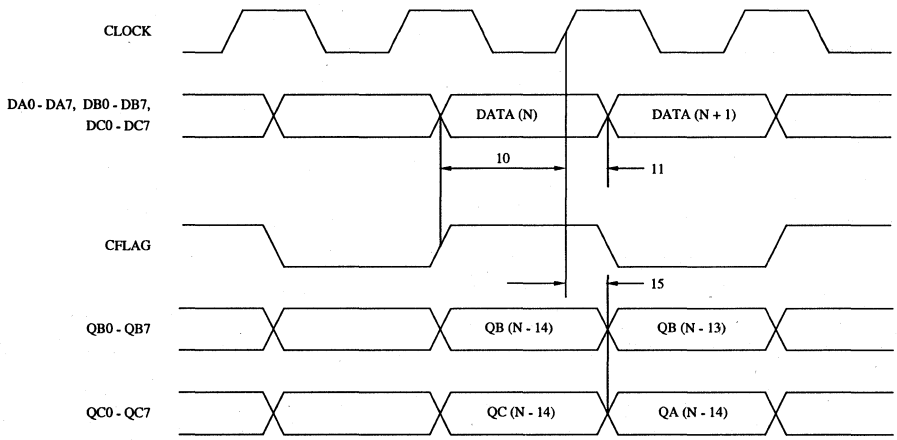


Figure 10. Video Input/Output Timing (24-bit Input, Multiplexed and Decimated 16-bit Output).

Timing Waveforms *(continued)*

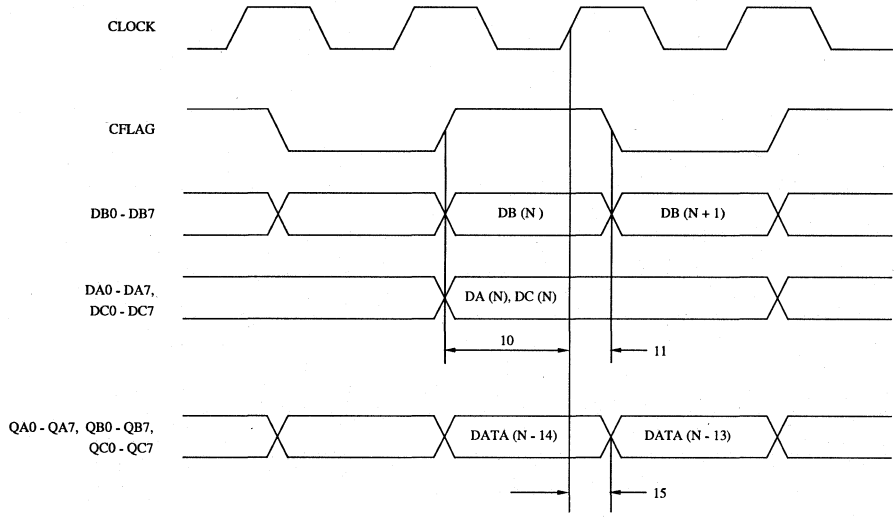


Figure 11. Video Input/Output Timing (Nonmultiplexed and Interpolated 24-bit Input, and 24-bit Output).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt281KPJ	84-pin Plastic J-Lead	0° to +70° C

Advance Information

This document contains information on a product under development. The information providedis subject to change.

Bt812

NTSC / PAL to RGB / YCrCb Decoder

3

Distinguishing Features

- Ability to Digitize Composite or Y/C (NTSC or PAL)
- Flexible Video Resolutions up to 16.5 MSPS
- On-Chip Ultralock™
- Programmable Hue, Brightness, Contrast, and Saturation
- Supports 2X Clock Operation
- RGB or YCrCb Output Formats
- 0.7–2 V Video Input Signals
- Standard MPU Interface
- 160-pin PQFP Package
- JTAG Support
- Typical Power Dissipation: 1.6 W

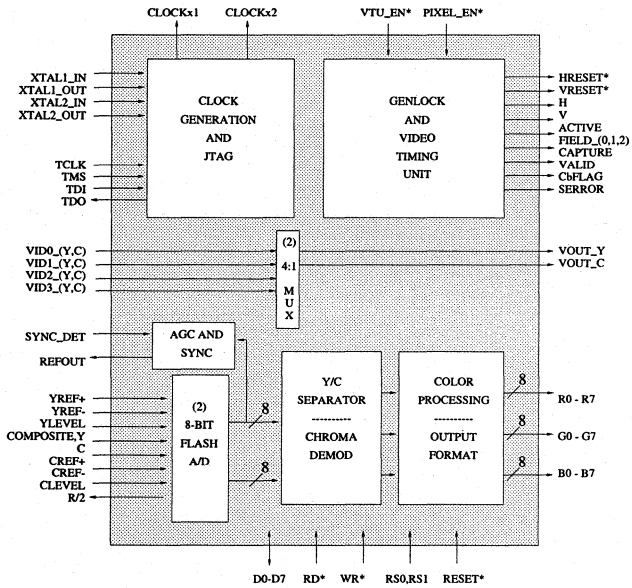
Applications

- Multimedia
- Image Processing
- Desktop Video

Related Products

- Bt858
- Bt855

Functional Block Diagram



Product Description

The Bt812 Image Digitizer converts NTSC and PAL composite or Y/C analog video signals to either digital RGB or YCrCb video data at pixel rates from 8–16.5 MHz. This digitizer supports 24-bit RGB, 16-bit RGB, 15-bit RGB, 4:4:4 24-bit YCrCb, or 4:2:2 16-bit YCrCb output formats.

The hue, contrast, saturation, and brightness levels are adjustable through the MPU interface.

The 4:1 analog multiplexers enable the NTSC, PAL, Y, and C video signals to be individually filtered before the Bt812 is driven, simplifying external circuitry.

Horizontal and vertical timing information is generated and output through HRESET* and VRESET*. Programmable blanking information is output on the H, V, and ACTIVE pins. The FIELD_0, FIELD_1 and FIELD_2 outputs specify which one of four (NTSC) or eight (PAL) fields is being processed.

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L812001 Rev. A

Brooktree®

Advance Information

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Bt855

12–18 MHz RGB/YCrCb-to-NTSC/PAL Encoder

3

Distinguishing Features

- Pin/Software Compatible with Bt858
- NTSC or PAL Composite Video Output
- Interlaced 60 Hz 525-Line Digital RGB or YCrCb Input (NTSC Output)
- Interlaced 50 Hz 625-Line Digital RGB or YCrCb Input (PAL Output)
- Separate Y/C Video (S-Video) Outputs
- 4-Field NTSC or 8-Field PAL Generation
- On-Chip Color Bar Generation
- Three 256 x 8 Input Lookup Table RAMs
- 15 x 24 Overlay Registers
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 160-pin PQFP Package
- Typical Power Dissipation: 1.0 W

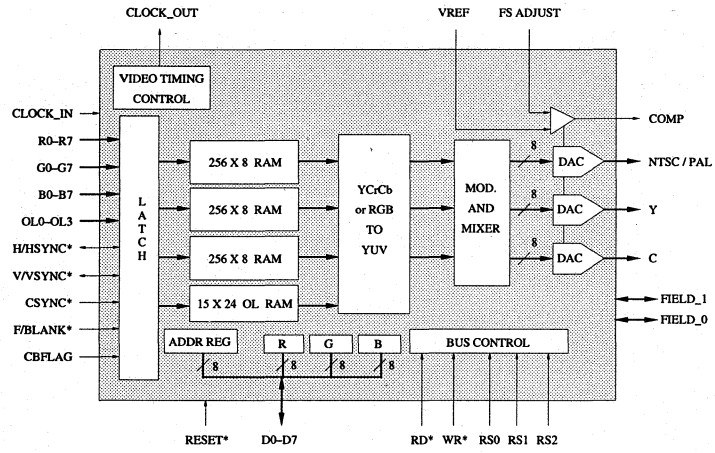
Applications

- Desktop Video
- Video Editing
- Video Presentations

Related Products

- Bt858

Functional Block Diagram



Product Description

The Bt855 is designed specifically for graphics and imaging systems requiring the generation of four-field, 525-line (M) NTSC or eight-field, 625-line (B, D, G, H, I, N) PAL composite, or Y/C (S-video) video signals at pixel clock rates of 10–18 MHz. NTSC with a 4.43 MHz color subcarrier is also supported. The number of pixels per scan line is programmable, so applications other than 12.27 MHz square pixel NTSC, 13.5 MHz CCIR601, and 14.75 MHz square pixel PAL are easily supported.

Video timing control may be input with horizontal and vertical sync, or composite sync control signals. Alternately, the Bt855 may generate the horizontal and vertical sync signals.

The interlaced RGB or YCrCb data is converted to YUV. The color difference signals are digitally low-pass filtered to 1.3 MHz and modulated. The rise and fall times of sync, burst envelope, and video blanking are internally controlled to be within composite video specifications.

Analog luminance (Y) and chroma (C) information are available on the Y and C analog outputs for interfacing to S-video equipment. Composite analog video is output simultaneously onto the NTSC/PAL analog output.

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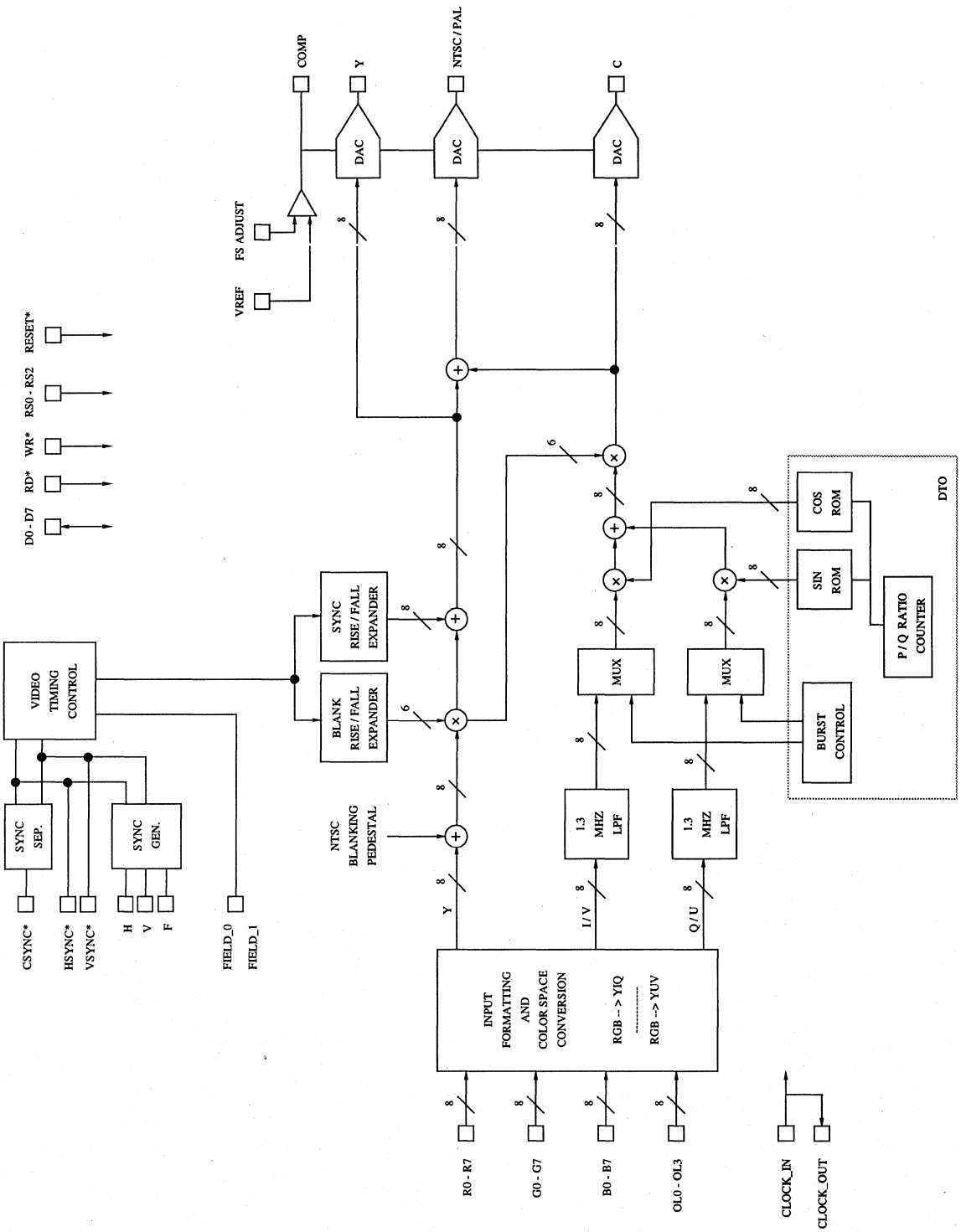


Figure 1. Detailed Block Diagram.

Circuit Description—MPU Interface

MPU Interface

As illustrated in the detailed block diagram (Figure 1), the Bt855 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, or control registers, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode, control register read/write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	control registers

Table 1. Control Input Truth Table.

Circuit Description—MPU Interface (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Control Register Data

To write control register data, the MPU loads the address register (control register read/write mode) with the address of the control register to be read. The MPU performs a write cycle, using RS0–RS2 to select the control registers. After the write cycle, the address register (ADDR0–ADDR7) increments to the next location, which the MPU may write by writing another byte of data. A block of data in consecutive control registers may be written by writing the start address and performing continuous write cycles until the entire block has been written.

Reading Control Register Data

To read control register data, the MPU loads the address register (control register read/write mode) with the address of the control register to be read. The MPU performs a read cycle, using RS0–RS2 to select the control registers. After the read cycle, the address register (ADDR0–ADDR7) increments to the next location, which the MPU may read by reading another byte of data. A block of data in consecutive control registers may be read by writing the start address and performing continuous read cycles until the entire block has been read.

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0, depending on the mode). Bit D0 also corresponds to data bus bit D0.

Note: The pixel read mask register is not initialized upon power-up. The user must initialize this register for proper operation.

Circuit Description—MPU Interface (continued)

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

When the MPU is accessing the control registers, the address register does not reset to $00 following a read or write cycle to address $FF. Data read from reserved locations returns invalid data.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. To reduce noticeable sparkling on the analog outputs during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7), incremented following a blue read or write cycle, are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	0	1	red/Cr value
	01	x	0	1	green/Y value
	10	x	0	1	blue/Cb value
ADDR0–7 (counts binary)	$00–$FF	0	0	1	color palette RAMs
	$x0	1	0	1	reserved
	$x1	1	0	1	overlay color 1
	:	:	:	:	:
	$xF	1	0	1	overlay color 15
	$00	1	1	0	command register_0
	$01	1	1	0	command register_1
	$02	1	1	0	command register_2
	$03	1	1	0	command register_3
	$04	1	1	0	command register_4
	$05	1	1	0	reserved ($00)
	$06	1	1	0	P1 low register (Note 1)
	$07	1	1	0	P1 high register (Note 1)
	$08	1	1	0	P2 low register (Note 1)
	$09	1	1	0	P2 high register (Note 1)
	$0A	1	1	0	reserved ($00)
	$0B	1	1	0	reserved ($00)
	$0C	1	1	0	HCOUNT low register
	$0D	1	1	0	HCOUNT high register

Note 1: Writing to this location automatically resets the timing circuitry.

Table 2. Address Register (ADDR) Operation.

Overlays

The OL0–OL3 inputs are used to select overlays and have priority over the pixel data. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the R0–R7, G0–G7, and B0–B7 pixel data. Overlay palette data must be in 2's complement format.

OL3–OL0	Color Selected
0000	RGB pixel input port
0001	overlay color 1
:	:
1111	overlay color 15

24-Bit RGB Input Mode (8, 8, 8)

The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN.

The R0–R7 inputs address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YUV matrix. If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YUV matrix.

16-bit RGB Input Mode (5, 6, 5)

The OL0–OL3, R0–R7 and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The B0–B7 inputs are ignored.

The R3–R7 inputs address the lower 32 locations of the red color palette RAM. The G5–G7 and R0–R2 inputs address the lower 64 locations of the green color palette RAM. The G0–G4 inputs address the lower 32 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YUV matrix. If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YUV matrix.

16-bit RGB Input Mode (6, 6, 4)

The OL0–OL3, R0–R7, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The B0–B7 inputs are ignored.

The R2–R7 inputs address the lower 64 locations of the red color palette RAM. The G4–G7, R0, and R1 inputs address the lower 64 locations of the green color palette RAM. The G0–G3 inputs address the lower 16 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YUV matrix. If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YUV matrix.

15-bit RGB Input Mode (5, 5, 5)

The OL0–OL3, R0–R6, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The R7 and B0–B7 inputs are ignored.

The R2–R6 inputs address the lower 32 locations of the red color palette RAM. The G5–G7, R0, and R1 inputs address the lower 32 locations of the green color palette RAM. The G0–G4 inputs address the lower 32 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YUV matrix. If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YUV matrix.

24-Bit YCrCb Mode

The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. The Y0–Y7 are input by G0–G7, Cr0–Cr7 are input by R0–R7, and Cb0–Cb7 are input by B0–B7. The Y0, Cr0, and Cb0 are the least significant bits.

The Y addresses the green color palette RAM, Cr addresses the red color palette RAM, and Cb addresses the blue color palette RAM. Each lookup table RAM provides 8 bits of information to the YCrCb-to-YUV matrix. Before the YCrCb-to-YUV matrix is addressed, Y has an input range of 16–235; values less than 16 are made 16, and values greater than 235 are made 235. The Cr and Cb have an input range of 16–240

with 128 equal to zero; values less than 16 are made 16, and values greater than 240 are made 240.

If overlay information is being displayed (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of YCrCb color information to the YCrCb-to-YUV matrix.

16-Bit YCrCb Mode

The OL0–OL3, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. The R0–R7 inputs are ignored. The Y0–Y7 are input by G0–G7, and multiplexed Cr and Cb data is input by the B0–B7 inputs, as specified in Table 3. The Y0, Cr0, and Cb0 inputs are the least significant bits.

The CbFLAG input is used to indicate when Cb data is present on the B0–B7 inputs. While CbFLAG is a logical one, Cb data is latched; while CbFLAG is a logical zero, Cr data is latched. CbFLAG is latched on the rising edge of CLOCK_IN.

The 16-bit YCrCb (4:2:2) data is converted to 24-bit YCrCb (4:4:4) with a two-tap interpolation filter to generate the missing Cr and Cb values. (The original Cr and Cb values pass through unchanged.)

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Y addresses the green color palette RAM, Cr addresses the red color palette RAM, and Cb addresses the blue color palette RAM. Each

3

RGB Inputs	24-bit RGB (8, 8, 8) Mode	16-bit RGB (5, 6, 5) Mode	16-bit RGB (6, 6, 4) Mode	15-bit RGB (5, 5, 5) Mode	24-bit YCrCb Mode	16-bit YCrCb Mode	Pseudo-Color Mode
R7	R7	R4	R5	x	Cr7	x	P7
R6	R6	R3	R4	R4	Cr6	x	P6
R5	R5	R2	R3	R3	Cr5	x	P5
R4	R4	R1	R2	R2	Cr4	x	P4
R3	R3	R0	R1	R1	Cr3	x	P3
R2	R2	G5	R0	R0	Cr2	x	P2
R1	R1	G4	G5	G4	Cr1	x	P1
R0	R0	G3	G4	G3	Cr0	x	P0
G7	G7	G2	G3	G2	Y7	Y7	P7
G6	G6	G1	G2	G1	Y6	Y6	P6
G5	G5	G0	G1	G0	Y5	Y5	P5
G4	G4	B4	G0	B4	Y4	Y4	P4
G3	G3	B3	B3	B3	Y3	Y3	P3
G2	G2	B2	B2	B2	Y2	Y2	P2
G1	G1	B1	B1	B1	Y1	Y1	P1
G0	G0	B0	B0	B0	Y0	Y0	P0
B7	B7	x	x	x	Cb7	Cb7 / Cr7	P7
B6	B6	x	x	x	Cb6	Cb6 / Cr6	P6
B5	B5	x	x	x	Cb5	Cb5 / Cr5	P5
B4	B4	x	x	x	Cb4	Cb4 / Cr4	P4
B3	B3	x	x	x	Cb3	Cb3 / Cr3	P3
B2	B2	x	x	x	Cb2	Cb2 / Cr2	P2
B1	B1	x	x	x	Cb1	Cb1 / Cr1	P1
B0	B0	x	x	x	Cb0	Cb0 / Cr0	P0

Table 3. Data Input Formats.

Circuit Description—Pixel Input Formats (continued)

lookup table RAM provides 8 bits of information to the YCrCb-to-YUV matrix. Before addressing the YCrCb-to-YUV matrix, Y has an input range of 16–235; values less than 16 are made 16, and values greater than 235 are made 235. The Cr and Cb have an input range of 16–240, with 128 equal to zero; values less than 16 are made 16, and values greater than 240 are made 240.

If overlay information is being displayed (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of RGB color information to the RGB-to-YUV matrix.

Pseudo-Color Mode

The R0–R7, G0–G7, or B0–B7 inputs (as specified by command bits CR04–CR07) address all three lookup table RAMs simultaneously, generating 24 bits of color information. The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. Each lookup table RAM provides 8 bits of color information to the RGB-to-YUV matrix. If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YUV matrix.

Internal Color Bar Generator

A color bar test pattern output can be internally generated by the device when it is configured for 24-bit RGB operation. This is enabled by bit CR32 in Command Register_3. The bars are 100 percent saturated, 75 percent amplitude consisting of gray, yellow, cyan, green, magenta, red, blue, and black. They fill the entire screen vertically, and the first seven colors occupy 64 pixels each, horizontally along a scan line. Black occupies the remaining active pixels on each scan line.

Circuit Description—Video Timing

General Video Timing

The Bt855 is designed to accept and output interlaced video to conform to the NTSC or PAL timing specifications. Interlaced 60-Hz, 525-line digital RGB or YCrCb input will produce standard analog NTSC outputs. Interlaced 50-Hz, 625-line digital RGB or YCrCb input will produce standard analog PAL output. Nonstandard line counts in PAL or NTSC modes are not supported.

The Bt855 automatically calculates the width of the analog horizontal sync pulses, and the start and end of color burst. It automatically disables color burst on appropriate scan lines, and generates serration and equalization pulses on appropriate scan lines.

In addition, the rise and fall times of sync, blanking, and the burst envelope are internally controlled to conform to the composite video specifications.

The user must only provide information on the number of pixels per scan line (via the HCOUNT register), and program the P1 and P2 registers to generate the correct color subcarrier frequency for a given pixel clock rate.

During NTSC operation, color burst information is automatically disabled on scan lines 1–6, 261–269, and 523–525, inclusive.

During PAL operation, color burst information is automatically disabled on scan lines 1–6, 310–318, and 622–625 during fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is automatically disabled on scan lines 1–5, 311–319, and 623–625, inclusive.

Master Mode 0

External horizontal sync (HSYNC*), vertical sync (VSYNC*), and composite blanking (BLANK*) must be supplied to the Bt855. HSYNC*, VSYNC*, and BLANK* are configured as inputs and are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, and OL0–OL3 inputs are ignored. The CSYNC* pin is configured as an input and is ignored.

CR43 programmed low will three-state CSYNC*, HSYNC*, and VSYNC*. CR43 programmed high will enable CSYNC* as a valid composite sync output, but HSYNC* and VSYNC* will still be internally gated to three-state as required by Master Mode 0.

Coincident falling edges of the HSYNC* and VSYNC* input indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

Only the falling edges of HSYNC* and VSYNC* are used—HSYNC* need not be the width of the analog horizontal sync pulse desired. VSYNC* need not be the width of the analog vertical sync pulse desired and must not contain serration or equalization pulses.

Figures 2 and 3 illustrate the video timing for NTSC and PAL, respectively. Nonstandard NTSC line numbering is used in Figure 2.

Vertical Timing

Coincident falling edges of VSYNC* and HSYNC* reset the 10-bit vertical counter to $001. (The number one scan line is the first scan line of the vertical sync interval at the beginning of an odd field.) The vertical counter increments on the falling edge of HSYNC*.

The Bt855 will generate 525 scan lines (NTSC operation) or 625 scan lines (PAL operation) per frame, 2:1 interlaced. The 10-bit vertical counter is also reset to $001 upon reaching a count of 525 (NTSC) or 625 (PAL).

Horizontal Timing

The falling edge of HSYNC* resets a 12-bit horizontal counter to $001. The horizontal counter increments on the rising edge of CLOCK_IN. The counter value is compared to various internal values automatically calculated by the device to determine when to start and stop various control signals (such as horizontal sync and burst gate).

The 12-bit horizontal counter is also reset to $001 upon reaching the count specified by HCOUNT.

NTSC Blanking

The BLANK* input is used to specify when to output active video. Blanking is automatically done (regardless of the value of BLANK*) for the entire scan line at the beginning of scan lines 1–17, 261–279, and 523–525, inclusive.

On scan line 260 (where the first half of the scan line contains active video), the Bt855 automatically blanks the last half of the scan line regardless of the value of BLANK*. On scan line 280 (where the last half of the scan line contains active video), the Bt855 automatically blanks the first half of the scan line regardless of the value of BLANK*.

On the remaining scan lines, BLANK* is used to specify when to display active video. For further information, refer to P2 Low and High Registers in the Internal Registers section.

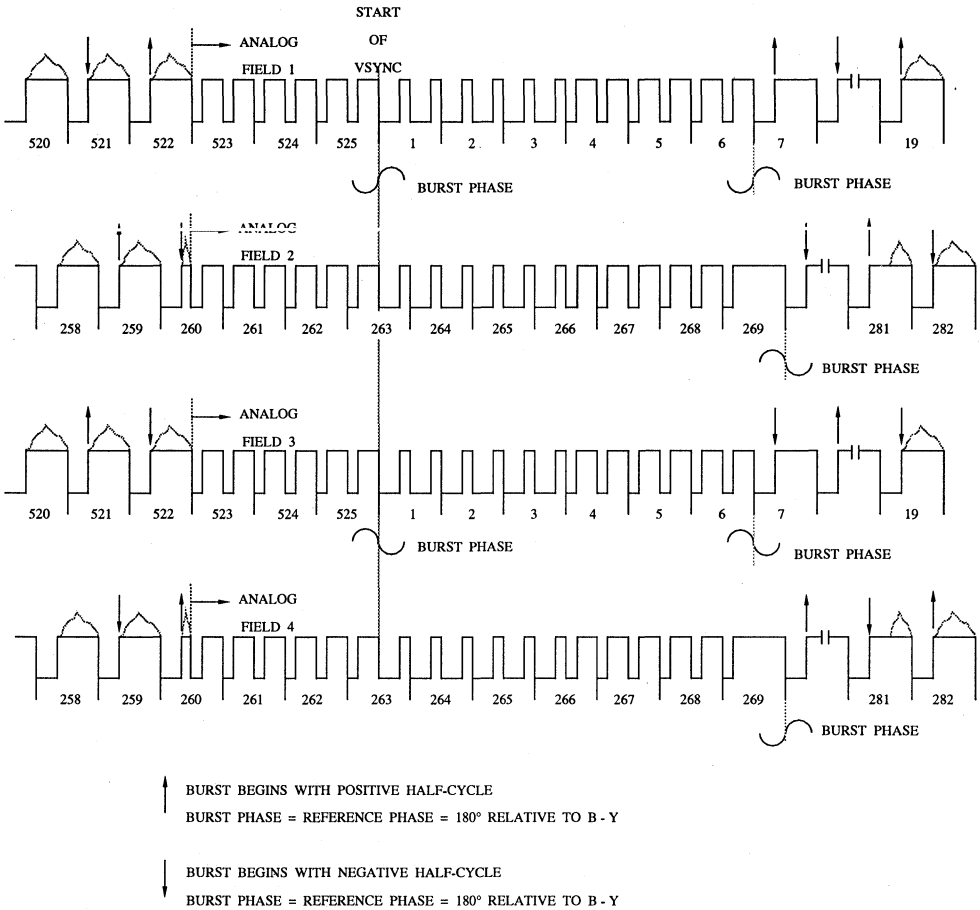
PAL Blanking

The BLANK* input is used to specify when to output active video. Blanking is automatically done (regardless of the value of BLANK*) for the entire scan line at the beginning of scan lines 1–22, 311–335, and 624–625, inclusive.

On scan line 623 (where the first half of the scan line contains active video), the Bt855 automatically blanks the last half of the scan line regardless of the value of BLANK*. On scan line 23 (where the last half of the scan line contains active video), the Bt855 automatically blanks the first half of the scan line regardless of the value of BLANK*.

On the remaining scan lines, BLANK* is used to specify when to display active video. For further information, refer to P2 Low and High Registers in the Internal Registers section.

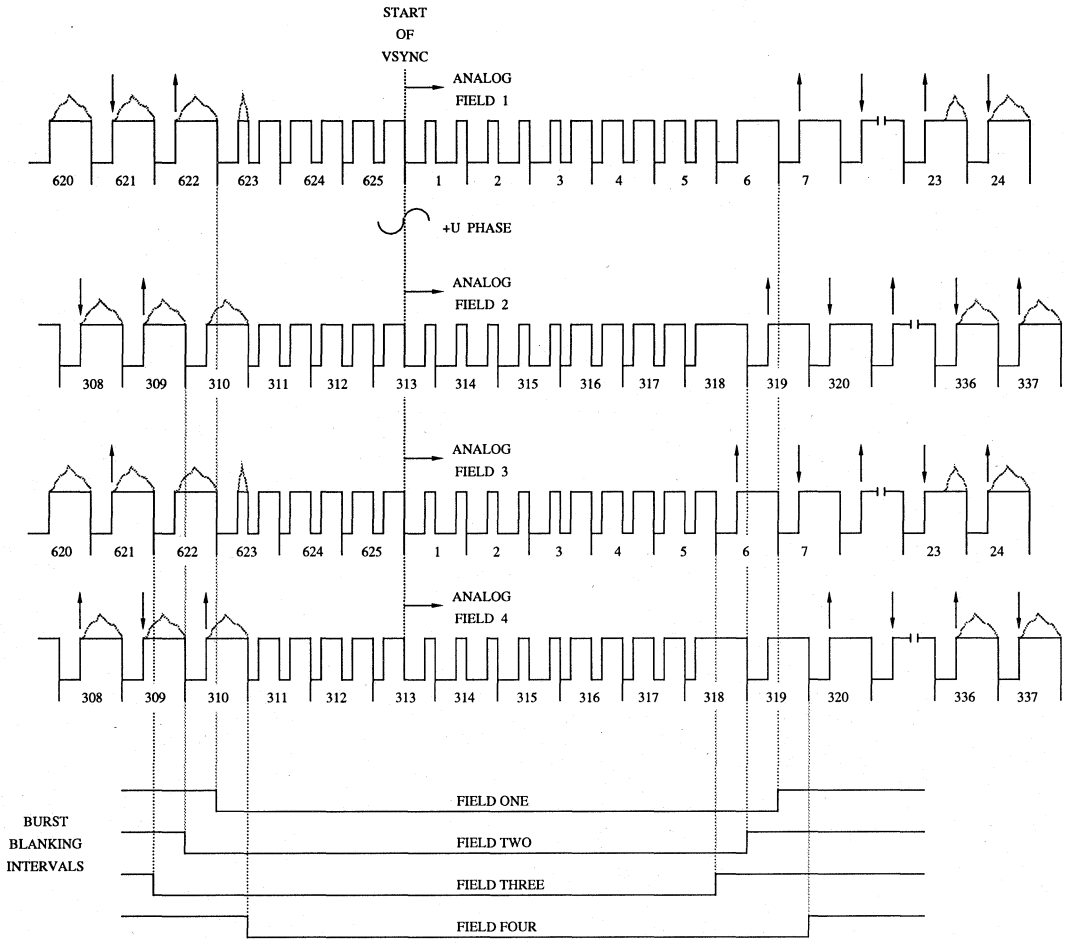
Circuit Description—Video Timing (continued)



Note: To simplify the implementation, the line numbering does not match that used in standard practice for NTSC video signals.

Figure 2. NTSC Video Timing.

Circuit Description—Video Timing (continued)



BURST PHASE = REFERENCE PHASE = 135° RELATIVE TO U
PAL SWITCH = 0, +V COMPONENT

BURST PHASE = REFERENCE PHASE +90° = 225° RELATIVE TO U
PAL SWITCH = 1, -V COMPONENT

Figure 3a. PAL Video Timing.

Circuit Description—Video Timing (continued)

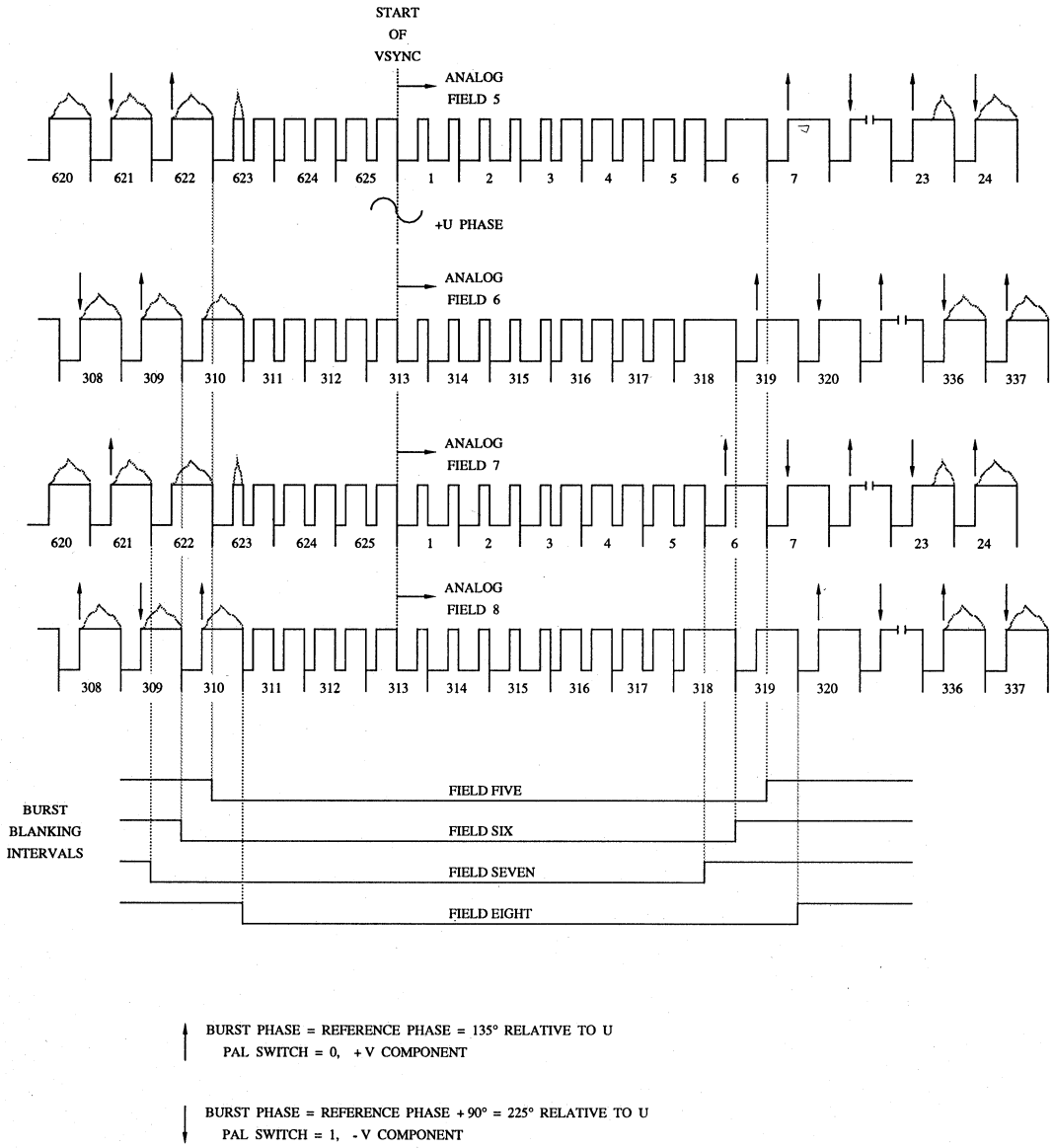


Figure 3b. PAL Video Timing (continued).

Circuit Description—Video Timing (continued)

Master Mode 1

External composite sync (CSYNC*) and composite blanking (BLANK*) must be supplied to the Bt855. CSYNC* and BLANK* are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, and OL0–OL3 inputs are ignored. The HSYNC* and VSYNC* pins are configured as outputs and three-stated. CR43 must be set low to three-state CSYNC*, HSYNC*, and VSYNC*.

The composite sync (CSYNC*) information is separated into horizontal and vertical sync information internally. When the horizontal and vertical sync information is separated from the CSYNC* signal, the functionality and timing are the same as that for Master Mode 0.

In this instance, CSYNC* must contain the proper serration and equalization pulses during the vertical retrace intervals for proper operation.

Vertical Timing

If the previous scan line samples of CSYNC* (at one-fourth and three-fourths HCOUNT) were both a logical one and the current scan line sample of CSYNC* (at one-fourth HCOUNT) is a logical zero, it is assumed to be the beginning of an odd field. The 10-bit vertical counter is reset to $001.

The 10-bit vertical counter is also reset to $001 upon reaching a count of 525 (NTSC operation) or 625 (PAL operation).

Horizontal Timing

After a falling edge of CSYNC* (three-fourths HCOUNT), clock cycles must pass before the next falling edge of CSYNC* is interpreted as a horizontal sync. This filters out any serration and equalization pulses from the composite sync signal. Each gated falling edge resets the horizontal counter to $001.

Master Mode 2

In this mode of operation, the Bt855 is designed to be clocked at 13.5 MHz for digital component video (i.e., CCIR601) applications that use the H (horizontal blanking), V (vertical blanking), and F (even/odd field) control signals.

External horizontal blank (H), vertical blank (V), and even/odd field (F) information must be supplied to the Bt855. The H, V, and F pins are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While either the H or V input is a logical one, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an output and three-stated.

As in Master Mode 0, H and V are internally gated to three-state, and CR43 configures only CSYNC* as an unused input or a valid CSYNC* output.

The horizontal counter is reset to $001, 63 clock cycles after each rising edge of H (horizontal blanking).

The F (field) input is sampled by horizontal sync. When a falling edge of the F input (while both the H and V inputs are a logical one) has been detected, the vertical counter is reset to $001. Thus, while F is a logical zero, an odd field is generated; while F is a logical one, an even field is generated.

The remaining functionality is the same as that for Master Mode 0.

Master Mode 3

Master Mode 3 is similar to Master Mode 0, except that the Bt855 generates and outputs horizontal sync (HSYNC*) and vertical sync (VSYNC*). Composite blanking (BLANK*) must be supplied to the Bt855. HSYNC* and VSYNC* are output following the rising edge of CLOCK_IN. HSYNC* and VSYNC* are asserted for one clock cycle when the horizontal and vertical counters overflow after reaching the value of HCOUNT, and 525 (NTSC) or 625 (PAL).

Coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

BLANK* is an input. It is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, and OL0–OL3 inputs are ignored. The CSYNC* pin is configured as an input and is ignored.

Circuit Description—Video Timing (continued)

FIELD_0 and FIELD_1 Pins

The FIELD_0 and FIELD_1 pins, in conjunction with the HSYNC* and VSYNC* timing relationship (or the F input if the BLANK* input is not required), determine which one of four fields (NTSC) or eight fields (PAL) is being generated.

Even or odd fields may be determined by the HSYNC* and VSYNC* timing relationship. Coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

NTSC

If command bit CR45 is a logical zero, the FIELD_0 pin is configured as an input and is latched on the rising edge of CLOCK_IN. The FIELD_0 pin indicates whether to generate fields one and two (logical zero) or fields three and four (logical one) (see Figure 4). As an input, the FIELD_0 pin should change state only at the beginning of vertical sync during fields one and three. The FIELD_1 pin is configured as an input and is ignored.

If command bit CR45 is a logical one, the FIELD_0 pin is configured as an output following the rising edge of CLOCK_IN. The FIELD_0 pin indicates whether fields one and two (logical zero) or fields three and four (logical one) are being generated. As an output the FIELD_0 pin changes state at the beginning of vertical sync during fields one and three. The FIELD_1 pin is configured as an input and is ignored.

PAL

If command bit CR45 is a logical zero, the FIELD_0 and FIELD_1 pins are configured as inputs and are latched on the rising edge of CLOCK_IN. The FIELD_0 and FIELD_1 pins indicate which field to generate, as shown in Figure 5. As an input, the FIELD_0 pin should change state only at the beginning of vertical sync during fields one, three, five, and seven. The FIELD_1 pin should change state only at the beginning of vertical sync during fields one and five.

If command bit CR45 is a logical one, the FIELD_0 and FIELD_1 pins are configured as outputs and are output following the rising edge of CLOCK_IN. As an output, FIELD_0 changes state at the beginning of vertical sync during fields one, three, five, and seven. FIELD_1 changes state at the beginning of vertical sync during fields one and five.

Analog Outputs

The D/A converter values for 100-percent saturation, 100-percent amplitude color bars are shown in in Figures 4–9.

Luminance (Y) Analog Output

Digital composite luminance information drives the 8-bit D/A converter that generates the analog Y video output (see Figures 4 and 5, and Tables 4 and 5). The Y analog output is designed to drive a 50 Ω load.

Chrominance (C) Analog Output

Digital chrominance information drives the 8-bit D/A converter that generates the analog C video output (see Figures 6 and 7, and Tables 6 and 7). The C analog output is designed to drive a 50 Ω load.

NTSC/PAL Analog Output

Digital composite video information drives the 8-bit D/A converter that generates the composite analog NTSC / PAL video output (see Figures 8 and 9, and Tables 8 and 9). The NTSC/PAL analog output is designed to drive a 50 Ω load.

Circuit Description (continued)

Subcarrier Frequency

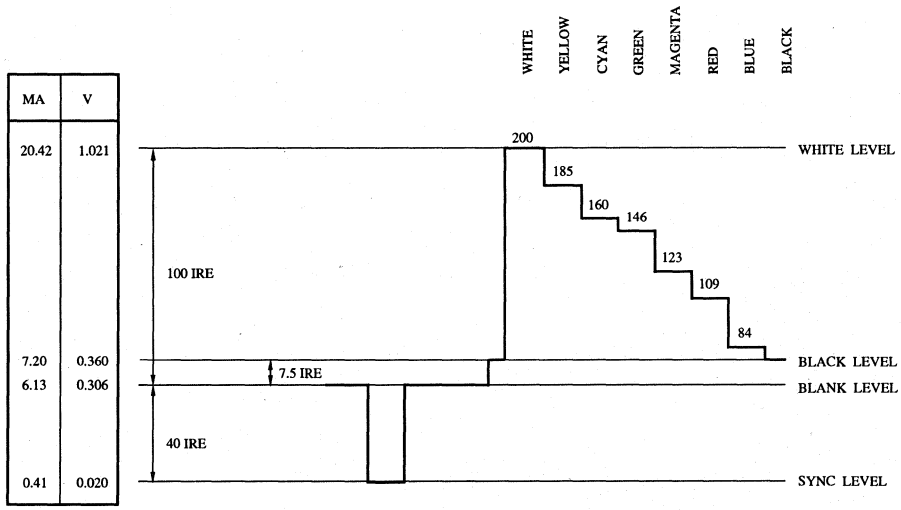
The subcarrier is computed by:

NTSC: FSC = FCLK * [P1 + P2/ (4*HCOUNT)]/2048

PAL: FSC = FCLK * [P1 + (P2 + (67/625)) / (4*HCOUNT)] / 2048

The subcarrier frequency errorwill track the clock frequency error. If the clock has a tolerance of 100 PPM, then the resulting subcarrier will also have a tolerance of 100 PPM. Broadcast specifications for the subcarrier tolerance for NTSC is ±10 Hz, or roughly 3 PPM.

In addition, any jitter on the clock will be reflected in the subcarrier. Thus, care must be taken to provide a clean, stable clock to the Bt855 to produce the highest quality output.



Note: 50 Ω load, VREF = 1.235 V, and RSET = 91 Ω. RS-170 levels and tolerances are assumed on all levels. Saturation is 100 percent, and 100-percent amplitude luminance color bars are shown.

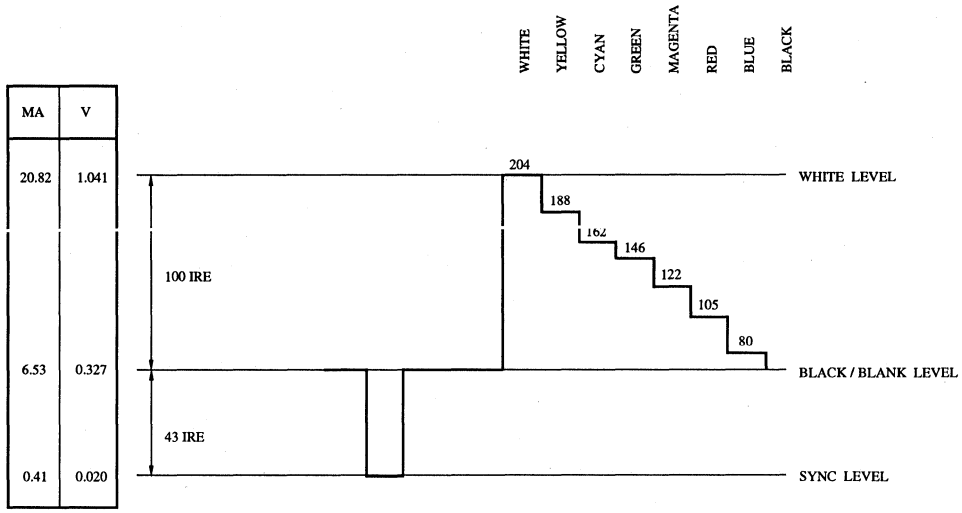
Figure 4. NTSC Y (Luminance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
WHITE	20.42	1	1	200
BLACK	7.2	1	1	70
BLANK	6.13	1	0	60
SYNC	0.41	0	0	4

Note: Typical with VREF = 1.235 V and RSET = 91 Ω.

Table 4. NTSC Y (Luminance) Video Output Truth Table.

Circuit Description (continued)



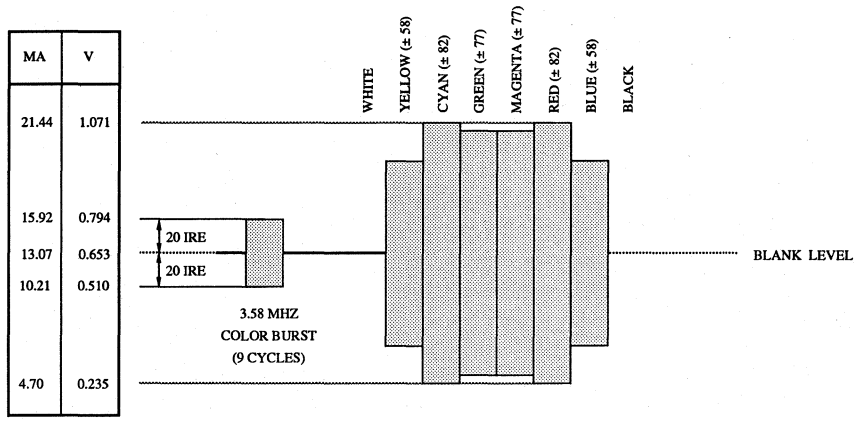
Note: 50 Ω load, VREF = 1.235 V, and RSET = 91 Ω. RS-170 levels and tolerances are assumed on all levels. Saturation is 100 percent, and 100-percent amplitude luminance color bars are shown.

Figure 5. PAL Y (Luminance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
WHITE	20.82	1	1	204
BLACK	6.53	1	1	64
BLANK	6.53	1	0	64
SYNC	0.41	0	0	4

Note: Typical with VREF = 1.235 V and RSET = 91 Ω.

Table 5. PAL Y (Luminance) Video Output Truth Table.



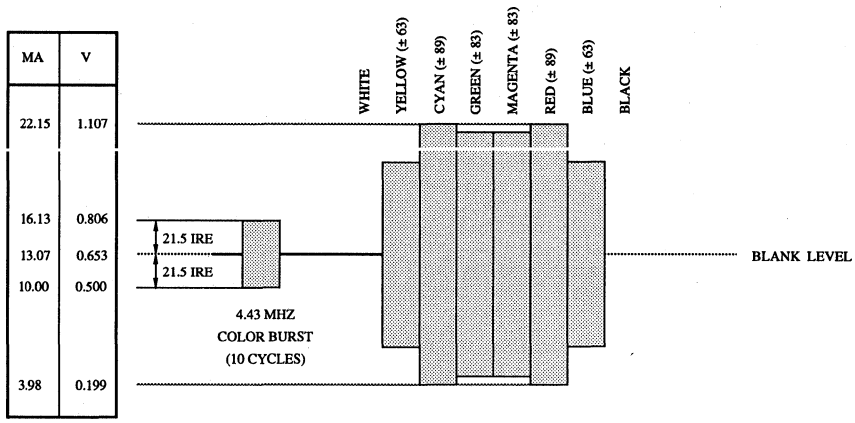
Note: 50 Ω load, VREF = 1.235 V, and RSET 91 Ω. RS-170A levels and tolerances are assumed on all levels. Saturation is 100 percent, and 100-percent amplitude chrominance color bars are shown.

Figure 6. NTSC C (Chrominance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	21.44	x	1	210
Burst (high)	15.92	x	0	156
BLANK	13.07	x	0	128
Burst (low)	10.21	x	0	100
Peak Chroma	4.7	x	1	46

Note: Typical with VREF = 1.235 V and RSET = 91 Ω.

Table 6. NTSC C (Chrominance) Video Output Truth Table.



Note: 50 Ω load, VREF = 1.235 V, and RSET = 91 Ω. PAL levels and tolerances are assumed on all levels. Saturation is 100 percent, and 100-percent amplitude chrominance color bars are shown.

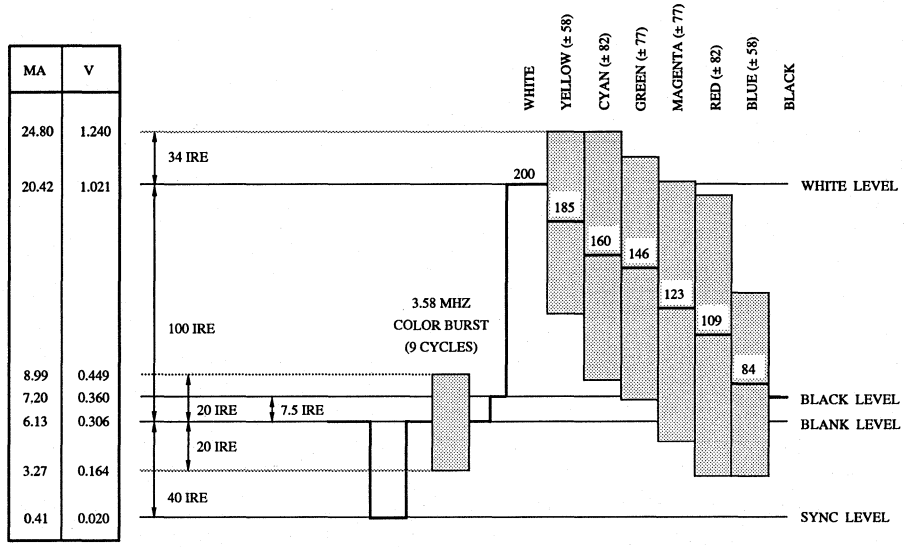
Figure 7. PAL C (Chrominance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	22.15	x	1	217
Burst (high)	16.13	x	0	158
BLANK	13.07	x	0	128
Burst (low)	10	x	0	98
Peak Chroma	3.98	x	1	39

Note: Typical with VREF = 1.235 V and RSET = 91 Ω.

Table 7. PAL C (Chrominance) Video Output Truth Table.

Circuit Description (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET= 91 Ω. RS-170A levels and tolerances are assumed on all levels. Saturation is 100 percent, and 100-percent amplitude color bars are shown.

Figure 8. Composite NTSC Video Output Waveform.

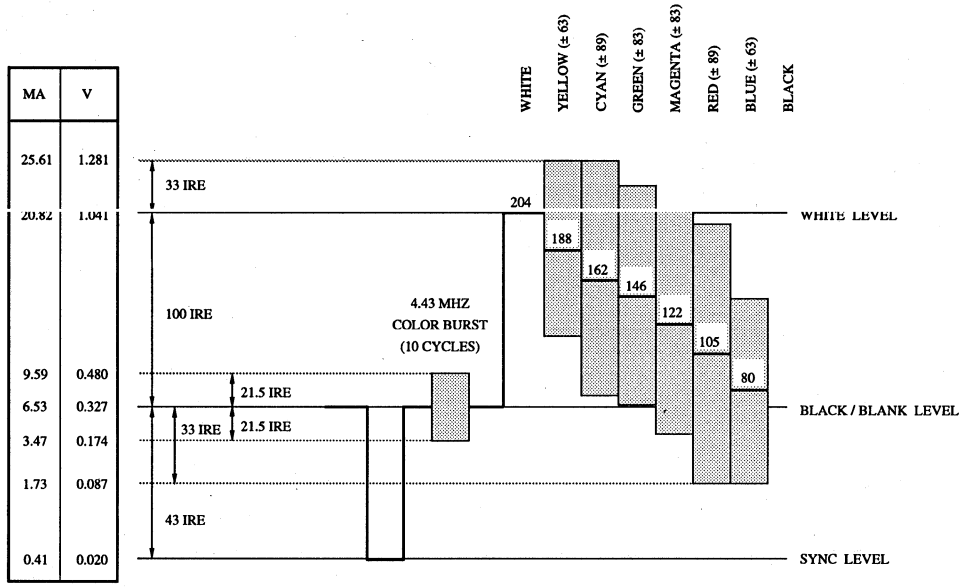
Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	24.80	1	1	243
WHITE	20.42	1	1	200
Burst (high)	8.99	1	0	88
BLACK	7.20	1	1	70
BLANK	6.13	1	0	60
Burst (low)	3.27	1	0	32
Peak Chroma (Note 1)	2.66	1	1	26
SYNC	0.41	0	0	4

Typical with VREF = 1.235 V and RSET = 91 Ω.

Note 1: If command bit CR31 is a logical zero, DAC data values less than 31 are made 31.

Table 8. Composite NTSC Video Output Truth Table.

Circuit Description (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 91 Ω. PAL levels and tolerances are assumed on all levels. Saturation is 100 percent, and 100-percent amplitude color bars are shown.

Figure 9. Composite PAL Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	25.61	1	1	251
WHITE	20.82	1	1	204
Burst (high)	9.59	1	0	94
BLACK	6.53	1	1	64
BLANK	6.53	1	0	64
Burst (low)	3.47	1	0	34
Peak Chroma (Note 1)	1.73	1	1	17
SYNC	0.41	0	0	4

Typical with VREF = 1.235 V and RSET = 91 Ω.

Note 1: If command bit CR31 is a logical zero, DAC data values less than 31 are made 31.

Table 9. Composite PAL Video Output Truth Table.

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR00 is the least significant bit and corresponds to data bus bit D0.

CR07–CR04 Color data input format

(0000) 24-bit true-color RGB (8,8,8)
(0001) 16-bit true-color RGB (6,6,4)
(0010) 16-bit true-color RGB (5,6,5)
(0011) 15-bit true-color RGB (5,5,5)
(0100) 8-bit pseudo-color (red)
(0101) 8-bit pseudo-color (green)
(0110) 8-bit pseudo-color (blue)
(0111) reserved
(1000) reserved
(1001) 24-bit YCrCb (4:4:4)
(1010) 16-bit YCrCb (4:2:2)
(1011) reserved
(1100) reserved
(1101) reserved
(1110) reserved
(1111) reserved

These bits specify the input format of the video data, as detailed in Table 3. The pipeline delay remains unchanged regardless of the mode of operation.

YCrCb data is assumed to be derived from gamma-corrected RGB data. The lookup table RAMs may be used to provide gamma correction (typically 2.2 for NTSC and 2.8 for PAL) when inputting RGB or pseudo-color data. If the lookup table RAMs are being bypassed, RGB input data should be gamma corrected.

CR03–CR02 Reserved

CR01–CR00 Reserved (logical zero)

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR10 is the least significant bit and corresponds to data bus bit D0.

CR17	OL3 read mask (0) force OL3 data to zero (1) pass OL3 data	This bit is logically ANDed with the OL3 input prior to addressing the overlay registers.
CR16	OL2 read mask (0) force OL2 data to zero (1) pass OL2 data	This bit is logically ANDed with the OL2 input prior to addressing the overlay registers.
CR15	OL1 read mask (0) force OL1 data to zero (1) pass OL1 data	This bit is logically ANDed with the OL1 input prior to addressing the overlay registers.
CR14	OL0 read mask (0) force OL0 data to zero (1) pass OL0 data	This bit is logically ANDed with the OL0 input prior to addressing the overlay registers.
CR13	8-bit/6-bit color select (0) 6-bit (1) 8-bit	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle when the MPU is accessing the lookup table RAMs. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles. (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles.) When the Bt855 is in the 6-bit mode, the full-scale output current will be about 1.5-percent lower than when it is in the 8-bit mode. This is because the 2 LSBs of color data are a logical zero in the 6-bit mode.
CR12	Lookup table RAM bypass enable (0) use lookup table RAMs (1) bypass RAMs	This bit specifies whether to bypass the lookup table RAMs and pixel read mask registers. When internal color bar generation is used (CR32 = 1), the lookup table RAMs are automatically bypassed regardless of the value of this bit. The selection does not affect the pipeline delay through the device.
CR11, CR10	Reserved	

Internal Registers (continued)

Command Register_2

This command register may be written to or read by the MPU at any time and is initialized to $F0 following a reset sequence. CR20 is the least significant bit and corresponds to data bus bit D0.

CR27–CR24 Reserved (logical one)

CR23 Reserved (logical zero)

CR22 Software reset

(0) normal operation
(1) reset device

Writing a logical one to this bit resets the device, clearing the pixel pipeline and resetting the command register bits to their initialized state (equivalent to asserting the RESET* input pin). The bit is reset to a logical zero when the software reset sequence is complete.

Following a reset condition, the Bt855 is configured for NTSC operation (square pixels, Master Mode 1) and 24-bit RGB input data format. The lookup table RAMs must be initialized before valid video may be generated.

CR21, CR20 Reserved (logical zero)

Internal Registers (continued)

Command Register_3

This command register may be written to or read by the MPU at any time and is initialized to $12 following a reset sequence. CR30 is the least significant bit and corresponds to data bus bit D0.

CR37–CR34 Output mode select

(0000) NTSC master mode 0
(0001) NTSC master mode 1
(0010) NTSC master mode 2
(0011) NTSC master mode 3
(0100) reserved
(0101) PAL master mode 0
(0110) PAL master mode 1
(0111) PAL master mode 2
(1000) PAL master mode 3
(1001) reserved
(1010) reserved
: :
(1110) reserved
(1111) power-down mode

These bits specify the timing and analog output mode of the Bt855.

Mode (1111) turns power off to the DACs (no current is output) and to the A/D converter, three-states all TTL-compatible outputs, and inhibits clocking to most of the internal circuitry to minimize power consumption. The pixel and control inputs are ignored, and CLOCK_IN is directly output onto CLOCK_OUT. All the control registers and color palette RAMs are still accessible to the MPU. About 1 second is required for the Bt855 to become operational after the power-down mode is disabled.

CR33 Color kill enable

(0) normal operation
(1) disable color information

This bit enables (logical zero) or disables (logical one) color information on the NTSC/PAL and C video outputs.

CR32 Color bar test enable

(0) normal operation
(1) generate color bars

If a logical one is specified, full-screen 100-percent saturated, 75-percent amplitude color bars are generated—consisting of gray, yellow, cyan, green, magenta, red, blue, and black. The first seven colors each occupy 64 pixels of active video each scan line. Black occupies the remaining active pixels each scan line. Color bars may only be generated when the device is configured to operate in 24-bit RGB mode.

CR31 Color level limiting bypass

(0) use level limiting
(1) bypass level limiting

A logical zero enables the NTSC/PAL level limiting circuitry that limits the minimum active composite video levels. Active video values less than 31 (8-bit value) are made 31 (approximately one half the sync height) to avoid possible sync detection problems with downstream video equipment.

CR30 Illegal video flag

(0) reset by MPU
(1) illegal value detected

This bit is set to a logical one if active video generates values less than 31 (8-bit value). The MPU must write a logical zero to this bit to clear it to a logical zero.

Command Register_4

This command register may be written to or read by the MPU at any time and is initialized to $18 following a reset sequence. CR40 is the least significant bit and corresponds to data bus bit D0.

CR47 — UV low-pass filter bypass

(0) use filters
(1) bypass filters

This bit specifies whether to bypass the UV low-pass filters (just after the matrix). Regardless of the selection, there is no change in the pipeline delay.

CR46 — Reserved (logical one)

CR45 — FIELD input/output select

(0) inputs
(1) outputs

This bit specifies whether the FIELD_0 and FIELD_1 pins are inputs (logical zero) or outputs (logical one). In all modes, FIELD_0 and FIELD_1 are three-stated if CR45 is programmed low.

CR44 — CLOCK_OUT output enable

(0) output three-stated
(1) output enabled

A logical zero three-states the CLOCK_OUT pin asynchronously to the pixel clock.

CR43 — Control output enable

(0) output three-stated
(1) output enabled

A logical zero three-states the FIELD_0, FIELD_1, CSYNC*, HSYNC*, and VSYNC* pins, if they are configured as outputs, asynchronously to the pixel clock. *For HSYNC*, VSYNC*, FIELD_0, and FIELD_1, this three-state is independent of the mode of operation. The CSYNC* pin is not internally gated and must be configured by CR43 according to the mode for proper operation of the part. In all modes, FIELD_0 and FIELD_1 are three-stated if CR43 is programmed low.*

CR43: H/L	CSYNC*	V/VSYNC*	H/HSYNC*
mode 0	Q/Z	Z	Z
mode 1	X/Z	X/Z	X/Z
mode 2	Q/Z	Z	Z
mode 3	Q/Z	Q/Z	Q/Z

Z = Three-State
X = State Not Allowed in Mode
Q = Valid Output

CR42–CR41 — Reserved (logical zero)

CR40 — Genlock available status

(0) genlock not available
(1) genlock available

This bit indicates whether the device has genlock support. On the Bt855, this bit is always a logical zero, indicating genlock is not supported. MPU write cycles to this bit are ignored.

Internal Registers (continued)

HCOUNT Register

This 16-bit register specifies the number of pixels per scan line. It is initialized to $030C (780) following a reset condition and may be written to and read by the MPU at any time. The HCOUNT low and high registers are independent and are individually written to and read by the MPU.

The HCOUNT low and high registers are cascaded to form a 16-bit HCOUNT register. The D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. Even values from $0002 (2) to $0FFE (4094) may be specified.

	HCOUNT High				HCOUNT Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

The HCOUNT value is used to automatically calculate many of the horizontal timing parameters. With the falling edge of horizontal sync as a reference, the following are internally calculated:

analog horizontal sync width (50-percent amplitude) = (HCOUNT/16) + (HCOUNT/128) + (HCOUNT/256) + 1

start of color burst (50-percent amplitude) = (HCOUNT/16) + (HCOUNT/64) + (HCOUNT/256) + (HCOUNT/512) + 1

end of color burst (NTSC, 50-percent amplitude) = BURST GATE start value + (HCOUNT/32) + (HCOUNT/128) + 1

end of color burst (PAL, 50-percent amplitude) = BURST GATE start value + (HCOUNT/32) + (HCOUNT/256) + 1

Internal Registers (continued)

P1 and P2 are used to generate the color subcarrier (3.58 MHz for [M] NTSC, 4.43 MHz for [B, D, G, H, I] PAL) from the pixel clock. They must be calculated, and the values must be loaded into the P1 and P2 registers.

P1 Low and High Registers

The P1 low and high registers are cascaded to form a 16-bit P1 register. Values from $0000 (0) to $0400 (1024) may be specified. The 16-bit register is initialized to $0255 (597) following a reset condition and may be written to and read by the MPU at any time. The P1 low and high registers are independent of each other and are individually written to and read by the MPU. The D2–D7 of P1 high are ignored during MPU write cycles and return a logical zero during MPU read cycles.

	P1 High		P1 Low							
Data Bit	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P2 Low and High Registers

The P2 low and high registers are cascaded to form a 16-bit P2 register. Values from $0000 (0) to $1000 (4096) may be specified. The 16-bit register is initialized to $0410 (1040) following a reset condition and may be written to and read by the MPU at any time. The P2 low and high registers are independent and are individually written to and read by the MPU. The D4–D7 of P2 high are ignored during MPU write cycles and return a logical zero during MPU read cycles.

	P2 High				P2 Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P1 and P2 are calculated as follows:

$$\text{(M) NTSC: } \frac{465{,}920}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

$$\text{(4.43) NTSC (Note 1): } \frac{465{,}920}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

$$\text{(B, D, G, H, I) PAL: } \frac{581{,}123.2768}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

$$\text{(N) PAL: } \frac{469{,}507.2768}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

Note 1: (4.43) NTSC is NTSC using a 4.43 MHz subcarrier. It is normally used for standard conversion betweeen PAL and NTSC video signals.

After the appropriate value for HCOUNT is inserted, the result is separated into an integer value (P1) and a fractional value (whose numerator is P2). Table 10 lists some of the common HCOUNT values and the resulting P1 and P2 values. Table 11 lists some of the common blanking intervals.

Internal Registers (continued)

In order to guarantee the highest quality of signal integrity (i.e., meeting the broadcast spec), the following method should be used to determine the P1 and P2 values.

Determine the HCOUNT value by:

NTSC: HCOUNT = (int) (FCLK_desired/15734.264)
PAL: HCOUNT = (int) (FCLK_desired/15625)

Determine P1 by:

NTSC: P1 = (int) [455*2048/(2*HCOUNT)]
PAL: P1 = (int) [1135*2048/(4*HCOUNT)]

Determine P2 by:

NTSC: P2 = 2*455*2048 – P1*4*HCOUNT
PAL: P2 = 1135*2048 – P1*4*HCOUNT + 13

Determine the actual clock frequency by:

NTSC: FCLK_actual = 3579545*2*HCOUNT/455
PAL: FCLK_actual = 4433618.75*HCOUNT/ [(1135/4) + (1/625)]

Typical Application	Total Pixels per Scan Line (HCOUNT)	Active Pixels	4x HCOUNT	P1	P2
13.5 MHz NTSC	858	720	3432	543	104
13.5 MHz PAL	864	720	3456	672	2061
12.27 MHz (square pixels) NTSC	780	640	3120	597	1040
14.75 MHz (square pixels) PAL	944	768	3776	615	2253
14.32 MHz (4x Fsc) NTSC	910	768	3640	512	0
17.72 MHz (4x Fsc) PAL	1135	910	4540	512	0

NTSC refers to (M) NTSC. PAL refers to (B, D, G, H, I) PAL.

Table 10. Typical HCOUNT, P1 (Fsc), and P2 (Fsc) Values.

Typical Application	Sync + Back Porch Blanking (Pixels)	Front Porch Blanking (Pixels)
13.5 MHz NTSC	121	17
13.5 MHz PAL	131	13
12.27 MHz (square pixels) NTSC	118	22
14.75 MHz (square pixels) PAL	145	31
14.32 MHz (4x Fsc) NTSC	120	22
17.72 MHz (4x Fsc) PAL	159	28

NTSC refers to (M) NTSC. PAL refers to (B, D, G, H, I) PAL.

Table 11. Typical BLANK* Input Horizontal Timing.

Pin Descriptions

Pin Name	Description
F/BLANK*	Composite blank control input (TTL compatible). BLANK* is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In all modes, except Master Mode 2, the R0–R7, G0–G7, B0–B7, and OL0–OL3 inputs are ignored while BLANK* is a logical zero. In Master Mode 2, this pin is the F (field) input. This pin is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. This input must be asserted with the proper timing in all modes.
H/HSYNC*	Horizontal sync control input/output (TTL compatible). In Master Mode 0, HSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Mode 1, this pin is ignored. In Master Mode 2, this pin is the H (horizontal blank) input. This pin is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The R0–R7, G0–G7, B0–B7, and OL0–OL3 inputs are ignored while the H or V inputs are a logical one. In Master Mode 3, HSYNC* is an output. HSYNC* is output following the rising edge of CLOCK_IN. As an output, it should drive a maximum of one LS TTL load. Absolute minimum loading should be observed. When HSYNC* is programmed as an input, the period must match the programmed HCOUNT value.
V/VSYNC*	Vertical sync control input/output (TTL compatible). In Master Mode 0, VSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Mode 1, this pin is ignored. In Master Mode 2, this pin is the V (vertical blank) input. The V input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The R0–R7, G0–G7, B0–B7, and OL0–OL3 inputs are ignored while the H or V inputs are a logical one. In Master Mode 3, VSYNC* is an output. VSYNC* is output following the rising edge of CLOCK_IN. As an output, VSYNC* should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
CSYNC*	Composite sync control input/output (TTL compatible). In Master Mode 1, CSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Modes 0, 2, and 3, this pin is ignored.
FIELD_0, FIELD_1	FIELD inputs/outputs (TTL compatible). As inputs, these pins are latched on the rising edge of CLOCK_IN. As outputs, they are output following the rising edge of CLOCK_IN and should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
R0–R7, G0–G7, B0–B7	Pixel inputs (TTL compatible). They are latched on the rising edge of CLOCK_IN. Unused inputs should be connected to GND.
OL0–OL3	Overlay select input (TTL compatible). These inputs specify, on a pixel basis, which overlay color (if any) is to be generated. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. Unused inputs should be connected to GND.
CbFLAG	CbFLAG control input (TTL compatible). When inputting 16-bit YCrCb pixel data, this input indicates whether Cb (logical one) or Cr (logical zero) data is present on the B0–B7 inputs. It is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. If unused, this pin should be connected to GND.
CLOCK_IN	Pixel clock input (TTL compatible). This clock input is output onto the CLOCK_IN pin when enabled by CR43.
CLOCK_OUT	Pixel clock output (TTL compatible). This pin should drive a maximum of one LS TTL load. (Absolute minimum loading should be observed.)

Pin Descriptions (continued)

Pin Name	Description
NTSC/PAL, Y, C	Composite NTSC/PAL, luminance, and chroma current outputs. These high-impedance current sources can drive a 37.5 Ω load (Figure 10 in the PC Board Layout Considerations section).
VREF	Voltage reference input. An external voltage reference must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figure 10. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the NTSC/PAL, Y, and C outputs. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = 1,924 * VREF (V) / Iout (mA)
COMP, NCOMP, YCOMP, CCOMP	Compensation pins. A 0.1 µF ceramic capacitor must be used to bypass each pin (except COMP) to VAA. Each capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. All pins must also be connected together as close to the device as possible.
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as specified in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
RESET*	Reset control input (TTL compatible). A logical zero for a minimum of three pixel clock cycles initializes the device. RESET* must be a logical one for normal operation. It is latched on the rising edge of CLOCK_IN.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions (continued)

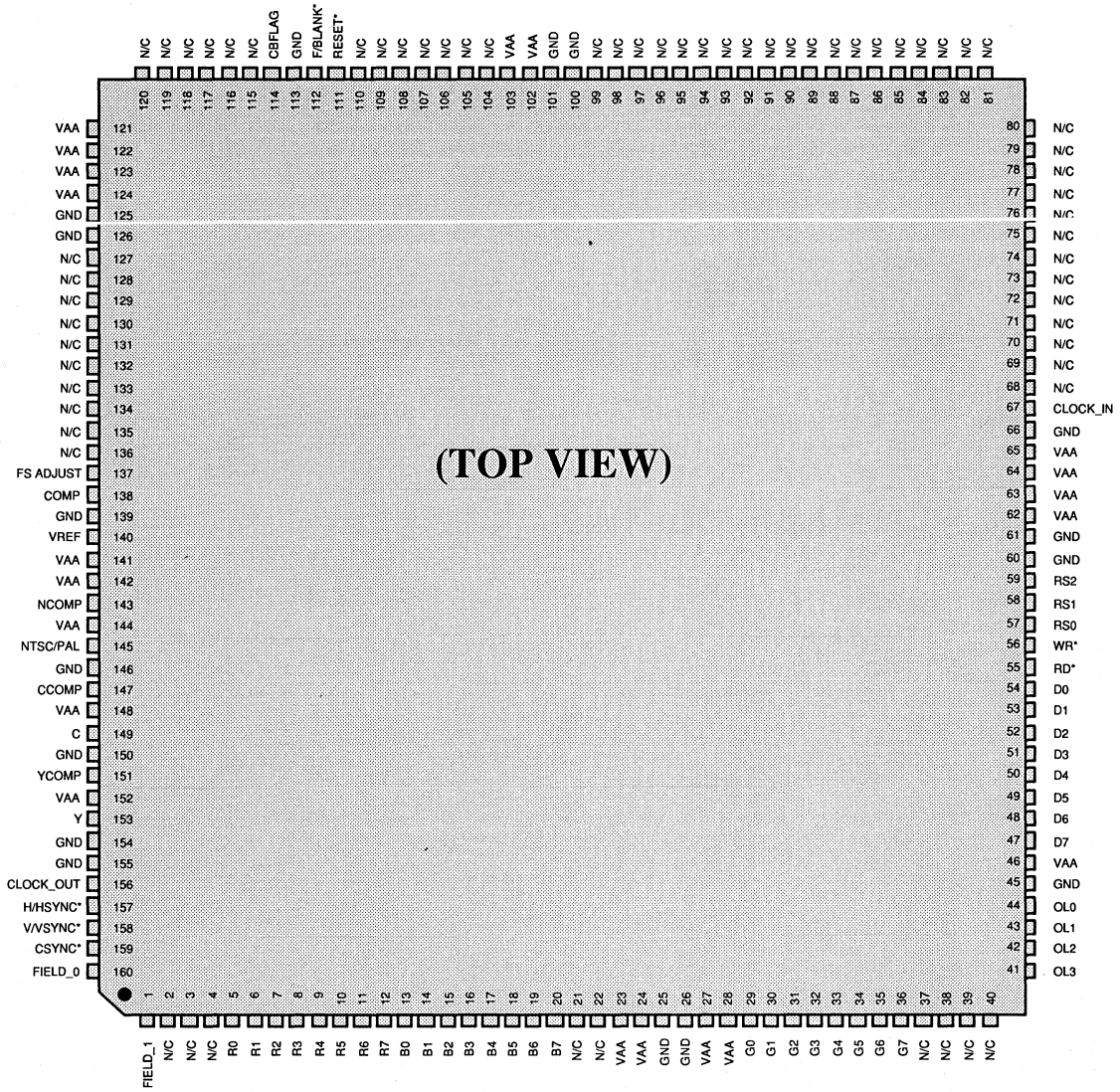
Pin Number	Signal
1	FIELD_1
2	N/C
3	N/C
4	N/C
5	R0
6	R1
7	R2
8	R3
9	R4
10	R5
11	R6
12	R7
13	B0
14	B1
15	B2
16	B3
17	B4
18	B5
19	B6
20	B7
21	N/C
22	N/C
23	VAA
24	VAA
25	GND
26	GND
27	VAA
28	VAA
29	G0
30	G1
31	G2
32	G3
33	G4
34	G5
35	G6
36	G7
37	N/C
38	N/C
39	N/C
40	N/C

Pin Number	Signal
41	OL3
42	OL2
43	OL1
44	OL0
45	GND
46	VAA
47	D7
48	D6
49	D5
50	D4
51	D3
52	D2
53	D1
54	D0
55	RD*
56	WR*
57	RS0
58	RS1
59	RS2
60	GND
61	GND
62	VAA
63	VAA
64	VAA
65	VAA
66	GND
67	CLOCK_IN
68	N/C
69	N/C
70	N/C
71	N/C
72	N/C
73	N/C
74	N/C
75	N/C
76	N/C
77	N/C
78	N/C
79	N/C
80	N/C
81	N/C
82	N/C
83	N/C

Pin Number	Signal
84	N/C
85	N/C
86	N/C
87	N/C
88	N/C
89	N/C
90	N/C
91	N/C
92	N/C
93	N/C
94	N/C
95	N/C
96	N/C
97	N/C
98	N/C
99	N/C
100	GND
101	GND
102	VAA
103	VAA
104	N/C
105	N/C
106	N/C
107	N/C
108	N/C
109	N/C
110	N/C
111	RESET
112	F/BLANK*
113	GND
114	CBFLAG
115	N/C
116	N/C
117	N/C
118	N/C
119	N/C
120	N/C
121	VAA
122	VAA
123	VAA
124	VAA
125	GND
126	GND

Pin Number	Signal
127	N/C
128	N/C
129	N/C
130	N/C
131	N/C
132	N/C
133	N/C
134	N/C
135	N/C
136	N/C
137	FS ADJUST
138	COMP
139	GND
140	VREF
141	VAA
142	VAA
143	NCOMP
144	VAA
145	NTSC/PAL
146	GND
147	CCOMP
148	VAA
149	C
150	GND
151	YCOMP
152	VAA
153	Y
154	GND
155	GND
156	CLOCK_OUT
157	H/HSYNC*
158	V/VSYNC*
159	CSYNC*
160	FIELD_0

Pin Descriptions (continued)



Note: N/C and test pins *must* remain floating.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt855 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Components should be placed as close as possible to the associated pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt855 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt855 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 10. This bead should be located within 3 inches of the Bt855 The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the five groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 47 µF capacitor shown in Figure 10 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pins must be decoupled to VAA, typically with 0.1 µF ceramic capacitors. Low-frequency supply noise will require larger values. The COMP capacitors must be as close as possible to the COMP and VAA pins. Surface-mount ceramic chip capacitors are preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

PC Board Layout Considerations (continued)

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

Digital Signal Interconnect

The digital inputs to the Bt855 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt855 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

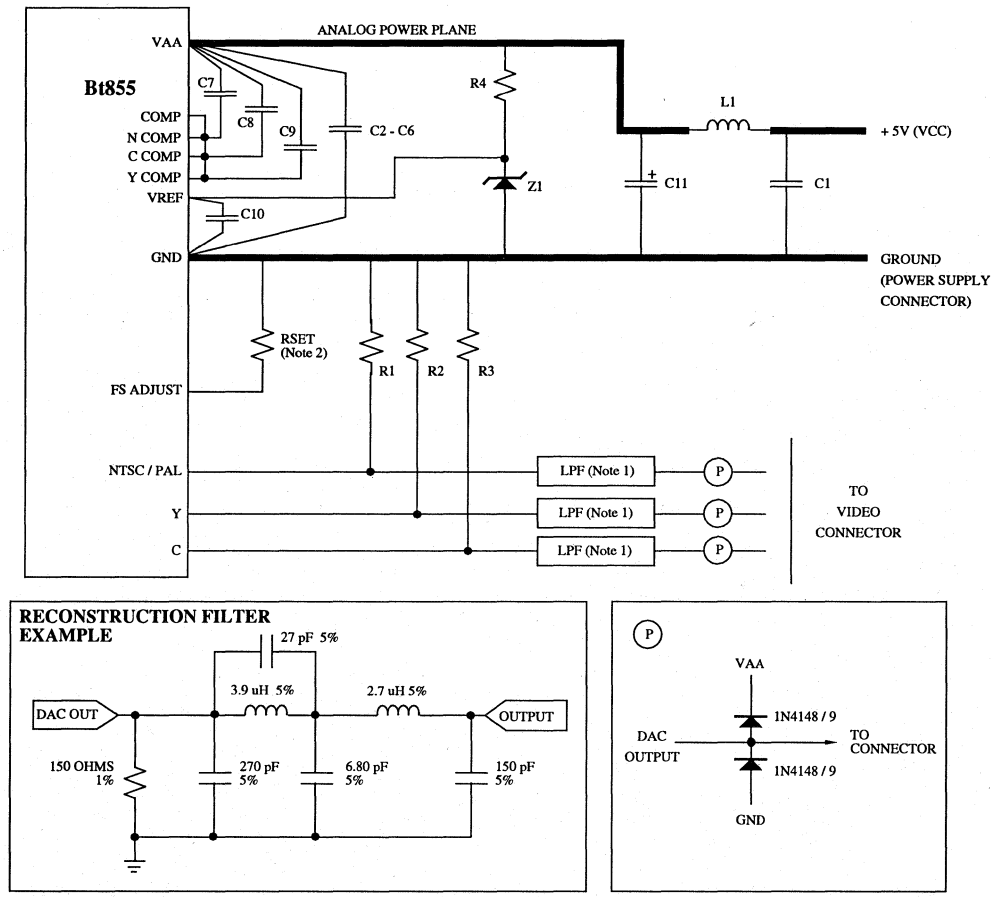
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt855 to minimize reflections. Unused analog outputs should be connected to GND.

Analog Output Protection

The Bt855 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 10 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Note 1: A 150 Ω to 75 Ω impedance matching reconstruction filter is necessary on each output for proper video levels and fidelity. An example filter is illustrated above. For alternative filter designs, call Brooktree Application Engineering at 1-800-VIDEOIC.

Note 2: The value of RSET may have to be varied slightly, depending on the reconstruction filter used, because of the filter insertion loss.

Location	Description	Vendor Part Number
C1–C10	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C11	47 µF tantalum capacitor	Mallory CSR13F476KM
L1	ferrite bead	Fair-Rite 2743001111
R1–R3	150 Ω 1% metal film resistor	Dale CMF-55F
R4	1 kΩ 5% resistor	
RSET	91 Ω 1% metal film resistor	
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt855.

Figure 10. Typical Connection Diagram and Parts List for Parallel 150 Ω/75 Ω Load and 150 Ω to 75 Ω Impedance Matching Reconstruction Filter.

Application Information

UV Low-pass Digital Filters

The transfer function of the 5-tap filters used to low-pass filter the UV color difference video signals is:

$$H(Z) = 80/256 * Z0 + (64/256)*(Z^{-1} + Z^{+1}) + (24/256)*(Z^{-2} + Z^{+2})$$

Full precision is maintained until the final output stage, then rounded to 7 bits plus sign.

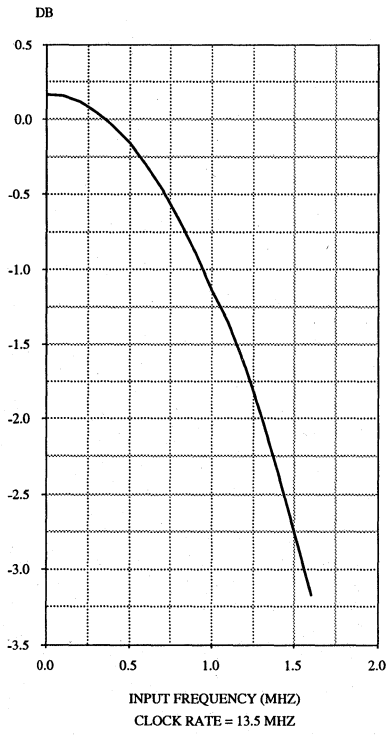
Figure 11 illustrates the pass-band and stop-band characteristics of the low-pass filters.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.



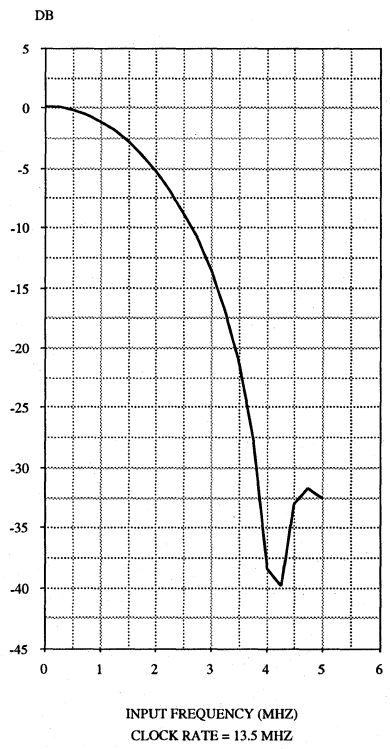


Figure 11. UV Low-pass Digital Filter Pass-Band and Stop-Band Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		50		Ω
External Voltage Reference	VREF	1.14	1.235	1.26	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Video D/A Resolution		8	8	8	Bits
Video D/A Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				5	% Gray Scale
Monotonicity			guaranteed		
Video D/A Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF
Other Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF
Video Analog Outputs					
Output Disabled Current		0	5	50	µA
LSB Size			102		µA
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
C Analog Output					
Output Current (NTSC)					
Peak Chroma Relative to Blank		±7.95	±8.37	±8.79	mA
Blank Level		12.42	13.07	13.72	mA
Peak Burst Relative to Blank		±2.72	±2.86	±3	mA
Output Current (PAL)					
Peak Chroma Relative to Blank		±8.63	±9.08	±9.54	mA
Blank Level		12.42	13.07	13.72	mA
Peak Burst Relative to Blank		±2.91	±3.06	±3.21	mA

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Y Analog Output					
Output Current (NTSC)					
White Level Relative to Black		12.56	13.22	13.88	mA
Black Level Relative to Blank		1.03	1.08	1.13	mA
Blank Level Relative to Sync		5.43	5.72	6	mA
Sync Level		0.39	0.41	0.43	µA
Output Current (PAL)					
White Level Relative to Black		13.57	14.29	15	mA
Black Level Relative to Blank		0	0	0	mA
Blank Level Relative to Sync		5.82	6.13	6.43	mA
Sync Level		0.39	0.41	0.43	µA
NTSC / PAL Analog Output					
Output Current (NTSC)					
White Level Relative to Black		12.56	13.22	13.88	mA
Black Level Relative to Blank		1.03	1.08	1.13	mA
Burst Relative to Blank		±2.71	±2.86	±3	mA
Blank Level Relative to Sync		5.43	5.72	6.01	mA
Sync Level		0.39	0.41	0.43	µA
Output Current (PAL)					
White Level Relative to Black		13.57	14.29	15	mA
Black Level Relative to Blank		0	0	0	mA
Burst Relative to Blank		±2.91	±3.06	±3.21	mA
Blank Level Relative to Sync		5.82	6.13	6.43	mA
Sync Level		0.39	0.41	0.43	µA
VREF Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		tbd		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 76 Ω, VREF = 1.235 V, NTSC operation, and CLOCK_IN frequency = 13.5 MHz. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
RS0–RS2 Setup Time	1	10			ns
RS0–RS2 Hold Time	2	10			ns
RD* Asserted to Data Bus Driven	3	3			ns
RD* Asserted to Data Valid	4			40	ns
RD* Negated to Data Bus 3-Stated	5			20	ns
Read Data Hold Time	6	5			ns
Write Data Setup Time	7	10			ns
Write Data Hold Time	8	10			ns
RD*, WR* Pulse Width Low	9	40			ns
RD*, WR* Pulse Width High	10	6*p15			ns
Analog Output Delay	19			30	ns
Analog Output Rise/Fall Time	20		3		ns
Analog Output Settling Time	21		13		ns
Clock and Data Feedthrough (Note 1)			tbd		dB
Glitch Impulse			tbd		pV - sec
DAC-to-DAC Crosstalk			tbd		dB
Analog Output Skew			0	5	ns
Pipeline Delay					
Blank/Sync into Sync/Field		3	3	3	Clocks
BlankSync into Analog Out		32	32	32	Clocks
VAA Supply Current (Note 2)	IAA		tbd	tbd	mA
Power-Down Mode			tbd	tbd	µA

See test conditions and notes at the end of this section.

AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Y Bandwidth			Fin/2		MHz
Color Difference (UV) Bandwidth			1.3		MHz
Burst Frequency (Note 3)					
(M) NTSC		3.579535	3.579545	3.579555	MHz
(B, D, G, H, I) PAL		4.433614	4.433619	4.433623	MHz
Burst Envelope Rise/Fall Time		8	8	8	Clocks
Burst Cycles					
NTSC		8		9	Fsc Cycles
PAL		9		10	Fsc Cycles
Analog Sync Rise/Fall Time		5	5	5	Clocks
Analog Blank Rise/Fall Time		9	9	9	Clocks
Differential Gain			3		%
Differential Phase			3		Degrees
SNR (per CCIR410)			60		dB
Hue Accuracy (Note 4)			1.5	3	%
Color Saturation Accuracy (Note 4)			1.5	3	%
Residual Subcarrier			–60		dB
Pixel and Control Setup Time	11	0			ns
Pixel and Control Hold Time	12	15			ns
Control Output Delay Time	13			tbd	ns
Control Output Hold Time	14	tbd			ns
CLOCK_IN Rate	Fin				
Normal Operation				18	MHz
Power Down Mode				80	MHz
CLOCK_IN Cycle Time (p15)	15				
Normal Operation		55.5			ns
Power Down Mode		12.5			ns
CLOCK_IN Pulse Width High Time	16	4			ns
CLOCK_IN Pulse Width Low Time	17	4			ns
CLOCK_IN to CLOCK_OUT Delay	18		tbd	tbd	ns

See test conditions and notes at the end of this section.

AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 91 Ω, VREF = 1.235 V, NTSC operation, and CLOCK_IN frequency = 13.5 MHz. Analog output load ≤75 pF; D0–D7, HSYNC*, VSYNC*, and CLOCK_OUT output load ≤75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. See the timing waveforms shown in Figures 12–14.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1k Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Note 3: Burst frequency tolerance is dependent on CLOCK_IN frequency tolerance and jitter. This burst frequency also assumes P1 and P2 registers are correctly configured.

Note 4: Measured using a Matthey VS618H filter. Accuracy is dependent on the pixel clock rate and the color space used.

Timing Waveforms

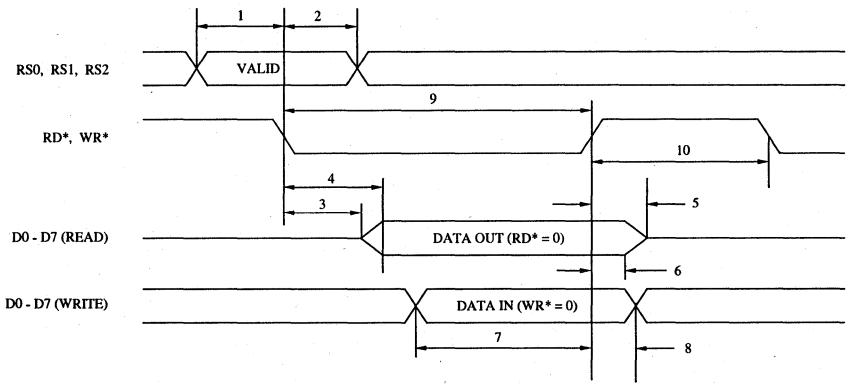
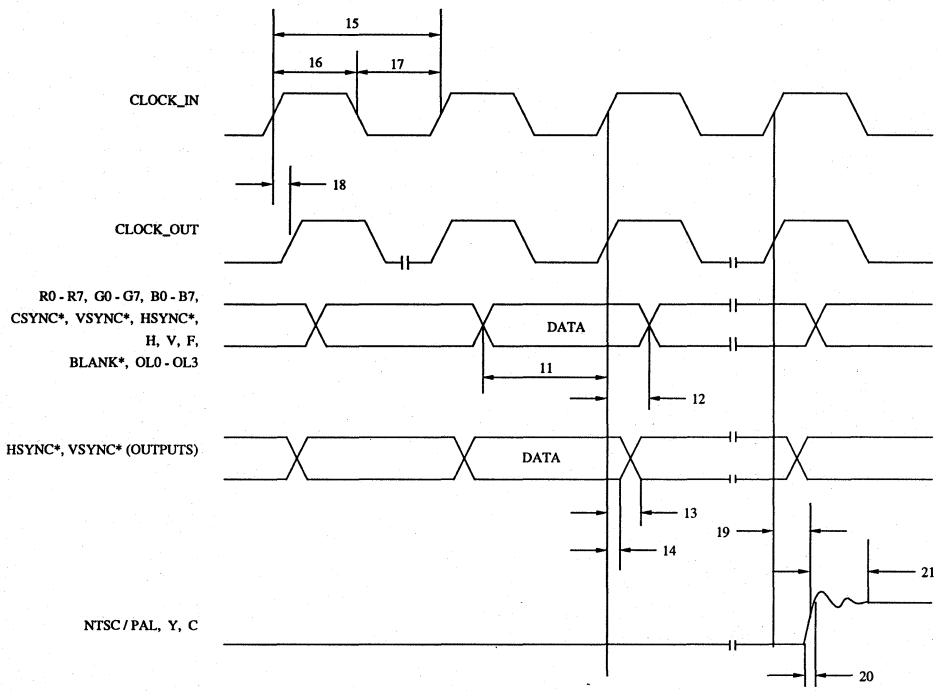


Figure 12. MPU Read/Write Timing.

Timing Waveforms (continued)



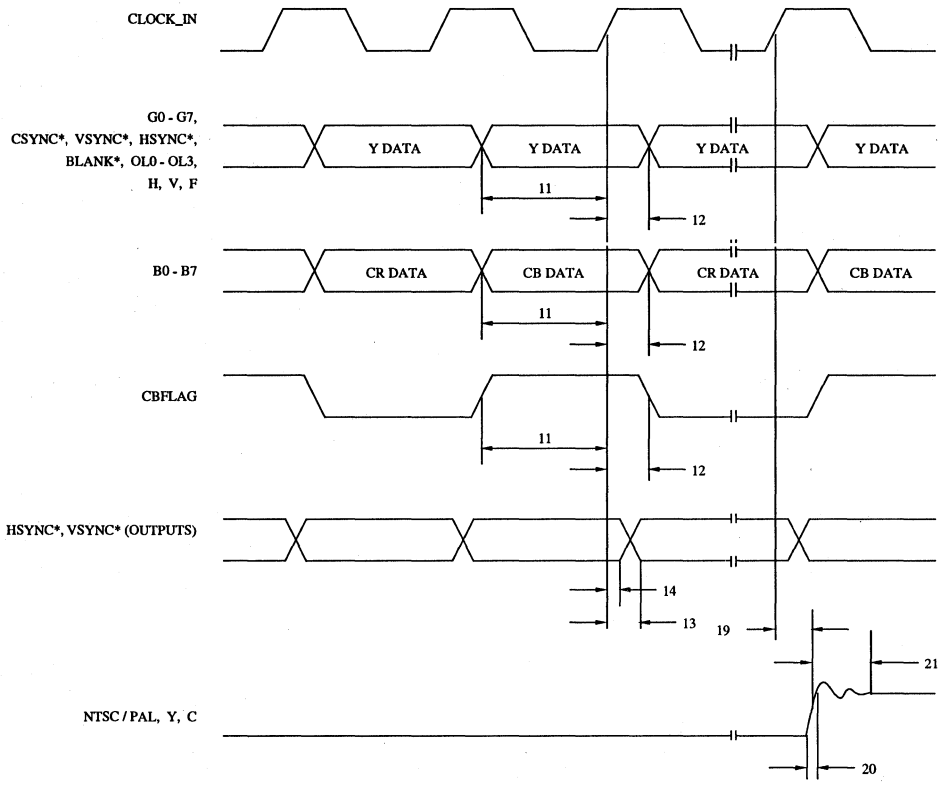
Note 1: Analog output delay is measured from the 50-percent point of the rising edge of CLOCK_IN to the 50-percent point of full-scale transition.

Note 2: Analog settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±2 LSB.

Note 3: Analog output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 13. Video Input/Output Timing (RGB and 24-bit YCrCb Input Formats).

Timing Waveforms (continued)



Note 1: Analog output delay is measured from the 50-percent point of the rising edge of CLOCK_IN to the 50-percent point of full-scale transition.

Note 2: Analog settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±2 LSB.

Note 3: Analog output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 14. Video Input/Output Timing (16-bit YCrCb Input Format).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt855KPF	160-pin Plastic Quad Flatpack	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Bt858

12–18 MHz RGB/YCrCb-to-NTSC/PAL Encoder

3

Distinguishing Features

- NTSC or PAL Composite Video Output
- Separate Y/C Video (S-Video) Outputs
- Interlaced 60 Hz, 525-Line Digital RGB or YCrCb Input (NTSC Output)
- Interlaced 50 Hz, 625-Line Digital RGB or YCrCb Input (PAL Output)
- 4-Field NTSC or 8-Field PAL Generation
- Studio-Quality Outputs
- On-Chip Color Bar Generation
- Graphics/Video Mixing (Pixel Basis)
- Three 256 x 8 Input Lookup Table RAMs
- 15 x 24 Overlay Registers
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 160-pin PQFP Package
- Typical Power Dissipation: 1.25 W
- Pseudo Color/YCrCb Color Keying Capability

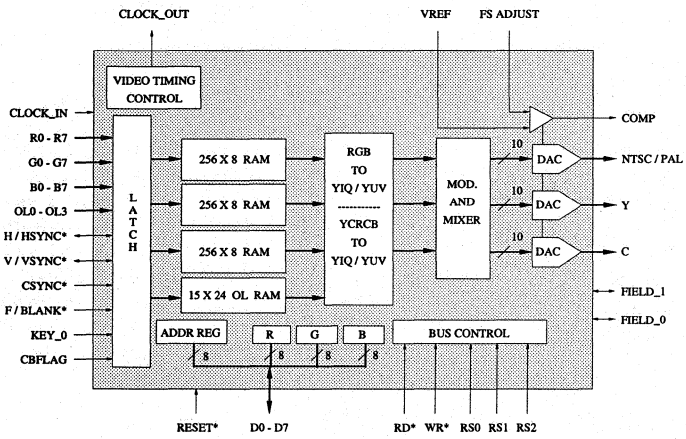
Applications

- Desktop Video
- Video Editing
- Video Presentations

Related Products

- Bt855

Functional Block Diagram



Product Description

The Bt858 is designed specifically for graphics and imaging systems requiring the generation of studio-quality 4-field, 525-line (M) NTSC or 8-field, 625-line (B, D, G, H, I, N) PAL composite or Y/C (S-video) video signals at pixel clock rates of 12–18 MHz. Standards conversion applications may also be generated by 4.43 NTSC. The number of pixels per scan line is programmable, so applications other than 12.27 MHz square pixel NTSC, 13.5 MHz CCIR601, and 14.75 MHz square pixel PAL are easily supported.

Video timing control may be input with horizontal and vertical sync, composite sync, or the CCIR601 H, V, and F control signals. Alternately, the Bt858 may generate the horizontal and vertical sync signals.

The interlaced RGB or YCrCb data is converted to either YIQ (NTSC operation) or YUV (PAL operation). The color difference signals are digitally low-pass filtered to 1.3 MHz and modulated. The rise and fall times of sync, burst envelope, and video blanking are internally controlled to be within composite video specifications.

Analog luminance (Y) and chroma (C) information is available on the Y and C analog outputs for interface to S-video equipment. Composite analog video is output simultaneously onto the NTSC/PAL analog output.

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L858001 Rev. C

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Detailed Block Diagram

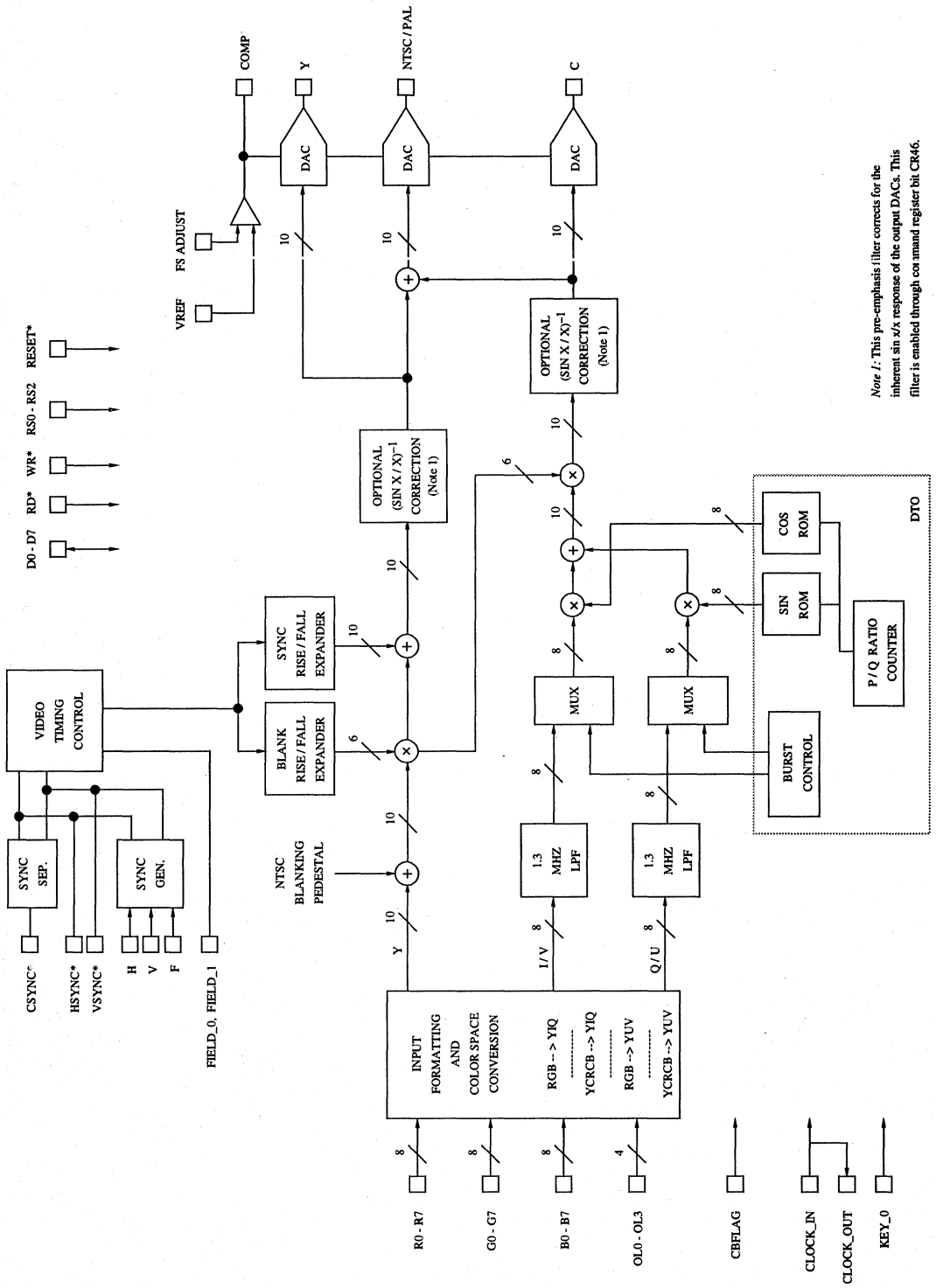


Figure 1. Detailed Block Diagram.

Circuit Description—MPU Interface

MPU Interface

As illustrated in the detailed block diagram (Figure 1), the Bt858 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, or control registers, as shown in Table 1. The 8-bit address register addresses the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode, control register read/write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	control registers

Table 1. Control Input Truth Table.

Circuit Description—MPU Interface (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Control Register Data

To write control register data, the MPU loads the address register (control register read/write mode) with the address of the control register to be read. The MPU performs a write cycle, using RS0–RS2 to select the control registers. After the write cycle, the address register (ADDR0–ADDR7) increments to the next location, which the MPU may write by writing another byte of data. A block of data in consecutive control registers may be written by writing the start address and performing continuous write cycles until the entire block has been written.

Reading Control Register Data

To read control register data, the MPU loads the address register (control register read/write mode) with the address of the control register to be read. The MPU performs a read cycle, using RS0–RS2 to select the control registers. After the read cycle, the address register (ADDR0–ADDR7) increments to the next location, which the MPU may read by reading another byte of data. A block of data in consecutive control registers may be read by writing the start address and performing continuous read cycles until the entire block has been read.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

When the MPU is accessing the control registers, the address register does not reset to $00 following a read or write cycle to address $FF. Data read from reserved locations returns invalid data.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. To reduce noticeable sparkling on the analog outputs during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles (or Y, Cr, and Cb read/write cycles), the address register has 2 additional bits (ADDRa, ADDRb) that count modulo three, as specified in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle, (ADDR0–7), are accessible to the MPU. These bits address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When the MPU is writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input (R0, G0, and B0). Bit D0 also corresponds to data bus bit D0.

Note: The pixel read mask register is not initialized upon power-up. The user must initialize this register for proper operation.

Circuit Description—MPU Interface (continued)

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	0	1	red/Cr value
	01	x	0	1	green/Y value
	10	x	0	1	blue/Cb value
ADDR0–7 (counts binary)	$00–$FF	0	0	1	color palette RAMs
	$x0	1	0	1	reserved
	$x1	1	0	1	overlay color 1
	:	:	:	:	:
	$xF	1	0	1	overlay color 15
	$00	1	1	0	command register_0
	$01	1	1	0	command register_1
	$02	1	1	0	command register_2
	$03	1	1	0	command register_3
	$04	1	1	0	command register_4
	$05	1	1	0	reserved ($00)
	$06	1	1	0	P1 low register (Note 1)
	$07	1	1	0	P1 high register (Note 1)
	$08	1	1	0	P2 low register (Note 1)
	$09	1	1	0	P2 high register (Note 1)
	$0A	1	1	0	Fsc phase adjust low register
	$0B	1	1	0	Fsc phase adjust high register
	$0C	1	1	0	HCOUNT low register
	$0D	1	1	0	HCOUNT high register
	$0E	1	1	0	color key_0 register
	$0F	1	1	0	color mask_0 register

Note 1: Writing to any of these locations automatically resets the timing circuity.

Overlay data may contain either RGB or YCrCb data, depending on the pixel input mode.

Table 2. Address Register (ADDR) Operation.

Overlays

The OL0–OL3 inputs select overlays and have priority over the pixel data. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the R0–R7, G0–G7, and B0–B7 pixel data. Overlay data must be in the same color space as the pixel data, and the overlay palette data must be in 2's complement format.

OL3–OL0	Color Selected
0000	pixel input port
0001	overlay color 1
:	:
1111	overlay color 15

24-bit RGB Input Mode (8, 8, 8)

The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN.

The R0–R7 inputs address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

16-bit RGB Input Mode (5, 6, 5)

The OL0–OL3, R0–R7, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The B0–B7 inputs are ignored.

The R3–R7 inputs address the lower 32 locations of the red color palette RAM. The G5–G7 inputs and R0–R2 address the lower 64 locations of the green color palette RAM. The G0–G4 inputs address the lower 32 locations of the blue color palette RAM.

Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

16-bit RGB Input Mode (6, 6, 4)

The OL0–OL3, R0–R7, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The B0–B7 inputs are ignored.

The R2–R7 inputs address the lower 64 locations of the red color palette RAM. The G4–G7, R0, and R1 inputs address the lower 64 locations of the green color palette RAM. The G0–G3 inputs address the lower 16 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

15-bit RGB Input Mode (5, 5, 5)

The OL0–OL3, R0–R6, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The R7 and B0–B7 inputs are ignored.

The R2–R6 inputs address the lower 32 locations of the red color palette RAM. The G5–G7, R0, and R1 inputs address the lower 32 locations of the green color palette RAM. The G0–G4 inputs address the lower 32 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

Circuit Description—Pixel Input Formats (continued)

24-bit YCrCb Mode

The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. The Y0–Y7 are input via G0–G7, Cr0–Cr7 are input via R0–R7, and Cb0–Cb7 are input via B0–B7. The Y0, Cr0, and Cb0 are the least significant bits. The Y addresses the green color palette RAM, Cr addresses the red color palette RAM, and Cb addresses the blue color palette RAM. Each lookup table RAM provides 8 bits of information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation). Before addressing the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation), Y has an input range of 16–235. Values less than 16 are made 16, and values greater than 235 are made 235. The Cr and Cb have an input range of 16–240 with 128 equal to zero. Values less than 16 are made 16, and values greater than 240 are made 240.

If overlay information is being displayed (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of YCrCb color information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation).

16-bit YCrCb Mode

The OL0–OL3, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. The R0–R7 inputs are ignored. The Y0–Y7 are input via G0–G7, and multiplexed Cr and Cb data is input via the B0–B7 inputs, as specified in Table 3. The Y0, Cr0, and Cb0 inputs are the least significant bits.

The CbFLAG input is used to indicate when Cb data is present on the B0–B7 inputs. While CbFLAG is a logical one, Cb data is latched; while CbFLAG is a logical zero, Cr data is latched. CbFLAG is latched on the rising edge of CLOCK_IN.

The 16-bit YCrCb (4:2:2) data is converted to 24-bit YCrCb (4:4:4) with a 2-tap interpolation filter to generate the missing Cr and Cb values as follows. The original Cr and Cb values pass through unchanged.

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Y addresses the green color palette RAM, Cr addresses the red color palette RAM, and Cb addresses the blue color palette RAM. Each lookup table RAM provides 8 bits of information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation). Before addressing the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation), Y has an input range of 16–235. Values less than 16 are made 16, and values greater than 235 are made 235. The Cr and Cb have an input range of 16–240 with 128 equal to zero. Values less than 16 are made 16, and values greater than 240 are made 240.

If overlay information is being displayed (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of YCrCb color information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation).

Pseudo-Color Mode

The R0–R7, G0–G7, or B0–B7 inputs (as specified by command bits CR04–CR07) address all three lookup table RAMs simultaneously, generating 24 bits of color information. The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

Internal Color Bar Generator

A color bar test pattern output can be internally generated by the device when it is configured for 24-bit RGB operation. This is enabled by bit CR32 in Command Register_3. The bars are 100 percent saturated, 75 percent amplitude consisting of gray, yellow, cyan, green, magenta, red, blue, and black. They fill the entire screen vertically, and the first seven colors occupy 64 pixels each, horizontally along a scan line. Black occupies the remaining active pixels on each scan line.

Circuit Description—Pixel Input Formats (continued)

RGB Inputs	24-bit RGB (8, 8, 8) Mode	16-bit RGB (5, 6, 5) Mode	16-bit RGB (6, 6, 4) Mode	15-bit RGB (5, 5, 5) Mode	24-bit YCrCb Mode	16-bit YCrCb Mode	Pseudo-Color Mode
R7	R7	R4	R5	x	Cr7	(P7)	P7
R6	R6	R3	R4	R4	Cr6	(P6)	P6
R5	R5	R2	R3	R3	Cr5	(P5)	P5
R4	R4	R1	R2	R2	Cr4	(P4)	P4
R3	R3	R0	R1	R1	Cr3	(P3)	P3
R2	R2	G5	R0	R0	Cr2	(P2)	P2
R1	R1	G4	G5	G4	Cr1	(P1)	P1
R0	R0	G3	G4	G3	Cr0	(P0)	P0
G7	G7	G2	G3	G2	Y7	Y7	P7
G6	G6	G1	G2	G1	Y6	Y6	P6
G5	G5	G0	G1	G0	Y5	Y5	P5
G4	G4	B4	G0	B4	Y4	Y4	P4
G3	G3	B3	B3	B3	Y3	Y3	P3
G2	G2	B2	B2	B2	Y2	Y2	P2
G1	G1	B1	B1	B1	Y1	Y1	P1
G0	G0	B0	B0	B0	Y0	Y0	P0
B7	B7	x	x	x	Cb7	Cb7 / Cr7	P7
B6	B6	x	x	x	Cb6	Cb6 / Cr6	P6
B5	B5	x	x	x	Cb5	Cb5 / Cr5	P5
B4	B4	x	x	x	Cb4	Cb4 / Cr4	P4
B3	B3	x	x	x	Cb3	Cb3 / Cr3	P3
B2	B2	x	x	x	Cb2	Cb2 / Cr2	P2
B1	B1	x	x	x	Cb1	Cb1 / Cr1	P1
B0	B0	x	x	x	Cb0	Cb0 / Cr0	P0

Table 3. Data Input Formats.

Mixed Pseudo-Color/YCrCb Mode

In this mode, 8 bits of pseudo-color data are input via the R0–R7 inputs. The data addresses all three lookup table RAMs simultaneously, generating 24 bits of RGB color information. The RGB data drives the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

Sixteen bits of 4:2:2 YCrCb digital video are input via the G0–G7 and B0–B7 inputs. (The input timing is the same as that for 16-bit YCrCb mode.) The 16-bit YCrCb (4:2:2) data is converted to 24-bit YCrCb (4:4:4) with a 2-tap interpolation filter to generate the missing Cr and Cb values as follows. (The original Cr and Cb values pass through unchanged.)

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

The resulting YCrCb data drives the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix(PAL operation). YCrCb data does not address the lookup table RAMs.

If the OL0–OL3 inputs are not (0000), the overlay color is output rather than the result of the mixed pseudo-color and YCrCb data (because overlays always take priority).

External Key Switching

The KEY_0 input, in conjunction with command bits CR00 and CR01, determine whether the pseudo-color data or the YCrCb data is selected to be used.

KEY_0 Input	CR00, CR01	Selected Source
0	1, 1	pseudo-color data
0	1, 0	YCrCb data
1	1, 1	YCrCb data
1	1, 0	pseudo-color data
x	0, 0	pseudo-color data
x	0, 1	YCrCb data

KEY_0 is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The KEY_0 input may change on a pixel basis.

The KEY_0 input is ignored unless the command bits CR04–CR07 equal (1100). KEY_0 is also ignored during blanking intervals.

Internal Color Key Switching

The Bt858 also generates an internal COLOR KEY_0 control signal, determined by the color key_0 and color mask_0 registers. For a programmed pseudo color, the COLOR KEY_0 control signal will be either a logical one or a logical zero coincident with the specified color being input on the R0–R7 inputs.

CR25, CR24	Color Key_0 Match	Selected Source
0, 0	yes	YCrCb data
0, 0	no	pseudo-color data
0, 1	yes	pseudo-color data
0, 1	no	YCrCb data
1, x	x	pseudo-color data

The COLOR KEY_0 control signal is pipelined to maintain synchronization with the pixel data.

If either the external color key signal (KEY_0) or the internal color key selects the YCrCb data, YCrCb data is selected. This data format is given in Table 3.

Circuit Description—Video Timing

General Video Timing

The Bt858 is designed to accept and output interlaced video to conform to the NTSC or PAL timing specifications. Interlaced 60 Hz, 525-line digital RGB or YCrCb input will produce standard analog NTSC outputs. Interlaced 50 Hz, 625-line digital RGB or YCrCb input will produce standard analog PAL output. Nonstandard line counts in PAL or NTSC modes are not supported.

The Bt858 automatically calculates the width of the analog horizontal sync pulses, and the start and end of color burst. It automatically disables color burst on appropriate scan lines and automatically generates serration and equalization pulses on appropriate scan lines.

In addition, the rise and fall times of sync, blanking, and the burst envelope are internally controlled to conform to the composite video specifications.

The user must only provide information on the number of pixels per scan line (via the HCOUNT register), and program the P1 and P2 registers to generate the correct color subcarrier frequency for a given pixel clock rate.

During NTSC operation, color burst information is automatically disabled on scan lines 1–6, 261–269, and 523–525, inclusively.

During PAL operation, color burst information is automatically disabled on scan lines 1–6, 310–318, and 622–625 during fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is automatically disabled on scan lines 1–5, 311–319, and 623–625, inclusively.

Master Mode 0

External horizontal sync (HSYNC*), vertical sync (VSYNC*), and composite blanking (BLANK*) must be supplied to the Bt858. HSYNC*, VSYNC*, and BLANK* are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an input and is ignored.

CR43 programmed low will three-state CSYNC*, HSYNC*, and VSYNC*. CR43 programmed high will enable CSYNC* as a valid composite sync output, but HSYNC* and VSYNC* will still be internally gated to three-state.

Coincident falling edges of the HSYNC* and VSYNC* input indicates the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field and is ignored.

Only the falling edges of HSYNC* and VSYNC* are used. HSYNC* need not be the width of the analog horizontal sync pulse desired. VSYNC* need not be the width of the analog vertical sync pulse desired and must not contain serration or equalization pulses.

Figures 2 and 3 illustrate the video timing for NTSC and PAL. Nonstandard NTSC line numbering is used in Figure 2.

Vertical Timing

Coincident falling edges of VSYNC* and HSYNC* reset the 10-bit vertical counter to $001. (The number one scan line is the first scan line of the vertical sync interval at the beginning of an odd field.) The vertical counter increments on the falling edge of HSYNC*.

The Bt858 will generate 525 scan lines (NTSC operation) or 625 scan lines (PAL operation) per frame, 2:1 interlaced. The 10-bit vertical counter is also reset to $001 upon reaching a count of 525 (NTSC) or 625 (PAL).

Horizontal Timing

The falling edge of HSYNC* resets a 12-bit horizontal counter to $001. The horizontal counter increments on the rising edge of CLOCK_IN. The counter value is compared to various internal values automatically calculated by the device to determine when to start and stop various control signals (such as horizontal sync and burst gate).

The 12-bit horizontal counter is also reset to $001 upon reaching the count specified by HCOUNT.

NTSC Blanking

The BLANK* input specifies when to output active video. Blanking takes place automatically (regardless of the value of BLANK*) for the entire scan line at the beginning of scan lines 1–17, 261–279, and 523–525, inclusively.

On scan line 260 (where the first half of the scan line contains active video), the Bt858 automatically blanks the last half of the scan line regardless of the value of BLANK*. On scan line 280 (where the last half of the scan line contains active video), the Bt858 automatically blanks the first half of the scan line regardless of the value of BLANK*.

On the remaining scan lines, BLANK* specifies when to display active video. The P2 Low and High Register section contains further information.

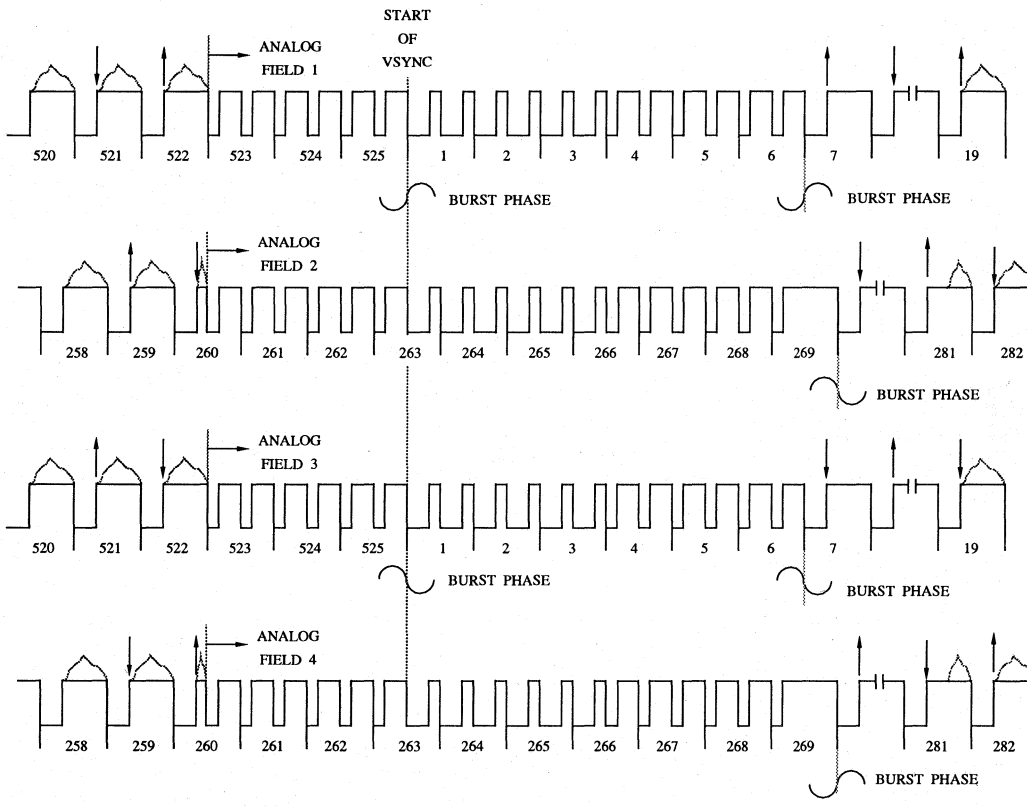
Circuit Description—Video Timing (continued)

PAL Blanking

The BLANK* input specifies when to output active video. Blanking takes place automatically (regardless of the value of BLANK*) for the entire scan line at the beginning of scan lines 1–22, 311–335, and 624–625, inclusively.

On scan line 623 (where the first half of the scan line contains active video), the Bt858 automatically blanks the last half of the scan line regardless of the value of BLANK*. On scan line 23 (where the last half of the scan line contains active video), the Bt858 automatically blanks the first half of the scan line regardless of the value of BLANK*.

On the remaining scan lines, BLANK* specifies when to display active video. The P2 Low and High Register section contains further information.



BURST BEGINS WITH POSITIVE HALF-CYCLE
BURST PHASE = REFERENCE PHASE = 180° RELATIVE TO B - Y

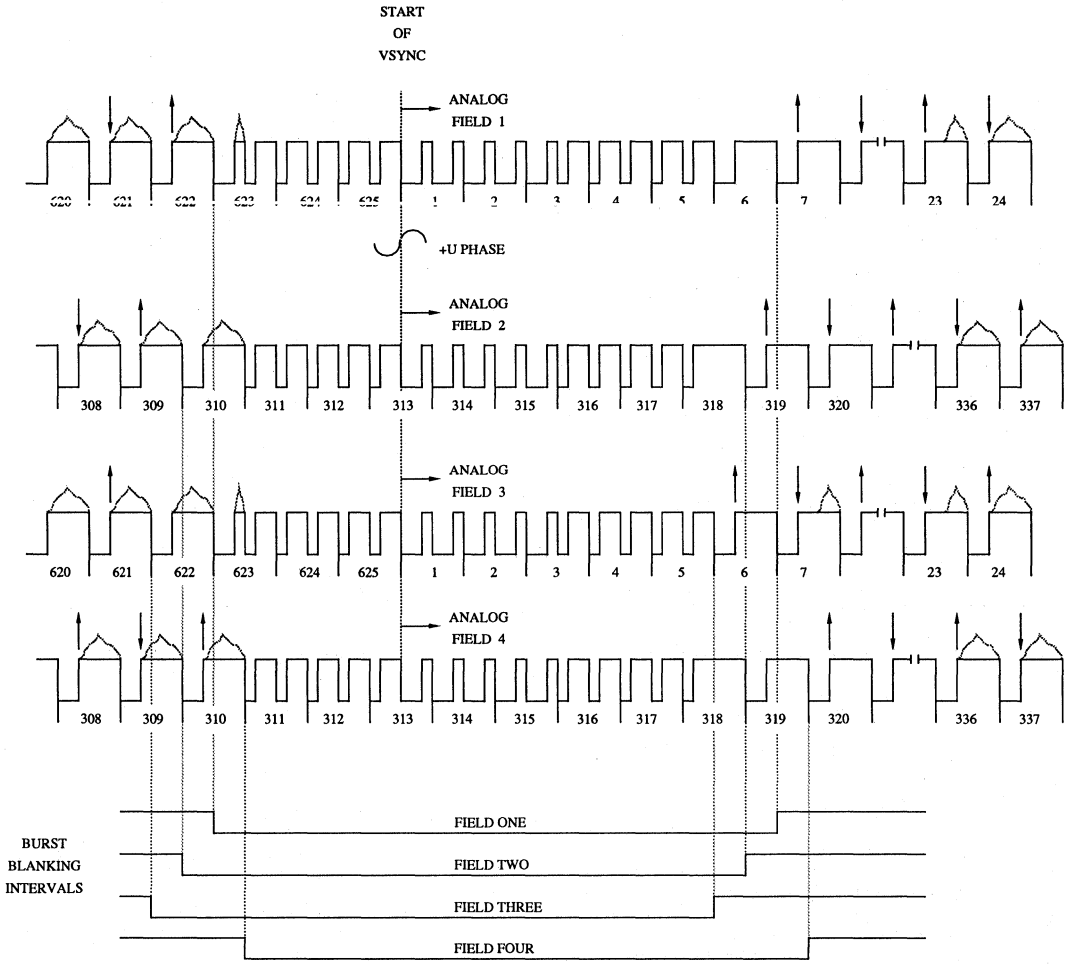
BURST BEGINS WITH NEGATIVE HALF-CYCLE
BURST PHASE = REFERENCE PHASE = 180° RELATIVE TO B - Y

FIELD_0 PIN	
0	FIELD ONE / TWO
1	FIELD THREE / FOUR

To simplify the implementation, the line numbering does not match that used in standard practice for NTSC video signals.

Figure 2. NTSC Video Timing.

Circuit Description—Video Timing (continued)



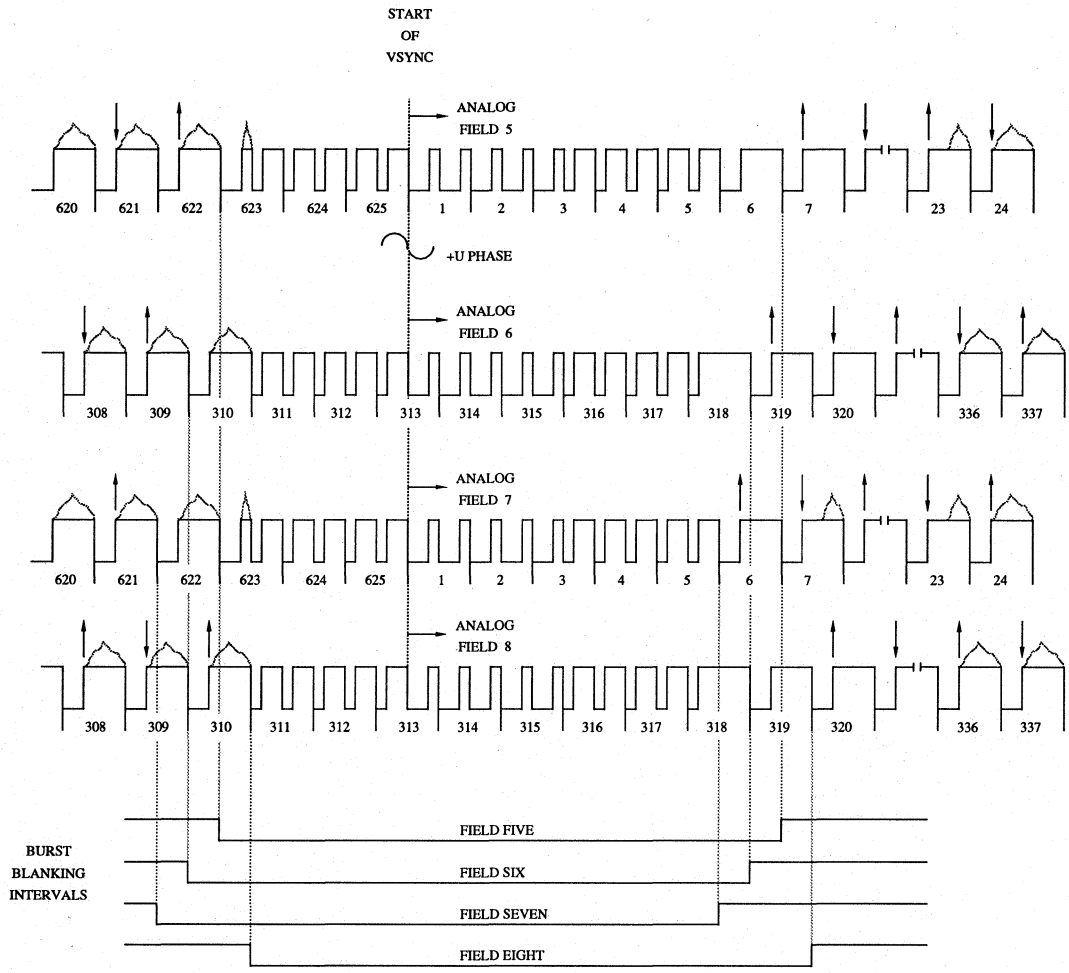
BURST PHASE = REFERENCE PHASE = 135° RELATIVE TO U
PAL SWITCH = 0, +V COMPONENT

BURST PHASE = REFERENCE PHASE + 90° = 225° RELATIVE TO U
PAL SWITCH = 1, –V COMPONENT

FIELD_1 PIN	FIELD_0 PIN	
0	0	FIELD ONE / TWO
0	1	FIELD THREE / FOUR
1	0	FIELD FIVE / SIX
1	1	FIELD SEVEN / EIGHT

Figure 3a. PAL Video Timing.

Circuit Description—Video Timing (continued)



BURST PHASE = REFERENCE PHASE = 135° RELATIVE TO U
PAL SWITCH = 0, +V COMPONENT

BURST PHASE = REFERENCE PHASE + 90° = 225° RELATIVE TO U
PAL SWITCH = 1, –V COMPONENT

FIELD_1 PIN	FIELD_0 PIN	
0	0	FIELD ONE / TWO
0	1	FIELD THREE / FOUR
1	0	FIELD FIVE / SIX
1	1	FIELD SEVEN / EIGHT

Figure 3b. PAL Video Timing (continued).

Circuit Description—Video Timing (continued)

Master Mode 1

External composite sync (CSYNC*) and composite blanking (BLANK*) must be supplied to the Bt858. CSYNC* and BLANK* are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The HSYNC*/H and VSYNC*/V pins are configured as outputs and three-stated. CR43 must be set low, three-stating all pins CSYNC*, HSYNC*, and VSYNC*.

The composite sync (CSYNC*) information is separated into horizontal and vertical sync information internally. When the horizontal and vertical sync information is separated from the CSYNC* signal, the functionality and timing are the same as that for Master Mode 0.

In this instance, CSYNC* must contain the proper serration and equalization pulses during the vertical retrace intervals for proper operation.

Vertical Timing

If the previous scan line samples of CSYNC* (at one-fourth HCOUNT and three-fourths HCOUNT) were both a logical one and the current scan line sample of CSYNC* (at one-fourth HCOUNT) is a logical zero, it is assumed to be the beginning of an odd field, and the 10-bit vertical counter is reset to $001.

The 10-bit vertical counter is also reset to $001 upon reaching a count of 525 (NTSC operation) or 625 (PAL operation).

Horizontal Timing

After a falling edge of CSYNC* (three-fourths HCOUNT), clock cycles must pass before the next falling edge of CSYNC* is interpreted as a horizontal sync. This filters out any serration and equalization pulses from the composite sync signal. Each gated falling edge resets the horizontal counter to $001.

Master Mode 2

In this mode of operation, the Bt858 is designed to be clocked at 13.5 MHz for digital component video (i.e., CCIR601) applications that use the H (horizontal blanking), V (vertical blanking), and F (even/odd field) control signals.

External horizontal blank (H), vertical blank (V), and even/odd field (F) information must be supplied to the Bt858. The H, V, and F pins are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While either the H or V input is a logical one, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an output and three-stated.

As in Master Mode 0, H and V are internally gated to three-state, and CR43 configures only CSYNC* as an unused input or a valid CSYNC* output.

The horizontal counter is reset to $001, 63 clock cycles after each rising edge of H (horizontal blanking).

The F (field) input is sampled by horizontal sync. When a falling edge of the F input (while both the H and V inputs are a logical one) has been detected, the vertical counter is reset to $001. Thus, while F is a logical zero, an odd field is generated; while F is a logical one, an even field is generated.

The remaining functionality is the same as that for Master Mode 0.

Master Mode 3

Master Mode 3 is similar to Master Mode 0, except that the Bt858 generates and outputs horizontal sync (HSYNC*) and vertical sync (VSYNC*). Composite blanking (BLANK*) must be supplied to the Bt858. HSYNC* and VSYNC* are output following the rising edge of CLOCK_IN. HSYNC* and VSYNC* are asserted for one clock cycle when the horizontal and vertical counters overflow after reaching the value of HCOUNT, and 525 (NTSC) or 625 (PAL).

Coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

BLANK* is an input. It is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an input and is ignored.

FIELD_0 and FIELD_1 Pins

The FIELD_0 and FIELD_1 pins, in conjunction with the HSYNC* and VSYNC* timing relationship (or the F input if the BLANK* input is not required), determine which one of four fields (NTSC) or eight fields (PAL) is being generated.

Even or odd fields may be determined by the HSYNC* and VSYNC* timing relationship. Coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

Circuit Description—Video Timing (continued)

NTSC

If command bit CR45 is a logical zero, the FIELD_0 pin is configured as an input and is latched on the rising edge of CLOCK_IN. The FIELD_0 pin indicates whether to generate fields one and two (logical zero) or fields three and four (logical one) (see Figure 4). As an input, the FIELD_0 pin should change state only at the beginning of vertical sync during fields one and three. The FIELD_1 pin is configured as an input and is ignored.

If command bit CR45 is a logical one, the FIELD_0 pin is configured as an output, and is output following the rising edge of CLOCK_IN. The FIELD_0 pin indicates whether fields one and two (logical zero) or fields three and four (logical one) are being generated. As an output, the FIELD_0 pin changes state at the beginning of vertical sync during fields one and three. The FIELD_1 pin is configured as an input and is ignored.

PAL

If command bit CR45 is a logical zero, the FIELD_0 and FIELD_1 pins are configured as inputs and are latched on the rising edge of CLOCK_IN. The FIELD_0 and FIELD_1 pins indicate which field to generate, as shown in Figure 5.

As an input, the FIELD_0 pin should change state only at the beginning of vertical sync during fields one, three, five, and seven. The FIELD_1 pin should change state only at the beginning of vertical sync during fields one and five.

If command bit CR45 is a logical one, the FIELD_0 and FIELD_1 pins are configured as outputs and are output following the rising edge of CLOCK_IN. As an output, FIELD_0 changes state at the beginning of vertical sync during fields one, three, five, and seven. FIELD_1 changes state at the beginning of vertical sync during fields one and five.

Analog Outputs

The D/A converter values for 100-percent saturation, 100-percent amplitude color bars are shown in in Figures 6–9.

The Bt858 is configured to drive into a 50 Ω load, and the analog lowpass filter is designed to provide the proper 75 Ω output impedance.

Luminance (Y) Analog Output

The digital composite Y information is optionally processed by a digital $(\sin x/x)^{-1}$ correction filter to compensate for the inherent sin x/x D/A converter frequency roll-off.

The result drives the 10-bit D/A converter that generates the analog Y video output (see Figures 4 and 5, and Tables 4 and 5). The Y analog output is designed to drive a 50 Ω load (maximum).

Chrominance (C) Analog Output

The digital chrominance information is optionally processed by a digital $(\sin x/x)^{-1}$ correction filter to compensate for the inherent sin x/x D/A converter frequency roll-off.

The result drives the 10-bit D/A converter that generates the analog C video output (see Figures 6 and 7, and Tables 6 and 7). The C analog output is designed to drive a 50 Ω load.

NTSC/PAL Analog Output

The composite video information is optionally processed by a digital $(\sin x/x)^{-1}$ correction filter to compensate for the inherent sin x/x D/A converter frequency roll-off.

The result drives the 10-bit D/A converter that generates the composite analog NTSC/PAL video output (see Figures 8 and 9, and Tables 8 and 9). The NTSC/PAL analog output is designed to drive a 50 Ω load.

Black Burst Operation

The Bt858 may be configured to generate black burst video signals, as shown in Figures 10 and 11 and listed in Tables 10 and 11.

The black burst video signal contains sync, blank, and burst information only (no active video).

Subcarrier Frequency

The subcarrier is computed by:

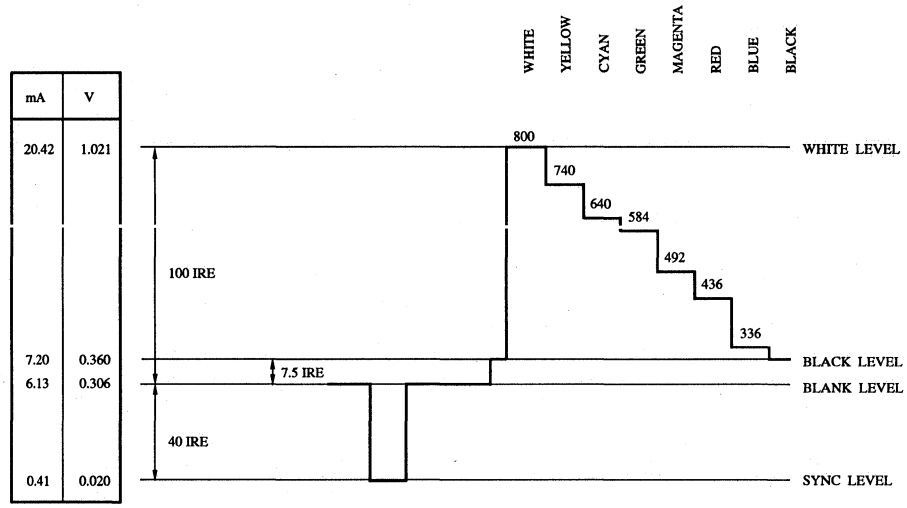
NTSC: FSC = FCLK * [P1 + P2/(4*HCOUNT)]/ 2048

PAL: FSC = FCLK * [P1 + (P2 + (67/625)) / (4*HCOUNT)] / 2048

The subcarrier frequency error will track the clock frequency error. If the clock has a tolerance of 100 PPM, then the resulting subcarrier will also have a tolerance of 100 PPM. Broadcast specifications for the subcarrier tolerance for NTSC is ±10 Hz, or roughly 3 PPM.

In addition, any jitter on the clock will be reflected in the subcarrier. Thus, care must be taken to provide a clean, stable clock to the Bt858 to produce the highest quality output.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. RS-170 levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude luminance color bars are shown.

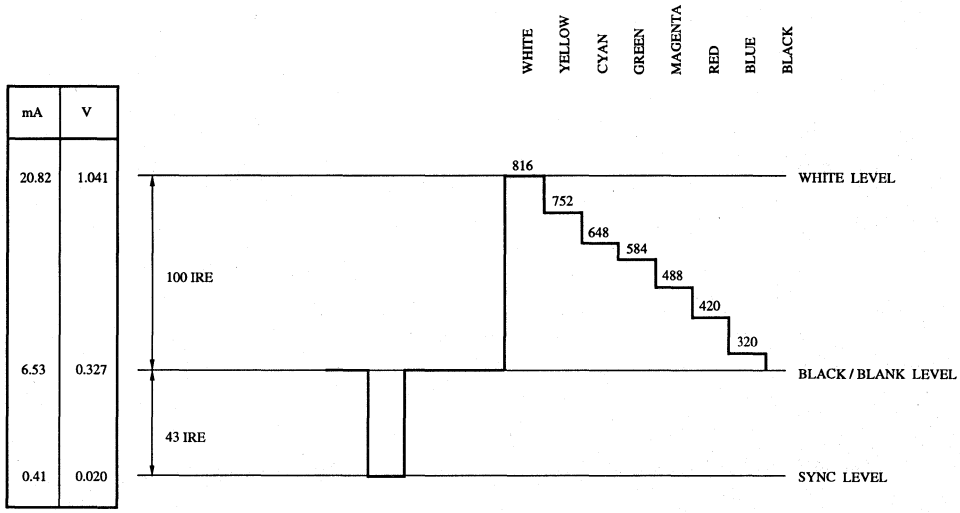
Figure 4. NTSC Y (Luminance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
WHITE	20.42	1	1	800
BLACK	7.2	1	1	282
BLANK	6.13	1	0	240
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 4. NTSC Y (Luminance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. RS-170 levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude luminance color bars are shown.

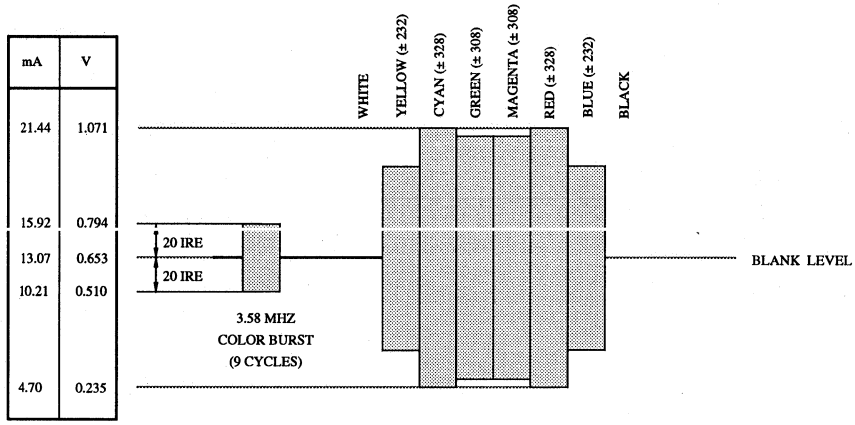
Figure 5. PAL Y (Luminance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
WHITE	20.82	1	1	816
BLACK	6.53	1	1	256
BLANK	6.53	1	0	256
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 Vand RSET = 97 Ω.

Table 5. PAL Y (Luminance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. RS-170A levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude chrominance color bars are shown.

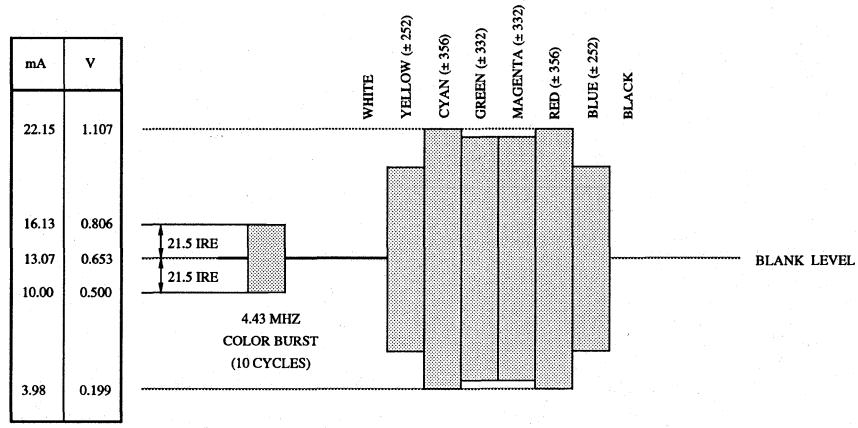
Figure 6. NTSC C (Chrominance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	21.44	x	1	840
Burst (high)	15.92	x	0	624
BLANK	13.07	x	0	512
Burst (low)	10.21	x	0	400
Peak Chroma	4.7	x	1	184

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 6. NTSC C (Chrominance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



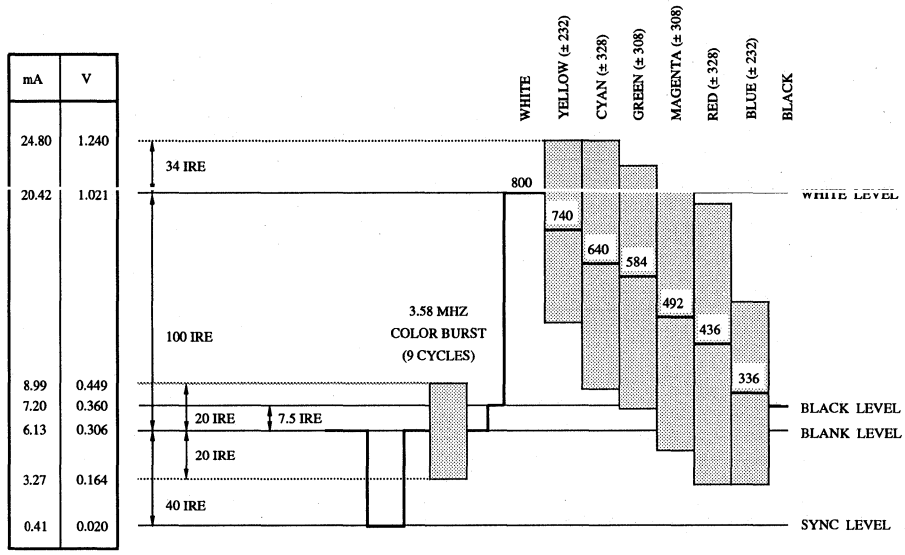
Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. PAL levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude chrominance color bars are shown.

Figure 7. PAL C (Chrominance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	22.15	x	1	868
Burst (high)	16.13	x	0	632
BLANK	13.07	x	0	512
Burst (low)	10	x	0	392
Peak Chroma	3.98	x	1	156

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 7. PAL C (Chrominance) Video Output Truth Table.



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. RS-170A levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude color bars are shown.

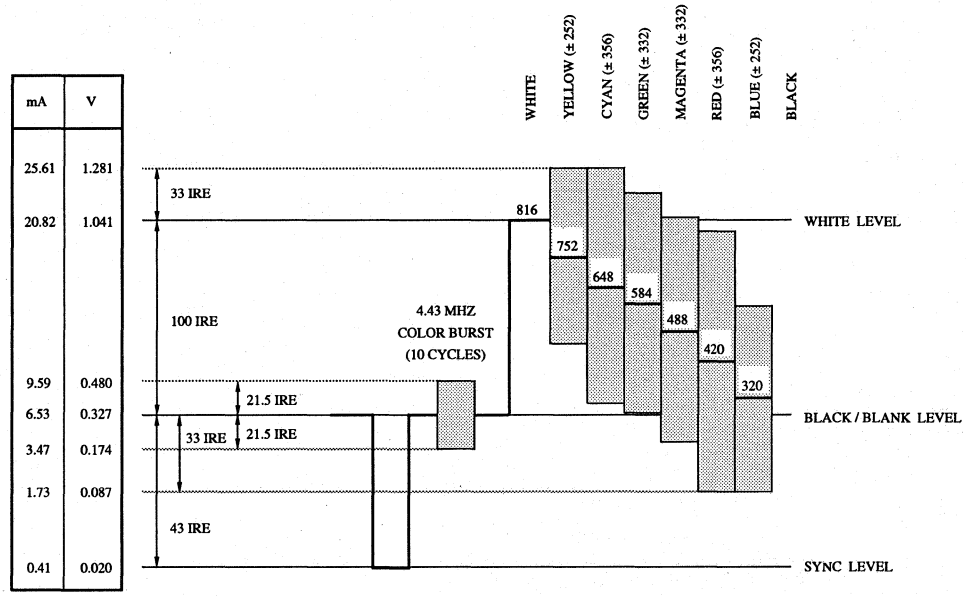
Figure 8. Composite NTSC Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	24.80	1	1	972
WHITE	20.42	1	1	800
Burst (high)	8.99	1	0	352
BLACK	7.20	1	1	282
BLANK	6.13	1	0	240
Burst (low)	3.27	1	0	128
Peak Chroma (Note 1)	2.66	1	1	104
SYNC	0.41	0	0	16

Note 1: If command bit CR31 is a logical zero, DAC data values less than 127 are made 127.

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 8. Composite NTSC Video Output Truth Table.



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. PAL levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude color bars are shown.

Figure 9. Composite PAL Video Output Waveform.

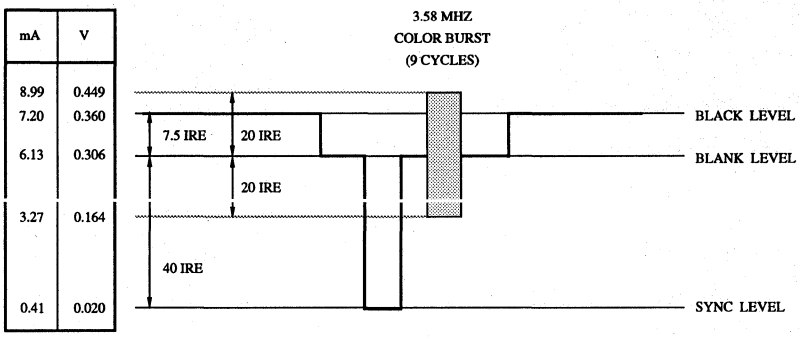
Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	25.61	1	1	1004
WHITE	20.82	1	1	816
Burst (high)	9.59	1	0	376
BLACK	6.53	1	1	256
BLANK	6.53	1	0	256
Burst (low)	3.47	1	0	136
Peak Chroma (Note 1)	1.73	1	1	68
SYNC	0.41	0	0	16

Note 1: If command bit CR31 is a logical zero, DAC data values less than 127 are made 127.

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 9. Composite PAL Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. RS-170A levels and tolerances are assumed on all levels.

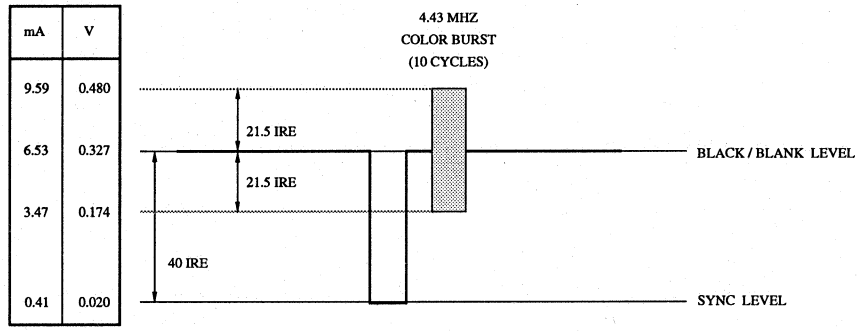
Figure 10. NTSC Black Burst Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Burst (high)	8.99	1	0	352
BLACK	7.20	1	1	282
BLANK	6.13	1	0	240
Burst (low)	3.27	1	0	128
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 10. NTSC Black Burst Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 97 Ω. PAL levels and tolerances are assumed on all levels.

Figure 11. PAL Black Burst Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Burst (high)	9.59	1	0	376
BLACK	6.53	1	1	256
BLANK	6.53	1	0	256
Burst (low)	3.47	1	0	136
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 V and RSET = 97 Ω.

Table 11. PAL Black Burst Video Output Truth Table.

Command Register_0

This command register may be written to or read by the MPU at any time, and is initialized to $00 following a reset sequence. CR00 is the least significant bit and corresponds to data bus bit D0.

CR07–CR04 Color data input format

(0000) 24-bit true-color RGB (8,8,8)
(0001) 16-bit true-color RGB (6,6,4)
(0010) 16-bit true-color RGB (5,6,5)
(0011) 15-bit true-color RGB (5,5,5)
(0100) 8-bit pseudo-color (red)
(0101) 8-bit pseudo-color (green)
(0110) 8-bit pseudo-color (blue)
(0111) reserved
(1000) reserved
(1001) 24-bit YCrCb (4:4:4)
(1010) 16-bit YCrCb (4:2:2)
(1011) reserved
(1100) mixed VGA / YCrCb
(1101) reserved
(1110) reserved
(1111) reserved

These bits specify the input format of the video data, as listed in Table 3. The pipeline delay remains unchanged regardless of the mode of operation.

YCrCb data is assumed to be derived from gamma-corrected RGB data. The lookup table RAMs may be used to provide gamma correction (typically 2.2 for NTSC and 2.8 for PAL) when RGB or pseudo-color data is being input. If the lookup table RAMs are bypassed, RGB input data should be gamma corrected.

CR03, CR02 reserved

CR01, CR00 KEY_0 read mask

(00) force KEY_0 data to zero
(01) force KEY_0 data to one
(10) invert KEY_0 input data
(11) pass KEY_0 input data

These bits either force the KEY_0 input value to a logical zero or logical one, invert the KEY_0 input value, or let it pass unchanged. These bits are ignored unless CR07–CR04 are (1100).

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time, and is initialized to $00 following a reset sequence. CR10 is the least significant bit and corresponds to data bus bit D0.

CR17	OL3 read mask (0) force OL3 data to zero (1) pass OL3 data	This bit is logically ANDed with the OL3 input prior to addressing the overlay registers.
CR16	OL2 read mask (0) force OL2 data to zero (1) pass OL2 data	This bit is logically ANDed with the OL2 input prior to addressing the overlay registers.
CR15	OL1 read mask (0) force OL1 data to zero (1) pass OL1 data	This bit is logically ANDed with the OL1 input prior to addressing the overlay registers.
CR14	OL0 read mask (0) force OL0 data to zero (1) pass OL0 data	This bit is logically ANDed with the OL0 input prior to addressing the overlay registers.
CR13	8-bit/6-bit color select (0) 6-bit (1) 8-bit	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle when the lookup table RAMs are being accessed. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles. D6 and D7 are ignored during color write cycles and a logical zero during color read cycles. In the 6-bit mode, the full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of color data are logical zeros in the 6-bit mode.
CR12	Lookup table RAM bypass enable (0) use lookup table RAMs (1) bypass RAMs	This bit specifies whether to bypass the lookup table RAMs and pixel read mask registers. When internal color bar generation is used (CR32 equals 1), the lookup table RAMs are automatically bypassed regardless of the value of this bit. The selection does not affect the pipeline delay through the device.
CR11, CR10	Reserved	

Internal Registers (continued)

Command Register_2

This command register may be written to or read by the MPU at any time, and is initialized to $F0 following a reset sequence. CR20 is the least significant bit and corresponds to data bus bit D0.

CR27, CR26 Reserved (logical one)

CR25, CR24 COLOR KEY_0 invert

(00) normal value
(01) invert value
(10) reserved
(11) disable color key_0

These bits specify whether to invert the COLOR KEY_0 value generated by the color key_0 and color mask_0 registers. These bits are ignored unless CR07–CR04 are (1100).

CR23 Reserved (logical zero)

CR22 Software reset

(0) normal operation
(1) reset device

Writing a logical one to this bit resets the device, clearing the pixel pipeline and resetting the command register bits to their initialized state (equivalent to asserting the RESET* input pin). The bit is reset to a logical zero when the software reset sequence is complete.

Following a reset condition, the Bt858 is configured for NTSC operation (square pixels, Master Mode_1) and 24-bit RGB input data format. The lookup table RAMs must be initialized before valid video may be generated.

CR21, CR20 Y / C output select

(00) normal video
(01) black burst video
(10) composite video
(11) reserved

The (00) specifies that the Y and C outputs generate normal luminance (Y) and chroma (C) video.

The (01) specifies that both the Y and C outputs generate black burst video (sync, blank, and burst, only).

The (10) specifies that both the Y and C outputs generate composite NTSC/PAL video (the same as the NTSC/PAL output) to drive multiple monitors and tape recorders.

Internal Registers (continued)

Command Register_3

This command register may be written to or read by the MPU at any time, and is initialized to $12 following a reset sequence. CR30 is the least significant bit and corresponds to data bus bit D0.

CR37–CR34 Output mode select

(0000) NTSC master mode 0
(0001) NTSC master mode 1
(0010) NTSC master mode 2
(0011) NTSC master mode 3
(0100) reserved
(0101) PAL master mode 0
(0110) PAL master mode 1
(0111) PAL master mode 2
(1000) PAL master mode 3
(1001) reserved
(1010) reserved
: :
(1110) reserved
(1111) power-down mode

These bits specify the timing and analog output mode of the Bt858.

Mode (1111) turns power off to the DACs and the A/D converter by disabling the output current. It also three-states all TTL-compatible outputs and inhibits clocking to most of the internal circuitry to minimize power consumption. The pixel and control inputs are ignored, and CLOCK_IN is directly output onto CLOCK_OUT. All the control registers and color palette RAMs are still accessible by the MPU. The Bt858 becomes operational about 1 second after the power-down mode is disabled.

CR33 Color kill enable

(0) normal operation
(1) disable color information

This bit enables (logical zero) or disables (logical one) color information on the NTSC/PAL and C video outputs.

CR32 Color bar test enable

(0) normal operation
(1) generate color bars

If this bit is a logical one and the full screen is 100-percent saturated, 75-percent amplitude color bars are generated, consisting of gray, yellow, cyan, green, magenta, red, blue, and black. The first seven colors each occupy 64 pixels of active video each scan line. Black occupies the remaining active pixels each scan line. BLANK* must be negated at the proper time in order to view the color bar output. The input format must be programmed to 24-bit RGB.

CR31 Color level limiting bypass

(0) use level limiting
(1) bypass level limiting

A logical zero enables the NTSC / PAL level limiting circuitry that limits the minimum active composite video levels. Active video values less than 127 (10-bit value) are made 127 (approximately half the sync height) to avoid possible sync detection problems with downstream video equipment.

CR30 Illegal video flag

(0) reset by MPU
(1) illegal value detected

This bit is set to a logical one if active video generates a value less than 127 (10-bit value). The MPU must write a logical zero to this bit to clear it to a logical zero.

Internal Registers (continued)

Command Register_4

This command register may be written to or read by the MPU at any time, and is initialized to $18 following a reset sequence. CR40 is the least significant bit and corresponds to data bus bit D0.

CR47 — IQ/UV low-pass filter bypass

(0) use filters
(1) bypass filters

This bit specifies whether to bypass the IQ and UV low-pass filters (just after the matrix). Regardless of the selection, there is no change in the pipeline delay.

CR46 — $(\text{Sin } x/x)^{-1}$ correction filter bypass

(0) use filters
(1) bypass filters

This bit specifies whether to bypass the $(\text{sin } x/x)^{-1}$ correction filters just prior to the analog outputs. Regardless of the selection, there is no change in the pipeline delay.

CR45 — FIELD input/output select

(0) inputs
(1) outputs

This bit specifies whether the FIELD_0 and FIELD_1 pins are inputs (logical zero) or outputs (logical one). In all modes, FIELD_0 and FIELD_1 are three-stated if CR45 is programmed low.

CR44 — CLOCK_OUT output enable

(0) output three-stated
(1) output enabled

A logical zero three-states the CLOCK_OUT pin asynchronously to the pixel clock.

CR43 — Control output enable

(0) output three-stated
(1) output enabled

A logical zero three-states the FIELD_0, FIELD_1, CSYNC*, HSYNC*, and VSYNC* pins, if they are configured as outputs, asynchronously to the pixel clock. *For HSYNC*, VSYNC*, FIELD_0, and FIELD_1, this three-state is independent of the mode of operation. The CSYNC* pin is not internally gated and must be configured by CR43 according to the mode for proper operation of the part. In all modes, FIELD_0 and FIELD_1 are three-stated if CR43 is programmed low.*

CR43: H/L	CSYNC*	V/VSYNC*	H/HSYNC*
mode 0	Q/Z	Z	Z
mode 1	X/Z	X/Z	X/Z
mode 2	Q/Z	Z	Z
mode 3	Q/Z	Q/Z	Q/Z

Z = Three-State
X = State Not Allowed in Mode
Q = Valid Output

CR42–CR41 — reserved (logical zero)

CR40 — Genlock availablility status

(0) genlock unavailable
(1) genlock available

This bit indicates whether the device has genlock support. On the Bt858, this bit is always a logical zero, indicating genlock is not supported. MPU write cycles to this bit are ignored.

Internal Registers (continued)

HCOUNT Register

This 16-bit register specifies the number of pixels per scan line. It is initialized to $030C (780) following a reset condition and may be written to and read by the MPU at any time. The HCOUNT low and high registers are independent and are individually written to and read by the MPU.

The HCOUNT low and high registers are cascaded to form a 16-bit HCOUNT register. The D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. Even values from $0002 (2) to $0FFE (4094) may be specified.

	HCOUNT High				HCOUNT Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

The HCOUNT value automatically calculates many of the horizontal timing parameters. Using the falling edge of horizontal sync as a reference, the following are internally calculated:

analog horizontal sync width (50% amplitude) = (HCOUNT/16) + (HCOUNT/128) + (HCOUNT/256) + 1

start of color burst (50% amplitude) = (HCOUNT/16) + (HCOUNT/64) + (HCOUNT/256) + (HCOUNT/512) + 1

end of color burst (NTSC, 50% amplitude) = BURST GATE start value + (HCOUNT/32) + (HCOUNT/128) + 1

end of color burst (PAL, 50% amplitude) = BURST GATE start value + (HCOUNT/32) + (HCOUNT/256) + 1

Fsc Phase Adjust Register

This 16-bit register specifies the amount of phase shift to add to the subcarrier. This may be used to adjust the subcarrier phase generated by the Bt858 to match that of an external source. It is initialized to $0000 (0) following a reset condition and may be written to and read by the MPU at any time. The Fsc phase adjust low and high registers are independent and are individually written to and read by the MPU.

The Fsc phase adjust low and high registers are cascaded to form a 16-bit Fsc phase adjust register. The D3–D7 of Fsc phase adjust high are ignored during MPU write cycles and return a logical zero during MPU read cycles. Values from $0000 (0°) to $07FF (360°) may be specified.

	Fsc Phase Adjust High			Fsc Phase Adjust Low							
Data Bit	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Internal Registers (continued)

P1 and P2 generate the color subcarrier (3.58 MHz for [M] NTSC, 4.43 MHz for [B, D, G, H, I] PAL) from the pixel clock. They must be calculated and the values loaded into the P1 and P2 registers.

P1 Low and High Registers

The P1 low and high registers are cascaded to form a 16-bit P1 register. Values from $0000 (0) to $0400 (1024) may be specified. The 16-bit register is initialized to $0255 (597) following a reset condition and may be written to and read by the MPU at any time. The P1 low and high registers are independent and are individually written to and read by the MPU. The D2–D7 of P1 high are ignored during MPU write cycles and return a logical zero during MPU read cycles.

	P1 High		P1 Low							
Data Bit	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P2 Low and High Registers

The P2 low and high registers are cascaded to form a 16-bit P2 register. Values from $0000 (0) to $1000 (4096) may be specified. The 16-bit register is initialized to $0410 (1040) following a reset condition and may be written to and read by the MPU at any time. The P2 low and high registers are independent and are individually written to and read by the MPU. The D4–D7 of P2 high are ignored during MPU write cycles and return a logical zero during MPU read cycles.

	P2 High				P2 Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P1 (Fsc) and P2 (Fsc) are calculated as follows:

$$\text{(M) NTSC: } \frac{465{,}920}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

$$\text{(B, D, G, H, I) PAL: } \frac{581{,}123.2768}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

$$\text{(N) PAL: } \frac{469{,}507.2768}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

$$\text{(4.43) NTSC (Note 1): } \frac{577{,}087.69}{\text{HCOUNT}} = P1 + \frac{P2}{4 \times \text{HCOUNT}}$$

Note 1: (4.43) NTSC is NTSC using a 4.43 MHz subcarrier. It is normally used for standards conversion between PAL and NTSC video signals.

After the appropriate value for HCOUNT value is inserted, the result is separated into an integer value (P1) and a fractional value (whose numerator is P2). Table 12 lists some of the common HCOUNT values and the resulting P1 and P2 values. Table 13 lists some of the common blanking intervals.

In order to guarantee the highest quality of signal integrity (i.e., meeting the broadcast spec), the following method should be used to determine the P1 and P2 values.

Determine the HCOUNT value by:

NTSC: HCOUNT = (int) (FCLK_desired/15734.264)
PAL: HCOUNT = (int) (FCLK_desired/15625)

Internal Registers (continued)

Determine P1 by:

NTSC: P1 = (int) [455*2048/(2*HCOUNT)]
PAL: P1 = (int) [1135*2048/(4*HCOUNT)]

Determine P2 by:

NTSC: P2 = 2*455*2048 – P1*4*HCOUNT
PAL: P2 = 1135*2048 – P1*4*HCOUNT + 13

Determine the actual clock frequency by:

NTSC: FCLK_actual = 3579545*2*HCOUNT/455
PAL: FCLK_actual = 4433618.75*HCOUNT/ [(1135/4) + (1/625)]

Color Key_0 Register

The 8-bit color key_0 register may be written to or read by the MPU at any time and is initialized to $00 following a reset condition. Data bit D0 is the least significant bit and corresponds to the R0 input bit.

The color key_0 register is compared to the R0–R7 inputs. If all unmasked bits match, the COLOR KEY_0 control signal is a logical one. This register is used only when CR07–CR04 equals (1100).

Color Mask_0 Register

The 8-bit color mask_0 register may be written to or read by the MPU at any time and is initialized to $FF following a reset condition. Data bit D0 is the least significant bit and corresponds to the R0 input bit.

A logical zero specifies that the corresponding R0–R7 input bit is to be compared against the corresponding bit in the color key_0 register. A logical one specifies that no comparison for the corresponding bit is to take place and is not used in the generation of the COLOR KEY_0 control signal. This register is used only when CR07–CR04 equals (1100).

Typical Application	Total Pixels per Scan Line (HCOUNT)	Active Pixels	4x HCOUNT	P1	P2
13.5 MHz NTSC	858	720	3432	543	104
13.5 MHz PAL	864	720	3456	672	2061
12.27 MHz (square pixels) NTSC	780	640	3120	597	1040
14.75 MHz (square pixels) PAL	944	768	3776	615	2253
14.32 MHz (4x Fsc) NTSC	910	768	3640	512	0
17.72 MHz (4x Fsc) PAL	1135	910	4540	512	0

NTSC refers to (M) NTSC; PAL refers to (B, D, G, H, I) PAL.

Table 12. Typical HCOUNT, P1, and P2 Values.

Typical Application	Sync + Back Porch Blanking (Pixels)	Front Porch Blanking (Pixels)
13.5 MHz NTSC	121	17
13.5 MHz PAL	131	13
12.27 MHz (square pixels) NTSC	118	22
14.75 MHz (square pixels) PAL	145	31
14.32 MHz (4x Fsc) NTSC	120	22
17.72 MHz (4x Fsc) PAL	159	28

NTSC refers to (M) NTSC; PAL refers to (B, D, G, H, I) PAL.

Table 13. Typical BLANK* Input Horizontal Timing.

Pin Descriptions

Pin Name	Description
F/BLANK*	Composite blank control input (TTL compatible). BLANK* is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In all modes, except Master Mode 2, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored while BLANK* is a logical zero. In Master Mode 2, this pin is the F (field) input. This pin is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. This input must be asserted with the proper timing in all modes.
H/HSYNC*	Horizontal sync control input/output (TTL compatible). In Master Mode 0, HSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Mode 1, this pin is ignored. In Master Mode 2, this pin is the H (horizontal blank) input. This pin is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored while the H or V inputs are a logical one. In Master Mode 3, HSYNC* is an output. HSYNC* is output following the rising edge of CLOCK_IN. As an output, it should drive a maximum of one LS TTL load. Absolute minimum loading should be observed. When HSYNC* is programmed as an input, the period must match the programmed HCOUNT value.
V/VSYNC*	Vertical sync control input/output (TTL compatible). In master mode 0, VSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Mode 1, this pin is ignored. In Master Mode 2, this pin is the V (vertical blank) input. The V input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored while the H or V inputs are a logical one. In Master Mode 3, VSYNC* is an output. VSYNC* is output following the rising edge of CLOCK_IN. As an output, VSYNC* should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
CSYNC*	Composite sync control input/output (TTL compatible). In Master Mode 1, CSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Modes 0, 2, and 3, this pin is ignored.
FIELD_0, FIELD_1	FIELD inputs/outputs (TTL compatible). As inputs, these pins are latched on the rising edge of CLOCK_IN. As outputs, they are output following the rising edge of CLOCK_IN and should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
R0–R7, G0–G7, B0–B7	Pixel inputs (TTL compatible). They are latched on the rising edge of CLOCK_IN. Unused inputs should be connected to GND.
OL0–OL3	Overlay select input (TTL compatible). These inputs specify, on a pixel basis, which overlay color (if any) is to be generated. They are latched on the rising edge of CLOCK_IN, and pipelined to maintain synchronization with the pixel data. Unused inputs should be connected to GND.
KEY_0	Key control input (TTL compatible). It is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. If unused, this pin should be connected to GND. This input is ignored unless command bits CR07–CR04 are (1100).
CLOCK_IN	Pixel clock input (TTL compatible). This clock input is output onto the CLOCK_OUT pin when enabled by CR43.

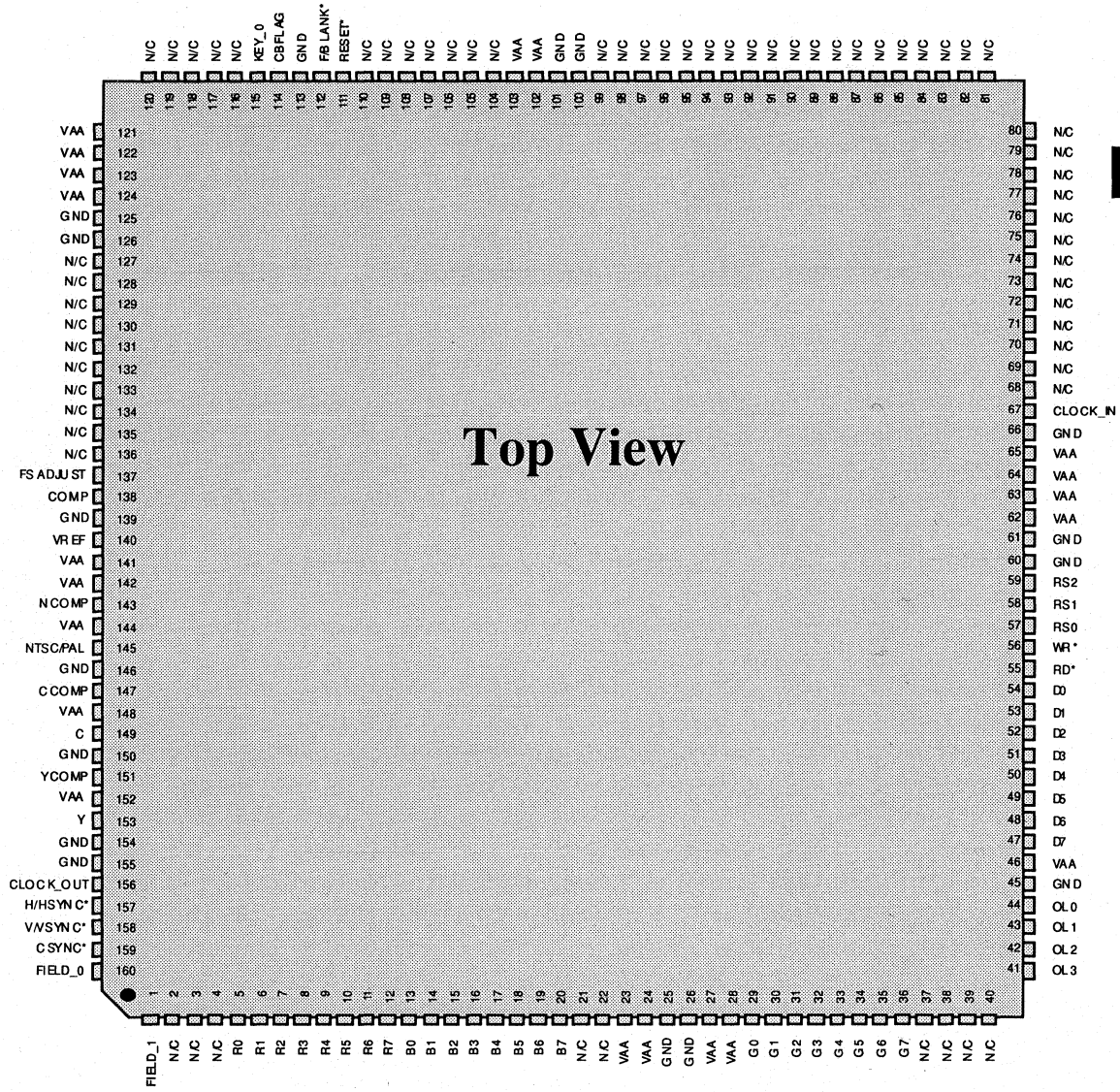
Pin Descriptions (continued)

Pin Name	Description
CLOCK_OUT	Pixel clock output (TTL compatible). This pin should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
CbFLAG	CbFLAG control input (TTL compatible). When inputting 16-bit YCrCb pixel data, this input indicates whether Cb (logical one) or Cr (logical zero) data is present on the B0–B7 inputs. CBFLAG is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. If unused, this pin should be connected to GND.
NTSC/PAL, Y, C	Composite NTSC/PAL, luminance, and chroma current outputs. These high-impedance current sources can drive a 50 Ω load (see Figure 12 in the PC Board Layout section).
COMP, NCOMP, YCOMP, CCOMP	Compensation pins. A 0.1 µF ceramic capacitor must be used to bypass each pin (except COMP) to VAA. Each capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. All pins must also be connected together as close to the device as possible.
VREF	Voltage reference input. An external voltage reference must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figure 12. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the NTSC/PAL, Y, and C outputs. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = 2059 * VREF (V) / Iout (mA)
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as specified in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
RESET*	Reset control input (TTL compatible). A logical zero for a minimum of three pixel clock cycles initializes the device. RESET* must be a logical one for normal operation. It is latched on the rising edge of CLOCK_IN.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	FIELD_1	41	OL3	84	N/C	127	N/C
		42	OL2	85	N/C	128	N/C
2	N/C	43	OL1	86	N/C	129	N/C
3	N/C	44	OL0	87	N/C	130	N/C
4	N/C			88	N/C	131	N/C
		45	GND	89	N/C	132	N/C
5	R0	46	VAA	90	N/C	133	N/C
6	R1			91	N/C	134	N/C
7	R2	47	D7	92	N/C	135	N/C
8	R3	48	D6	93	N/C	136	N/C
9	R4	49	D5	94	N/C		
10	R5	50	D4	95	N/C	137	FS ADJUST
11	R6	51	D3	96	N/C	138	COMP
12	R7	52	D2	97	N/C	139	GND
		53	D1	98	N/C	140	VREF
13	B0	54	D0	99	N/C	141	VAA
14	B1					142	VAA
15	B2	55	RD*	100	GND		
16	B3	56	WR*	101	GND	143	NCOMP
17	B4	57	RS0	102	VAA	144	VAA
18	B5	58	RS1	103	VAA	145	NTSC/PAL
19	B6	59	RS2			146	GND
20	B7			104	N/C		
		60	GND	105	N/C	147	CCOMP
21	N/C	61	GND	106	N/C	148	VAA
22	N/C	62	VAA	107	N/C	149	C
		63	VAA	108	N/C	150	GND
23	VAA	64	VAA	109	N/C		
24	VAA	65	VAA	110	N/C	151	YCOMP
25	GND					152	VAA
26	GND	66	GND	111	RESET	153	Y
27	VAA	67	CLOCK_IN	112	F/BLANK*	154	GND
28	VAA			113	GND		
		68	N/C	114	CBFLAG	155	GND
29	G0	69	N/C	115	KEY_0	156	CLOCK_OUT
30	G1	70	N/C			157	H/HSYNC*
31	G2	71	N/C	116	N/C	158	V/VSYNC*
32	G3	72	N/C	117	N/C	159	CSYNC*
33	G4	73	N/C	118	N/C	160	FIELD_0
34	G5	74	N/C	119	N/C		
35	G6	75	N/C	120	N/C		
36	G7	76	N/C				
		77	N/C	121	VAA		
37	N/C	78	N/C	122	VAA		
38	N/C	79	N/C	123	VAA		
39	N/C	80	N/C	124	VAA		
40	N/C	81	N/C	125	GND		
		82	N/C	126	GND		
		83	N/C				

Pin Descriptions (continued)



Note: N/C and test pins *must* remain floating.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt858 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Place components as close as possible to the associated pin. Whenever possible, place components so traces can be connected point to point.

The optimum layout enables the Bt858 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt858 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 12 This bead should be located within 3 inches of the Bt858 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1-µF ceramic capacitor in parallel with a 0.01-µF chip capacitor, decoupling each of the five groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 47 µF capacitor shown in Figure 12 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

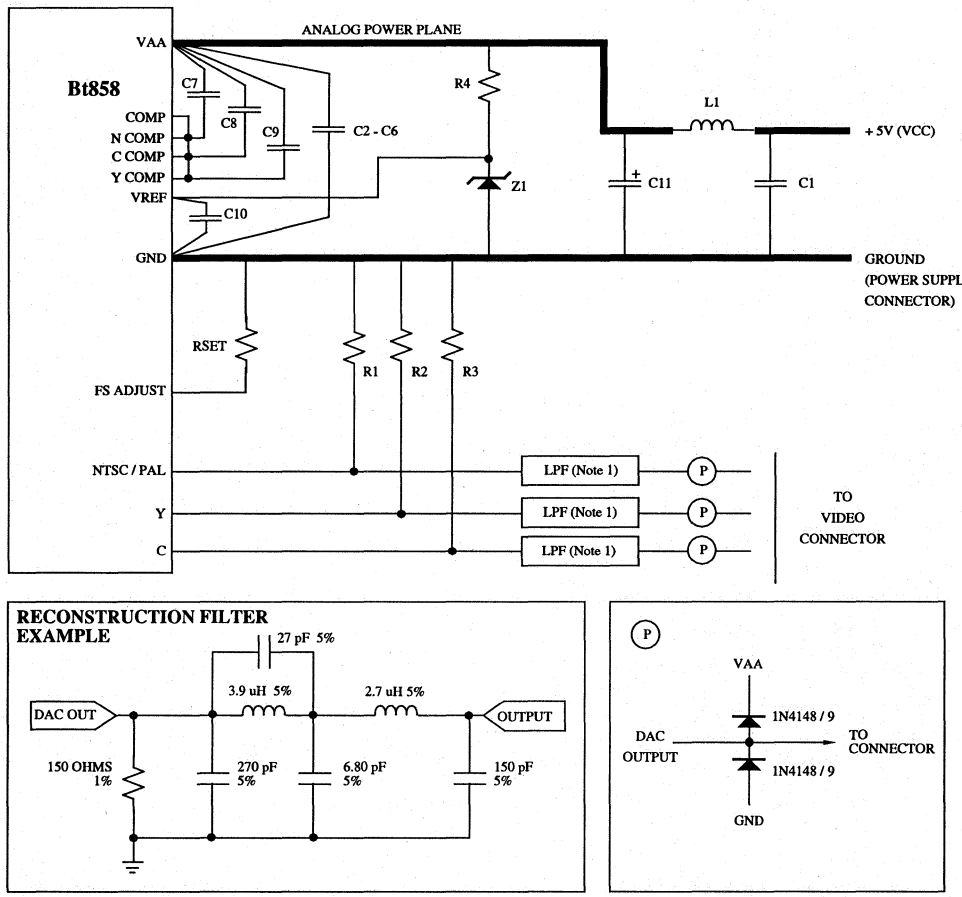
COMP Decoupling

The COMP pins must be decoupled to VAA, typically using 0.1 µF ceramic capacitors. Low-frequency supply noise will require larger values. The COMP capacitors must be as close as physically possible to the COMP and VAA pins. Surface-mount ceramic chip capacitors are preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

PC Board Layout Considerations (continued)



Note 1: A 150 Ω-to-75 Ω impedance-matching reconstruction filter is necessary on each output for proper video levels and fidelity. An example filter is illustrated above. For alternative filter designs call Brooktree Applications Engineering at 1-800-VIDEOIC.

Note 2: The value of RSET may require slight variance, depending on the reconstruction filter used, because of the filter insertion loss.

Location	Description	Vendor Part Number
C1–C10	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C11	47 µF tantalum capacitor	Mallory CSR13F476KM
L1	ferrite bead	Fair-Rite 2743001111
R1–R3	150 Ω 1% metal film resistor	Dale CMF-55F
R4	1k-Ω 5% resistor	
RSET	97 Ω 1% metal film resistor	Dale
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt858.

Figure 12. Typical Connection Diagram and Parts List for Parallel 150 Ω and 75 Ω Termination, and 150 Ω-to-75 Ω Impedance-Matching Reconstruction Filter.

PC Board Layout Considerations (continued)

Digital Signal Interconnect

The digital inputs to the Bt858 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates shouldn't be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt858 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt858 to minimize reflections. Unused analog outputs should be connected to GND.

Analog Output Protection

The Bt858 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 12 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

$(Sin\ x/x)^{-1}$ Correction Filters

The transfer function of the five-tap $(\sin x/x)^{-1}$ correction filter prior to the D/A converters is:

$$H(Z) = 294/256 * Z0 + (-24/256)*(Z^{-1} + Z^{+1}) + (5/256)*(Z^{-2} + Z^{+2})$$

Figure 13 illustrates the pass-band and stop-band characteristics of the $(\sin x/x)^{-1}$ correction filter.

IQ/UV Low-pass Digital Filters

The transfer function of the 19-tap filters that are used to low-pass filter the IQ or UV color difference video signals is:

$$H(Z) = 74/256 * Z0 + (64/256)*(Z^{-1} + Z^{+1}) + (37/256)*(Z^{-2} + Z^{+2}) + (9/256)*(Z^{-3} + Z^{+3}) + (-8/256)*(Z^{-4} + Z^{+4}) + (-11/256)*(Z^{-5} + Z^{+5}) + (-5/256)*(Z^{-6} + Z^{+6}) + (3/256)*(Z^{-8} + Z^{+8}) + (2/256)*(Z^{-9} + Z^{+9})$$

Figure 14 illustrates the pass-band and stop-band characteristics of the low-pass filters.

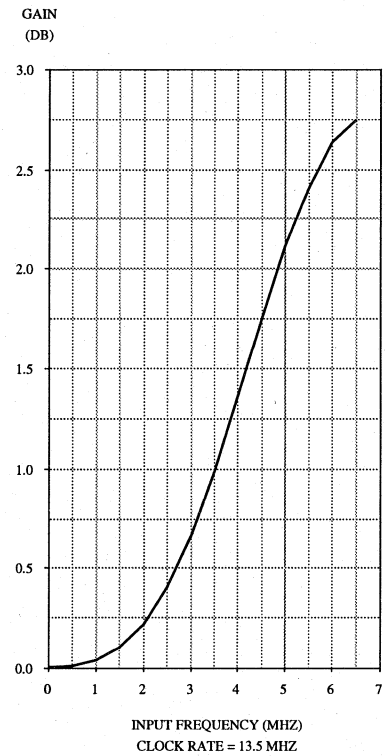


Figure 13. $(Sin\ x/x)^{-1}$ Correction Filter Characteristics.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

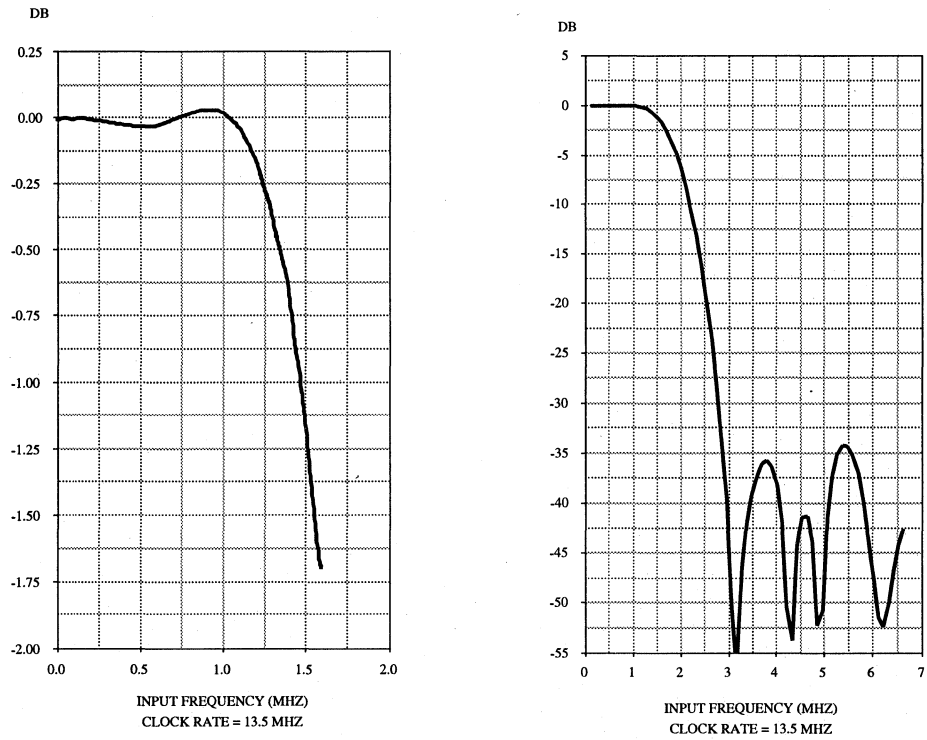


Figure 14. IQ/UV Low-pass Digital Filter Pass-Band and Stop-Band Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		50		Ω
External Voltage Reference	VREF	1.14	1.235	1.26	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating, only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Video D/A Resolution		10	10	10	Bits
Video D/A Accuracy					
Integral Linearity Error	IL			±2	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Video D/A Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF
Other Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF
Video Analog Outputs					
Output Disabled Current		0	5	50	µA
LSB Size			25.5		µA
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
C Analog Output					
Output Current (NTSC)					
Peak Chroma Relative to Blank		±7.95	±8.37	±8.79	mA
Blank Level		12.42	13.07	13.72	mA
Peak Burst Relative to Blank		±2.72	±2.86	±3.00	mA
Output Current (PAL)					
Peak Chroma Relative to Blank		±8.63	±9.08	±9.53	mA
Blank Level		12.42	13.07	13.72	mA
Peak Burst Relative to Blank		±2.91	±3.06	±3.21	mA

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Y Analog Output					
Output Current (NTSC)					
White Level Relative to Black		12.56	13.22	13.88	mA
Black Level Relative to Blank		1.03	1.08	1.13	mA
Blank Level Relative to Sync		5.43	5.72	6.01	mA
Sync Level		0.39	0.41	0.43	µA
Output Current (PAL)					
White Level Relative to Black		13.58	14.29	15.00	mA
Black Level Relative to Blank		0	0	0	mA
Blank Level Relative to Sync		5.82	6.13	6.43	mA
Sync Level		0.39	0.41	0.43	µA
NTSC / PAL Analog Output					
Output Current (NTSC)					
White Level Relative to Black		12.56	13.22	13.88	mA
Black Level Relative to Blank		1.03	1.08	1.13	mA
Burst Relative to Blank		±2.72	±2.86	±3.00	mA
Blank Level Relative to Sync		5.43	5.72	6.01	mA
Sync Level		0.39	0.41	0.43	µA
Output Current (PAL)					
White Level Relative to Black		13.58	14.29	15.00	mA
Black Level Relative to Blank		0	0	0	mA
Burst Relative to Blank		±2.91	±3.06	±3.21	mA
Blank Level Relative to Sync		5.82	6.13	6.43	mA
Sync Level		0.39	0.41	0.43	µA
VREF Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		tbd		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 97 Ω, VREF = 1.235 V, NTSC operation, and CLOCK_IN frequency = 13.5 MHz. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
RS0–RS2 Setup Time	1	10			ns
RS0–RS2 Hold Time	2	10			ns
RD* Asserted to Data Bus Driven	3	3			ns
RD* Asserted to Data Valid	4			40	ns
RD* Negated to Data Bus 3-Stated	5			20	ns
Read Data Hold Time	6	5			ns
Write Data Setup Time	7	10			ns
Write Data Hold Time	8	10			ns
RD*, WR* Pulse Width Low	9	40			ns
RD*, WR* Pulse Width High	10	6*p15			ns
Analog Output Delay	19			30	ns
Analog Output Rise/Fall Time	20		3		ns
Analog Output Settling Time	21		13		ns
Clock and Data Feedthrough (Note 1)			tbd		dB
Glitch Impulse			tbd		pV–sec
DAC-to-DAC Crosstalk			tbd		dB
Analog Output Skew			0	5	ns
Pipeline Delay					
Blank/Sync into Sync/Field Out		3	3	3	Clocks
Blank/Sync into Analog Out		34	34	34	Clocks
VAA Supply Current (Note 2)	IAA		tbd	tbd	mA
Power-Down Mode			tbd	tbd	µA

See test conditions following this section.

AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Y Bandwidth			Fin/2		MHz
Color Difference (IQ, UV) Bandwidth			1.3		MHz
Burst Frequency (Note 3)					
(M) NTSC		3.579535	3.579545	3.579555	MHz
(B, D, G, H, I) PAL		4.433614	4.433619	4.433623	MHz
Burst Envelope Rise / Fall Time		8	8	8	Clocks
Burst Cycles					
NTSC		8		9	Fsc Cycles
PAL		9		10	Fsc Cycles
Analog Sync Rise/Fall Time					
NTSC		6	6	6	Clocks
PAL		10	10	10	Clocks
Analog Blank Rise/Fall Time					
NTSC		10	10	10	Clocks
PAL		8	8	8	Clocks
Differential Gain			1		%
Differential Phase			1		Degree
SNR (per CCIR410)			60		dB
Hue Accuracy (Note 4)			0.5	1.2	%
Color Saturation Accuracy (Note 4)			0.5	1.2	%
Residual Subcarrier			–60		dB
Pixel and Control Setup Time	11	0			ns
Pixel and Control Hold Time	12	15			ns
Control Output Delay Time	13			tbd	ns
Control Output Hold Time	14	tbd			ns
CLOCK_IN Rate	Fin				
Normal Operation				18	MHz
Power Down Mode				80	MHz
CLOCK_IN Cycle Time (p15)	15				
Normal Operation		55.5			ns
Power Down Mode		12.5			ns
CLOCK_IN Pulse Width High Time	16	4			ns
CLOCK_IN Pulse Width Low Time	17	4			ns
CLOCK_IN to CLOCK_OUT Delay	18		tbd	tbd	ns

See test conditions following this section.

AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 97 Ω, VREF = 1.235 V, NTSC operation, and CLOCK_IN frequency = 13.5 MHz. Analog output load ≤10 pF; and D0–D7, FIELD_0, FIELD_1, HSYNC*, VSYNC*, and CLOCK_OUT output load ≤75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Note 3: Burst frequency tolerance is dependent on CLOCK_IN frequency tolerance and jitter. This also assumes that P1 and P2 registers are correctly configured.

Note 4: This is measured with a Matthey Vs618H filter; accuracy is dependent on pixel clock rate and the color space used.

Timing Waveforms

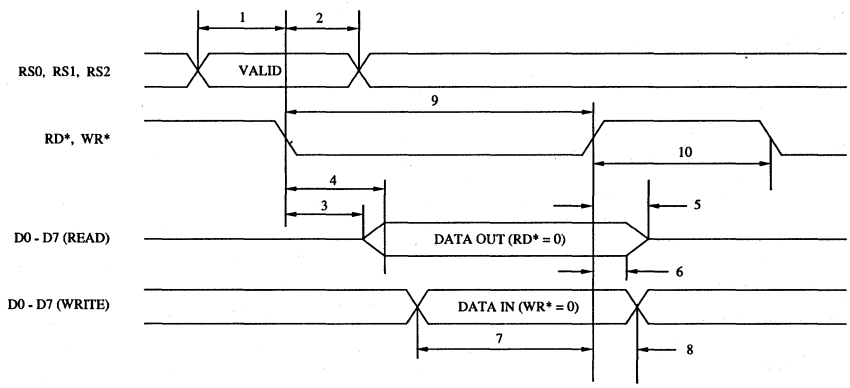
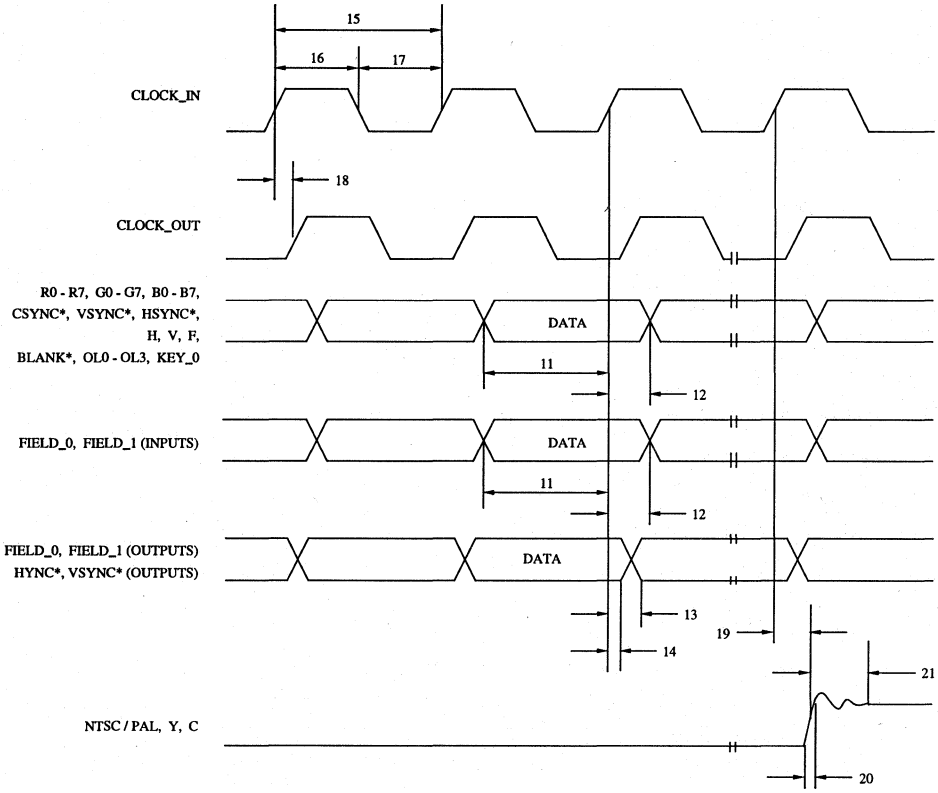


Figure 15. MPU Read/Write Timing.

Timing Waveforms (continued)



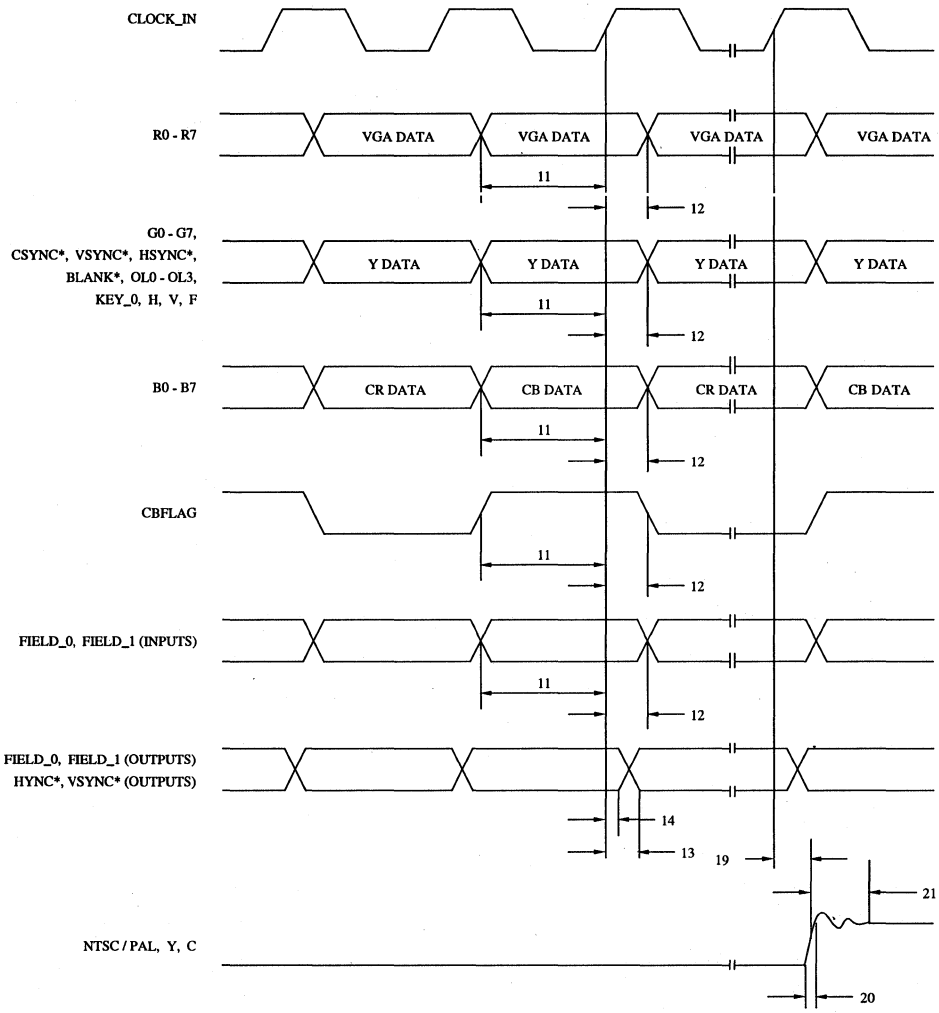
Note 1: Analog output delay is measured from the 50-percent point of the rising edge of CLOCK_IN to the 50-percent point of full-scale transition.

Note 2: Analog settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±2 LSB.

Note 3: Analog output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 16. Video Input/Output Timing. (All Input Formats Except 16-bit YCrCb).

Timing Waveforms (continued)



Note 1: Analog output delay is measured from the 50-percent point of the rising edge of CLOCK_IN to the 50-percent point of full-scale transition.

Note 2: Analog settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±2 LSB.

Note 3: Analog output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 17. Video Input/Output Timing (16-Bit YCrCb Input Format).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt858KPF	160-pin Plastic Quad Flatpack	0° to +70° C

Section 4

PC GRAPHICS RAMDACs

Brooktree®

Contents

Bt453

66 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

4

Distinguishing Features

- 66, 40 MHz Operation
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 3 x 24 Overlay Palette
- RS-343A/RS-170-Compatible Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 1 W

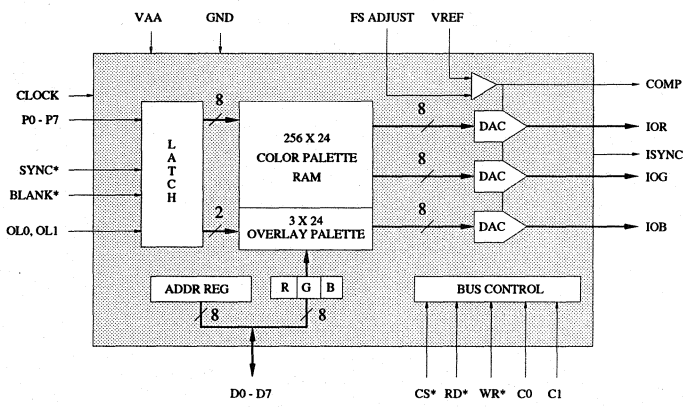
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt477, Bt478

Functional Block Diagram



Product Description

The Bt453 RAMDAC is designed specifically for high-resolution color graphics.

The Bt453 has a 256 x 24 color lookup table with triple 8-bit video D/A converters, supporting up to 259 simultaneous colors from a 16.8-million color palette. Three overlay registers provide, for example, overlaying cursors, grids, menus. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt453 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load.

Both the differential and linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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L453001 Rev. J

Brooktree®

MPU Interface

As illustrated in the functional block diagram, the Bt453 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The MPU interface operates asynchronously to the video data, simplifying the design interface.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, the color palette RAM, or the overlay registers, as indicated in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by reading another sequence of red, green, and blue data.

Any time the CS* input is a logical zero, the video outputs are forced to the black level. When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While the MPU is accessing the overlay color registers, the 6 most significant bits of the address register (ADDR2–7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as specified in Table 2.

Figure 1 illustrates the MPU read/write timing.

C1	C0	Addressed by MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

Table 1. Control Input Truth Table.

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0–7 (counts binary)	$00 - $FF	0	1	color palette RAM
	xxxx xx00	1	1	reserved
	xxxx xx01	1	1	overlay color 1
	xxxx xx10	1	1	overlay color 2
	xxxx xx11	1	1	overlay color 3

Table 2. Address Register (ADDR) Operation.

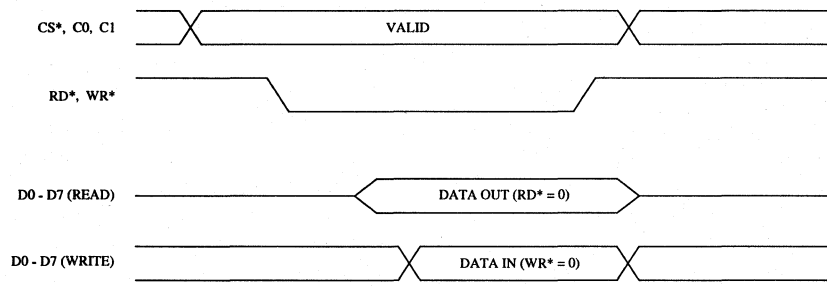


Figure 1. MPU Read/Write Timing.

Frame Buffer Interface

While CS* is a logical one, the P0–P7, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as specified in Table 3. The addressed location provides 24 bits of color information to the three D/A converters. (See Figure 2 for timing information.)

The SYNC* and BLANK* inputs are also latched on the rising edge of CLOCK to maintain synchronization with the color data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 4 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt453 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

OL1	OL0	P0 - P7	Addressed by frame buffer
0	0	$00	color palette RAM location $00
0	0	$01	color palette RAM location $01
:	:	:	:
0	0	$FF	color palette RAM location $FF
0	1	$xx	overlay color 1
1	0	$xx	overlay color 2

Table 3. Pixel and Overlay Control Truth Table.

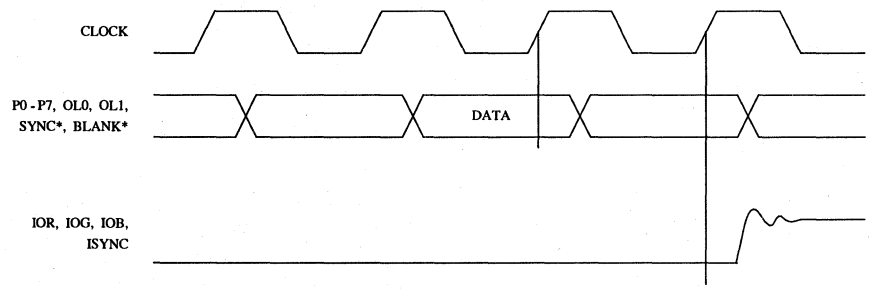
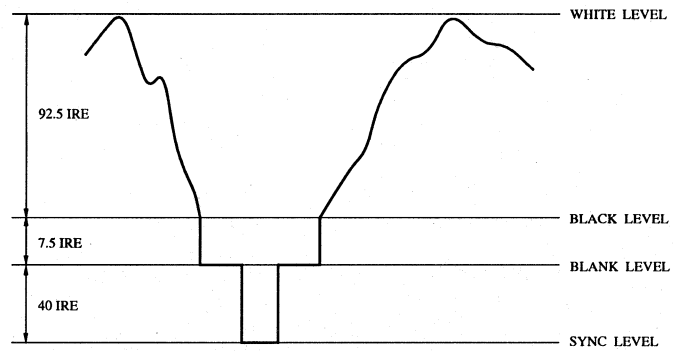


Figure 2. Video Input/Output Timing.

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 280 Ω, and VREF = 1.235 V. ISYNC is connected to IOG. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 280 Ω and VREF = 1.235 V. ISYNC is connected to IOG.

Table 4. Video Output Truth Table.

Pin Descriptions

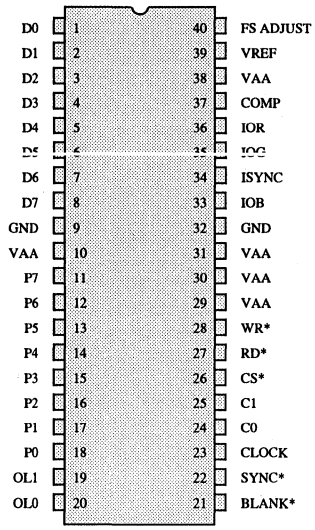
Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as specified in Table 4. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 4; therefore, SYNC* should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as specified in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 4 in the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. This high-impedance current source is typically connected directly to the IOG output (Figure 4) and is used to encode sync information onto the green channel. ISYNC does not output any current while SYNC* is a logical zero. The amount of current output while SYNC* is a logical one is: ISYNC (mA) = 1,728 * VREF (V) / RSET (Ω) If sync information is not required on the green channel, this output should be connected to GND.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). The IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is (assuming ISYNC is connected to IOG): RSET (Ω) = 6,047 * VREF (V) / IOG (mA) The relationship between RSET and the full-scale output current on IOR and IOB is: IOR, IOB (mA) = 4,319 * VREF (V) / RSET (Ω)

Pin Descriptions *(continued)*

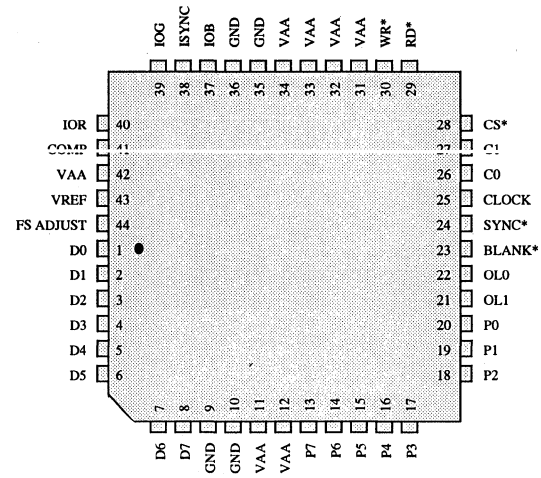
Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
VREF	Voltage reference input. An external voltage reference circuit, such as that shown in Figure 4, must supply this input with a 1.2 V (typical) reference. The Bt453 has an internal pullup resistor between VREF and VAA. As the value of this resistor may vary slightly with process variations, the use of a resistor divider network to generate the reference voltage is not recommended. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 4. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. While CS* is a logical zero, the IOR, IOG, and IOB outputs are forced to the black level. The Bt453 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first (see Figure 1).
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero (see Figure 1).
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as listed in Table 1.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions *(continued)*

40-pin DIP Package



44-pin Plastic J-Lead (PLCC) Package



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt453, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt453 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt453 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt453 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt453. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the three groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 4 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt453 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt453 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt453 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt453 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt453 to minimize reflections. Unused analog outputs should be connected to GND.

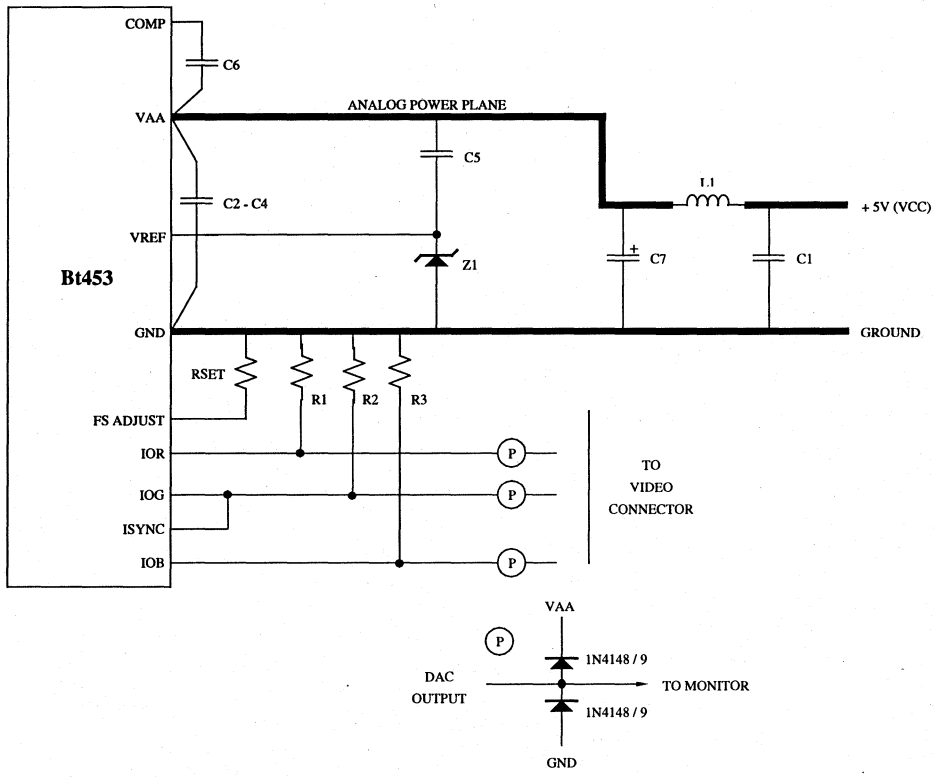
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt453 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1–C6	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C7	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	280 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt453.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.14	1.235	1.26	V
FS ADJUST Resistor	RSET		280		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			10	µA
Output Capacitance	CDOUT		20		pF
Analog Outputs					
Gray-Scale Current Range		15		22	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching (25–70° C.)			2	5	%
Output Compliance	VOC	–1.0		+1.4	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		30		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.12	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 Ω, VREF = 1.235 V, and ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	66 MHz Devices Min	66 MHz Devices Typ	66 MHz Devices Max	40 MHz Devices Min	40 MHz Devices Typ	40 MHz Devices Max	Units
Clock Rate	Fmax			66			40	MHz
CS*, C0, C1 Setup Time	1	35			35			ns
CS*, C0, C1 Hold Time	2	35			35			ns
RD*, WR* High Time	3	25			25			ns
RD* Asserted to Data Bus Driven	4	5			5			ns
RD* Asserted to Data Valid	5			100			100	ns
RD* Negated to Data Bus 3-Stated	6			15			15	ns
WR* Low Time	7	50			50			ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	5			5			ns
Pixel and Control Setup Time	10	5			7			ns
Pixel and Control Hold Time	11	2			3			ns
Clock Cycle Time	12	15			25			ns
Clock Pulse Width High Time	13	5			7			ns
Clock Pulse Width Low Time	14	5			7			ns
Analog Output Delay	15		20	30		20	30	ns
Analog Output Rise/Fall Time	16		3			3		ns
Analog Output Settling Time (Note 1)	17		25			25		ns
Clock and Data Feedthrough (Note 1)			–48			–48		dB
Glitch Impulse (Note 1)			50			50		pV–sec
DAC-to-DAC Crosstalk			–22			–22		dB
Analog Output Skew			1	2		1	2	ns
Pipeline Delay	18	2	2	2	2	2	2	Clocks
VAA Supply Current (Note 2)	IAA		220	275		190	250	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 Ω, VREF = 1.235 V, and ISYNC connected to IOG. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing waveforms and notes in Figures 5 and 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms

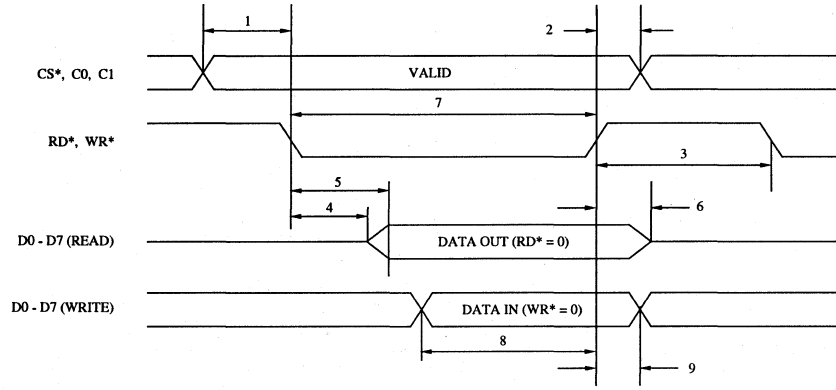
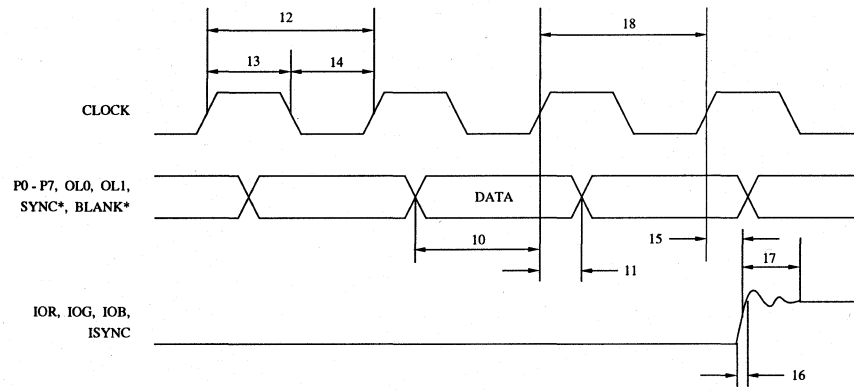


Figure 5. MPU Read/Write Timing Dimensions.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

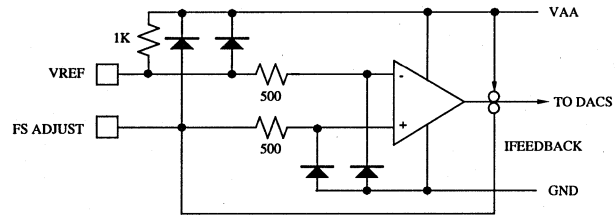
Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

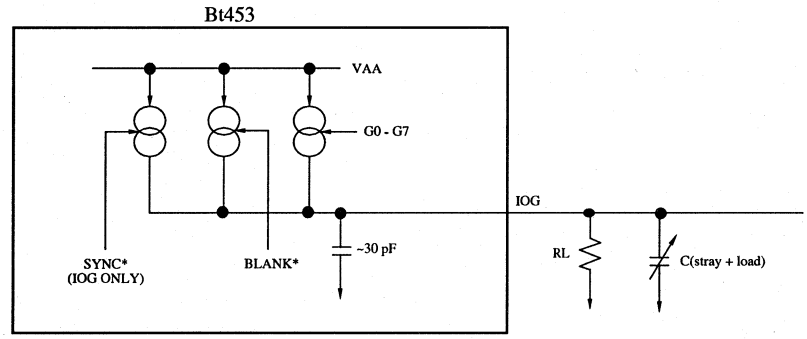
Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt453KP66	66 MHz	40-pin 0.6" Plastic DIP	0° to +70° C
Bt453KPJ66	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt453KC66	66 MHz	40-pin 0.6" CERDIP	0° to +70° C
Bt453KC	40 MHz	40-pin 0.6" CERDIP	0° to +70° C
Bt453KP	40 MHz	40-pin 0.6" Plastic DIP	0° to +70° C
Bt453KPJ	40 MHz	44-pin Plastic J-Lead	0° to +70° C



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output (IOG).

Bt471
Bt476
Bt478

80 MHz
256-Word Color Palette
Personal System/2®
RAMDAC™

4

Distinguishing Features

- Personal System/2® Compatibility
- 80, 66, 50, 35 MHz Operation
- Triple 6-bit or 8-bit D/A Converters
- 256-Word Color Palette RAM
- RS-343A-Compatible Outputs
- 15 Overlay Registers (Bt471/478)
- Sync on All Three Channels (Bt471/478)
- Programmable Pedestal (Bt471/478)
- External Voltage or Current Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC or 28-pin DIP Package

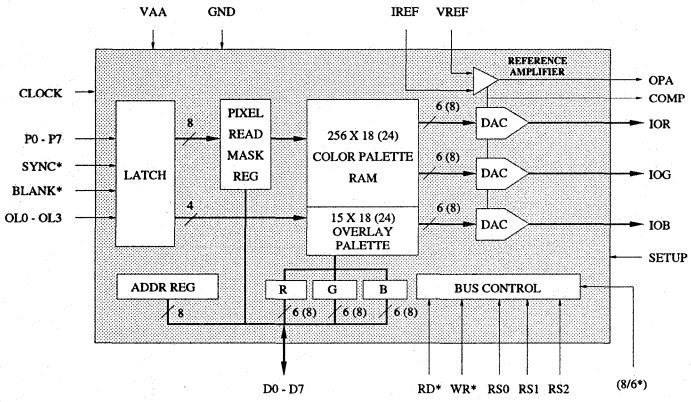
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt473, Bt477, Bt479
- Bt474, Bt475

Functional Block Diagram



Product Description

The Bt471, 476, and 478 are pin-compatible and software-compatible RAMDACs designed specifically for Personal System/2®-compatible color graphics. The Bt476 is also available in a 28-pin DIP package that is pin compatible with the IMS® G176.

The Bt471 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The Bt478 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6-bit or 8-bit D/A converter operation. The Bt476 is similar to the Bt471 but has no overlays, no programmable setup, and no sync information on the analog outputs.

Additional features on the Bt471 and Bt478 include 15 overlay registers that provide, for example, overlaying cursors, grids, menus, and EGA emulation. Also supported is sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference.

The Bt471/476/478 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load.

Note: "Personal System/2®" and "PS/2®" are registered trademarks of IBM. "IMS®" is a registered trademark of Inmos Limited.

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MPU Interface

As illustrated in the functional block diagram, the Bt471/476/478 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU loads the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. (See Figure 7 in the Timing Waveforms section.)

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU loads the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	reserved

Table 1. Control Input Truth Table.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (such as block fills of the color palette) should take place during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register are incremented following a blue read or write cycle. (ADDR0–7) are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as indicated in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Bt471/476 Data Bus Interface

Color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

Bt478 Data Bus Interface

On the Bt478, the 8/6* control input is used to specify whether the MPU is reading and writing 8 bits (8/6* = logical one) or 6 bits (8/6* = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and when the Bt471/476 is used), color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

When the Bt478 is in the 6-bit mode, its full-scale output current will be about 1.5-percent lower than when it is in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the Bt471/476) of color information to the three D/A converters. For proper operation, the pixel read mask register must be initialized by the user after power-up.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 1, 2, and 3. Tables 4, 5, and 6 detail how the SYNC* and BLANK* inputs modify the output levels.

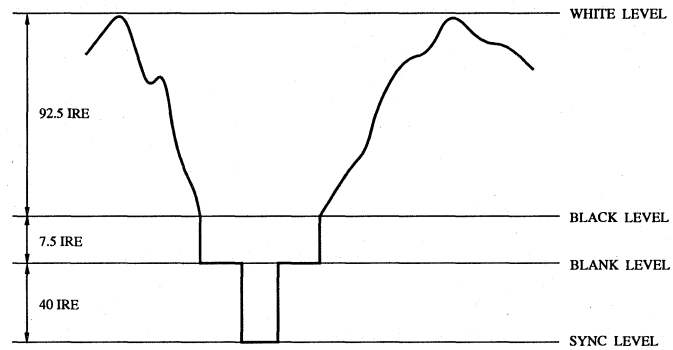
The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used. The Bt476 generates only a 0 IRE blanking pedestal (Figures 2 and 3).

The analog outputs of the Bt471/476/478 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

OL0–OL3	P0–P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF).

BT471 / 478 W/O SYNC		BT471 / 478 WITH SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

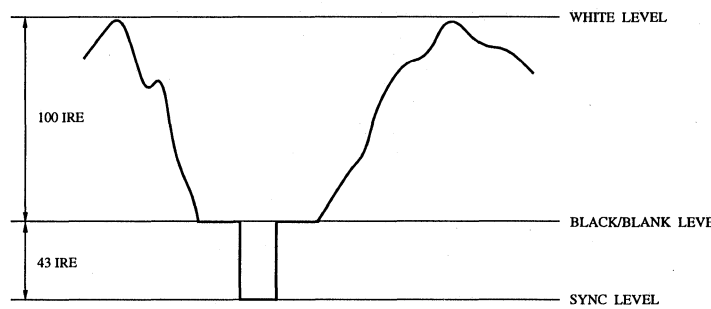
Figure 1. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

BT476 OR BT471 / 478 W/O SYNC		BT471 / 478 WITH SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

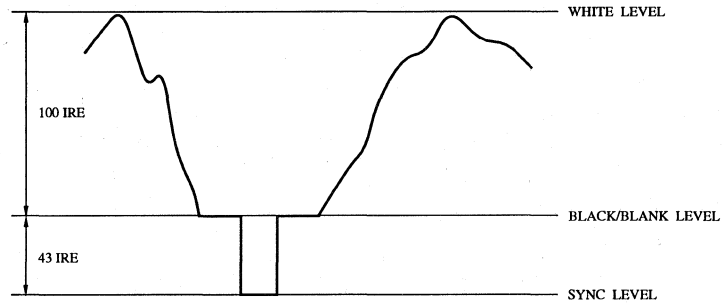
Figure 2. RS-343A Composite Video Output Waveforms. (SETUP = 0 IRE)

Description	Bt476 Iout (mA)	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 4, 5 and 6. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). SETUP is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Clock Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as shown in Table 3. When the overlay palette is accessed, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external voltage reference is used (Figure 4 in the PC Board Layout Considerations section), this pin should be connected to OPA. If an external current reference is used (Figure 5 in the PC Board Layout Considerations section), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 4), it must supply this input with a 1.2 V (typical) reference. IF an external current reference is used (Figure 5), this pin should be left floating; however, the bypass capacitor must still be connected. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figure 4. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 4), this pin must be connected to COMP. When an external current reference is used (Figure 5), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figures 4, 5, and 6 in the PC Board Layout Considerations section).
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>IREF</td><td>Full-scale adjust control. The IRE relationships in Figures 1, 2, and 3 are maintained, regardless of the full-scale output current.

When an external voltage reference is used (Figure 4), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2® applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

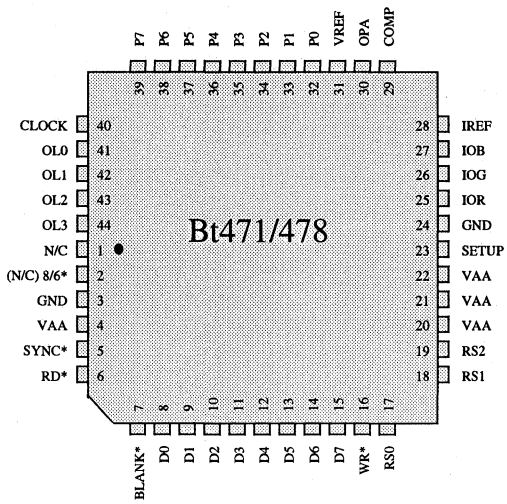
When an external current reference is used (Figures 5 and 6), the relationship between IREF and the full-scale output current on each output is:

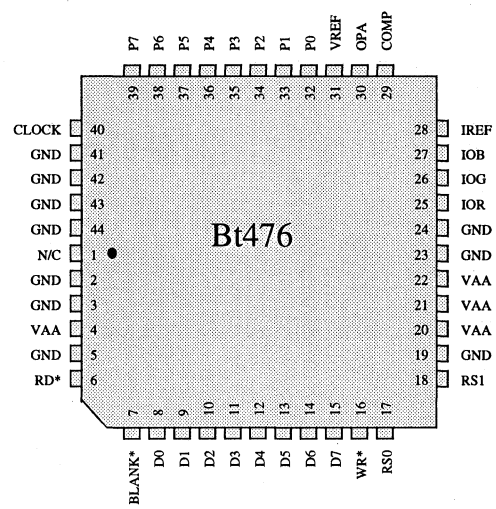
IREF (mA) = Iout (mA) / K

<table>
<tr><th>Part</th><th>Mode</th><th>Pedestal</th><th>K (with sync)</th><th>K (without sync)</th></tr>
<tr><td>Bt478</td><td>6-bit</td><td>7.5 IRE</td><td>3.170</td><td>2.26</td></tr>
<tr><td></td><td>8-bit</td><td>7.5 IRE</td><td>3.195</td><td>2.28</td></tr>
<tr><td></td><td>6-bit</td><td>0 IRE</td><td>3.000</td><td>2.10</td></tr>
<tr><td></td><td>8-bit</td><td>0 IRE</td><td>3.025</td><td>2.12</td></tr>
<tr><td>Bt471</td><td>(6-bit)</td><td>7.5 IRE</td><td>3.170</td><td>2.26</td></tr>
<tr><td></td><td></td><td>0 IRE</td><td>3.000</td><td>2.10</td></tr>
<tr><td>Bt476</td><td>(6-bit)</td><td>0 IRE</td><td>3.000</td><td>2.10</td></tr>
</table>
</td></tr>
<tr><td>WR*</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.</td></tr>
<tr><td>RD*</td><td>Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as detailed in Tables 1 and 2. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>D0 - D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>8/6*</td><td>8-bit/6-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles. (D6 and D7 are ignored during color write cycles and logical zeros during color read cycles.) This pin should be connected to GND when the Bt476 is used.</td></tr>
</table>

Pin Descriptions *(continued)*

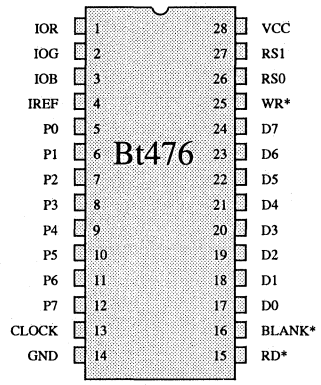
44-Pin Plastic J-Lead (PLCC)





Note 1: Names in parentheses are pin names for the Bt471.
Note 2: N/C pins may be left unconnected with no effect on the performance of the Bt471/476/478.

28-Pin DIP



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt471, Bt476, and Bt478, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook.*

The layout should be optimized for lowest noise on the Bt471, Bt476, and Bt478 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt471, Bt476, and Bt478 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt471, Bt476, and Bt478 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within 3 inches of the Bt471, Bt476, and Bt478. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 4, 5, and 6 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt471, Bt476, and Bt478 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt471, Bt476, and Bt478 require a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt471, Bt476, and Bt478 use the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt471, Bt476, and Bt478 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

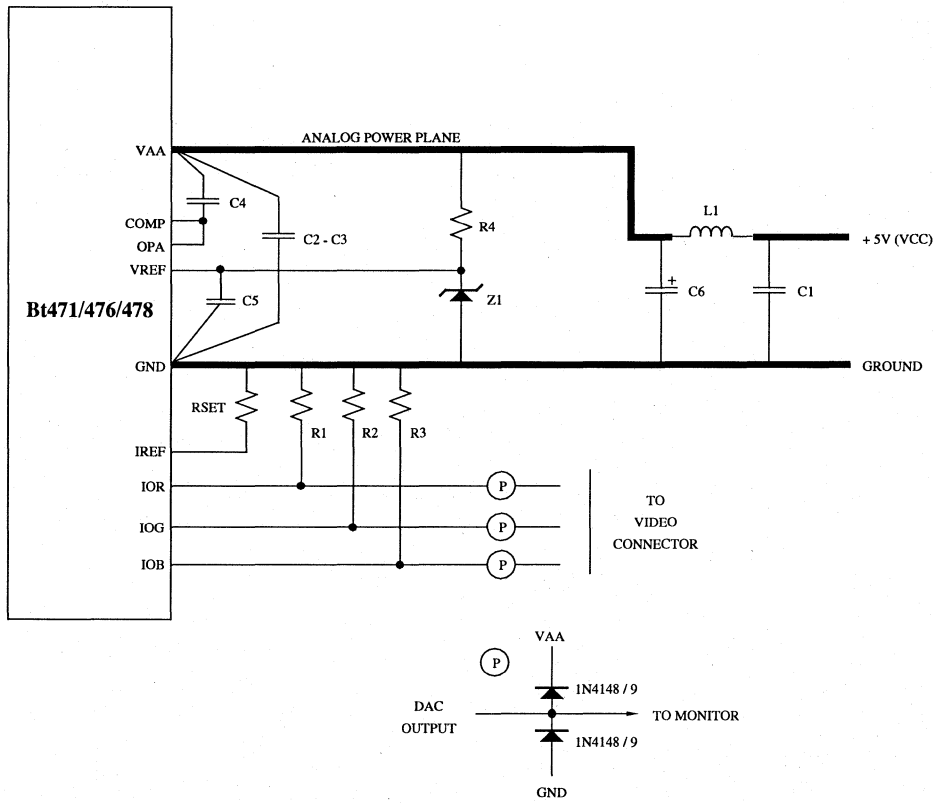
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt471, Bt476, and Bt478 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt471, Bt476, and Bt478 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

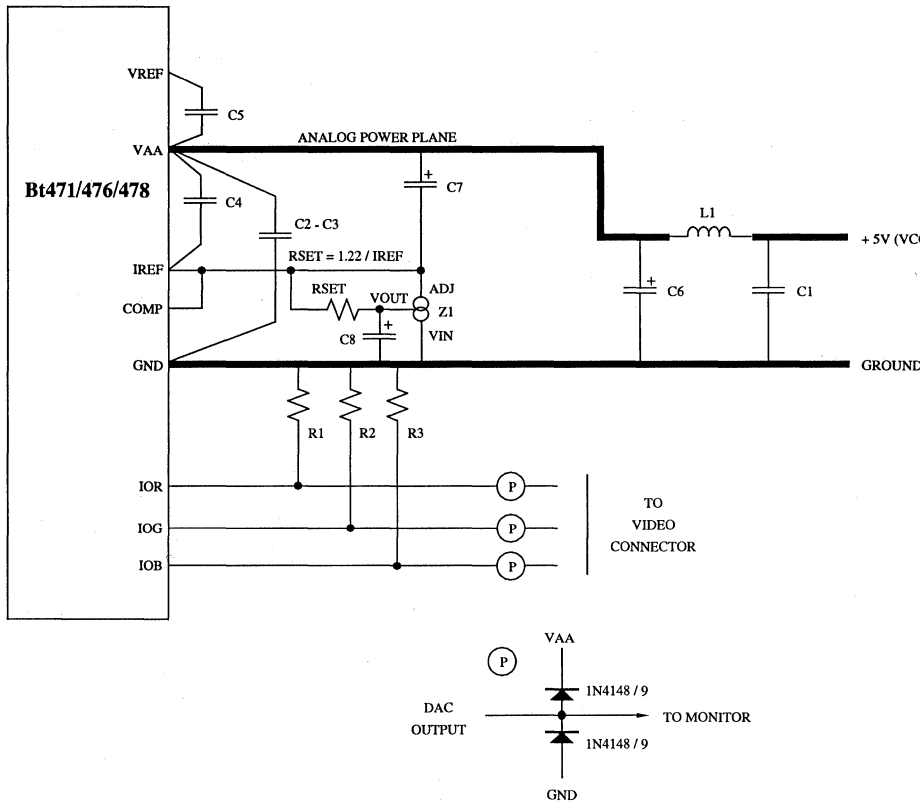


Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	—
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 4. Typical Connection Diagram and Parts List for the 44-Pin PLCC (External Voltage Reference).



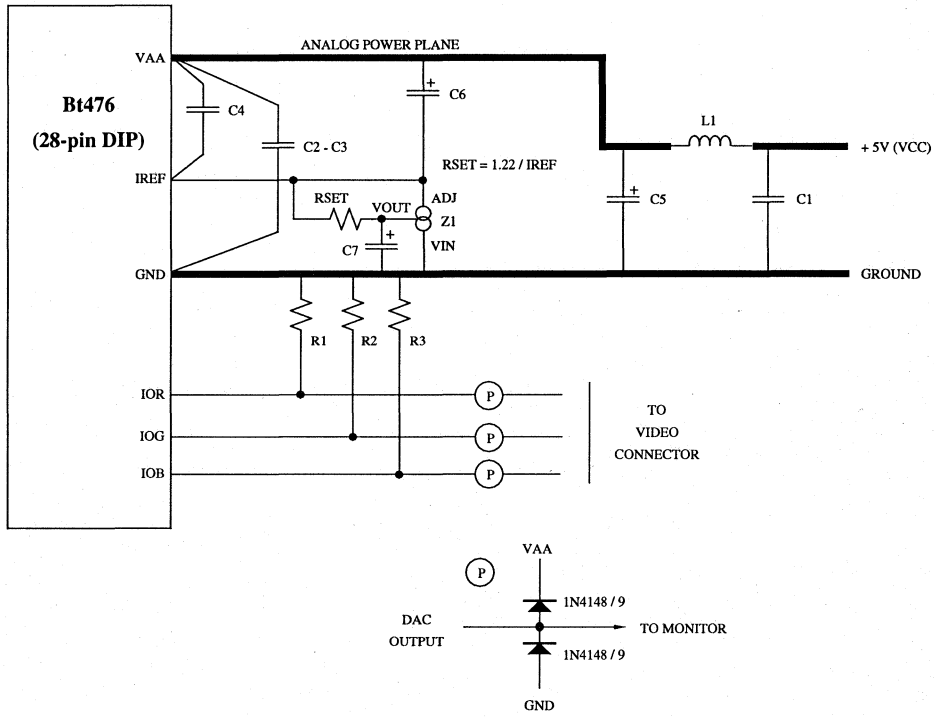
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 5. Typical Connection Diagram and Parts List for the 44-Pin PLCC (External Current Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF capacitor	Mallory CSR13G106KM
C6, C7	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt476.

Figure 6. Typical Connection Diagram and Parts List for the 28-Pin DIP (External Current Reference).

Application Information

Using Multiple Devices

When multiple RAMDACs are used, each RAMDAC should share a common power plane with one ferrite bead. In addition, a single reference may drive multiple devices. However, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance is obtained if each RAMDAC has its own reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

4

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt478		8	8	8	Bits
Bt471/476		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt478				±1	LSB
Bt476				±1/2	LSB
Bt471				±1/4	LSB
Differential Linearity Error	DL				
Bt478				±1	LSB
Bt476				±1/2	LSB
Bt471				±1/4	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black (Note 1)		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Bt476		0	0	0	µA
Blank Level					
Bt471/478		6.29	7.62	8.96	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA
LSB Size					
Bt478 (8/6* = logical one)			69.1		µA
Bt471/476			279.68		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IVREF		10		µA
Power Supply Rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Since the Bt471 and Bt476 have 6-bit DACs (and the Bt478 is in the 6-bit mode), the output levels are approximately 1.5-percent lower than these values.

Note 2: Guaranteed by characterization, not tested.

Analog Output Levels — PS/2® Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Bt476		0	5	50	µA
Blank Level					
Bt471/478		6.6	8	9.4	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA

Test conditions to generate PS/2®-compatible video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 140 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.88 mA.

AC Characteristics

Parameter	Symbol	80 MHz Devices Min	80 MHz Devices Typ	80 MHz Devices Max	66 MHz Devices Min	66 MHz Devices Typ	66 MHz Devices Max	Units
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	3			3			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17			3			3	ns
Analog Output Settling Time (Note 1)	18		13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–3			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	240		180	240	mA

See test conditions and notes on next page.

AC Characteristics *(continued)*

		80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	3			3			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17			3			3	ns
Analog Output Settling Time (Note 1)	18		20			28		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	240		180	240	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.39 mA. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing waveforms and notes in Figures 7 and 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: at Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

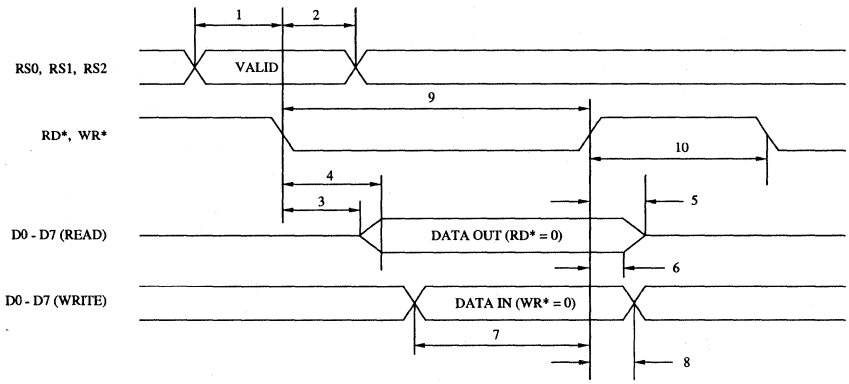
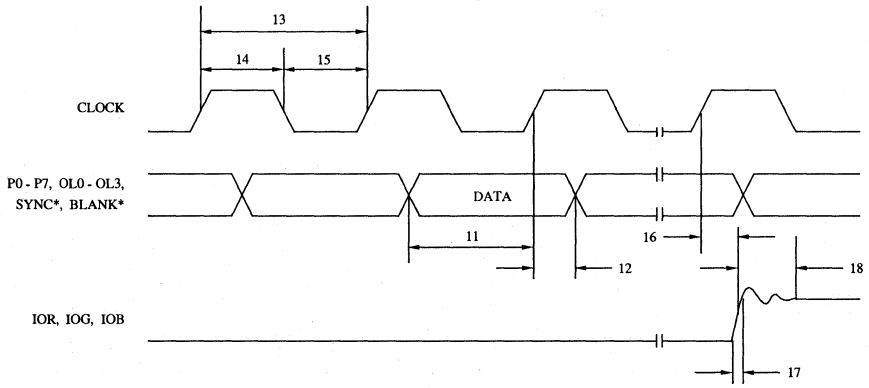


Figure 7. MPU Read/Write Timing Dimensions.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB (Bt478), ±1/4 LSB (Bt471), or ±1/2 LSB (Bt476).

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. Video Input/Output Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Sync Generation	Speed	Package	Ambient Temperature Range
Bt471KPJ80	256 x 18	15 x 18	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ66	256 x 18	15 x 18	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ50	256 x 18	15 x 18	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ35	256 x 18	15 x 18	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ66	256 x 18	—	no	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ50	256 x 18	—	no	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ35	256 x 18	—	no	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KP66	256 x 18	—	no	66 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt476KP50	256 x 18	—	no	50 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt476KP35	256 x 18	—	no	35 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt478KPJ80	256 x 24	15 x 24	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ66	256 x 24	15 x 24	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ50	256 x 24	15 x 24	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ35	256 x 24	15 x 24	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt473

80 MHz
Monolithic CMOS
Triple 8-bit
True-Color RAMDAC™

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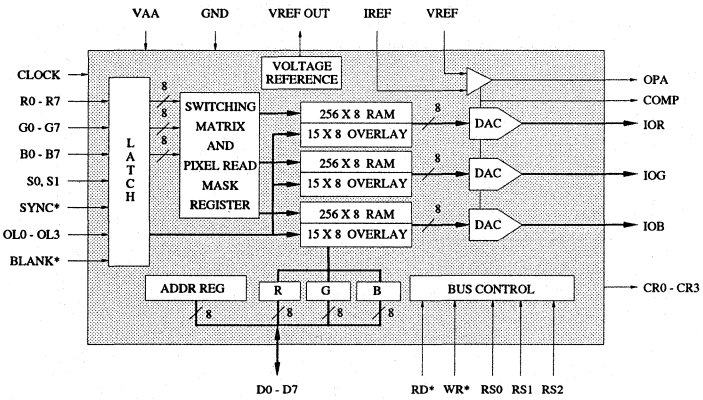
Distinguishing Features

- Bt471/478 Software Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 15 x 8 Overlay Registers
- RS-343A Compatible Outputs
- Sync on All Three Channels
- Programmable Pedestal(0 or 7.5 IRE)
- On-Chip Voltage Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 68-pin PLCC Package
- Typical Power Dissipation: 900 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt473 true-color RAMDAC is designed specifically for true-color computer graphics. It has three 256 x 8 color lookup tables with triple 8-bit video D/A converters to support 24-bit true-color operation. In addition, 8-bit pseudo- color, 8-bit true-color, and 15-bit true-color operations are supported.

Features include a programmable pedestal (0 or 7.5 IRE) and optional on-chip voltage reference. The 15 overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported are a pixel read mask register and sync generation on all three channels.

Either an external current reference, an external voltage reference, or the internal voltage reference may be used.

The Bt473 generates RS-343A compatible video signals into a doubly terminated 75 Ω load. Differential and integral linearity errors are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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L473001 Rev. I

Brooktree®

MPU Interface

As illustrated in the functional block diagram, the Bt473 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAMs
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register

Table 1. Control Input Truth Table.

into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (i.e., block fills of the color palette) should be done during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

8-Bit / 6-Bit Operation

The command register specifies whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the Bt473's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Color Modes

Four color modes are supported by the Bt473: 24-bit true color, 15-bit true color, 8-bit true color, and 8-bit pseudo color. The mode of operation is determined by the S0 and S1 inputs, in conjunction with CR7 and CR6 of the command register. S0 and S1 are pipelined to maintain synchronization with the R0–R7, G0–G7, B0–B7, and OL0–OL3 pixel and overlay data inputs.

Table 3 lists the modes of operation.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	0	1	red value
	01	x	0	1	green value
	10	x	0	1	blue value
ADDR0 - 7 (counts binary)	$00 - $FF	0	0	1	color palette RAMs
	xxxx 0000	1	0	1	reserved
	xxxx 0001	1	0	1	overlay color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description *(continued)*

OL3–OL0	S1, S0	CR7, CR6	Mode	R7–R0	G7–G0	B7–B0
1111 : 0001	xx : xx	xx : xx	overlay color 15 : overlay color 1	$xx : $xx	$xx : $xx	$xx : $xx
0000 0000 0000 0000	00 00 00 00	00 01 10 11	24-bit true color 24-bit true color 24-bit true color reserved	R7–R0 R7–R0 R7- R0 reserved	G7–G0 G7–G0 G7–G0 reserved	B7–B0 B7–B0 B7–B0 reserved
0000 0000 0000 0000	01 01 01 01	00 01 10 11	24-bit true color bypass 24-bit true color bypass 24-bit true color bypass reserved	R7–R0 R7–R0 R7–R0 reserved	G7–G0 G7–G0 G7–G0 reserved	B7–B0 B7–B0 B7–B0 reserved
0000 0000 0000 0000	10 10 10 10	00 01 10 11	8-bit pseudo color (red) 8-bit pseudo color (green) 8-bit pseudo color (blue) reserved	P7–P0 ignored ignored reserved	ignored P7–P0 ignored reserved	ignored ignored P7–P0 reserved
0000 0000 0000 0000	11 11 11 11	00 01 10 11	8-bit true-color bypass (red) 8-bit true-color bypass (green) 8-bit true-color bypass (blue) 15-bit true-color bypass	rrrgggbb ignored ignored 0rrrrrgg	ignored rrrgggbb ignored gggbbbbb	ignored ignored rrrgggbb ignored

Table 3. Color Operation Modes.

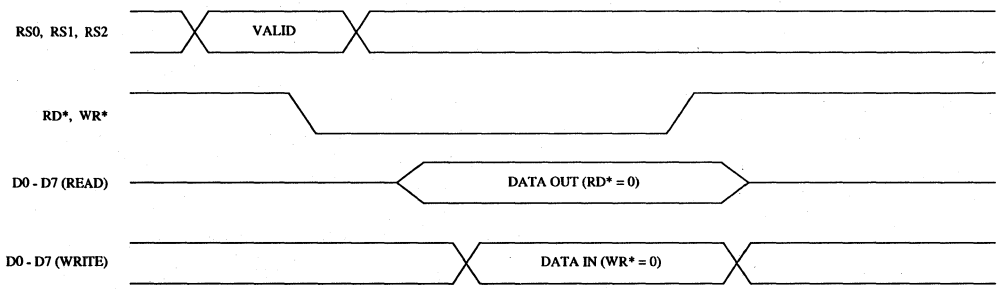


Figure 1. MPU Read/Write Timing.

Circuit Description *(continued)*

24-Bit True-Color Mode

Twenty-four bits of RGB color information may be input into the Bt473 every clock cycle. The 24 bits of pixel information are input via the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

24-Bit True-Color Bypass Mode

Twenty-four bits of pixel information may be input into the Bt473 every clock cycle. The 24 bits of pixel information are input via the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 drive the red DAC directly, G0–G7 drive the green DAC directly, and B0–B7 drive the blue DAC directly. The color palette RAMs and pixel read mask register are bypassed.

8-Bit Pseudo-Color Mode

Eight bits of pixel information may be input into the Bt473 every clock cycle. The 8 bits of pixel information (P0–P7) are input via the R0–R7, G0–G7 or B0–B7 inputs, as specified by CR7 and CR6. All three color palette RAMs are addressed by the same 8 bits of pixel data (P0–P7). Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

8-Bit True-Color Bypass Mode

Eight bits of pixel information may be input into the Bt473 every clock cycle. The 8 bits of pixel information are input via the R0–R7, G0–G7 or B0–B7 inputs, as specified by CR7 and CR6:

R0–R7 Inputs Selected	G0–G7 Inputs Selected	B0–B7 Inputs Selected	Input Format
R7	G7	B7	R7
R6	G6	B6	R6
R5	G5	B5	R5
R4	G4	B4	G7
R3	G3	B3	G6
R2	G2	B2	G5
R1	G1	B1	B7
R0	G0	B0	B6

As seen in the table, 3 bits of red, 3 bits of green, and 2 bits of blue data are input. The 3 MSBs of the red and green DACs are driven directly by the inputs, while the 2 MSBs of the blue DAC are driven directly. The 5 LSBs for the red and green DACs, and the 6 LSBs for the blue DAC, are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

15-Bit True-Color Bypass Mode

Fifteen bits of pixel information may be input into the Bt473 every clock cycle. The 15 bits of pixel information (5 bits of red, 5 bits of green, and 5 bits of blue) are input via the R0–R7 and G0–G7 inputs:

4

Pixel Inputs	Input Format
R7	0
R6	R7
R5	R6
R4	R5
R3	R4
R2	R3
R1	G7
R0	G6
G7	G5
G6	G4
G5	G3
G4	B7
G3	B6
G2	B5
G1	B4
G0	B3

The 5 MSBs of the red, green, and blue DACs are driven directly by the inputs. The 3 LSBs are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

Overlays

The overlay inputs, OL0–OL3, have priority regardless of the color mode, as shown in Table 3.

Circuit Description *(continued)*

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs. Thus, they are used only in the 24-bit true-color and 8-bit pseudo-color modes since these are the only modes that use the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0 depending on the mode). Bit D0 also corresponds to data bus bit D0. This register is not initialized. It must be initialized by the user after power-up for proper operation.

Programmable Setup

The command register specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be used.

Video Generation

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data (see figure 2), add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt473 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

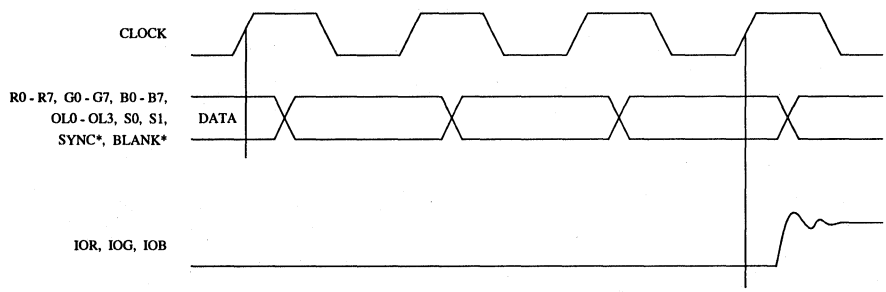
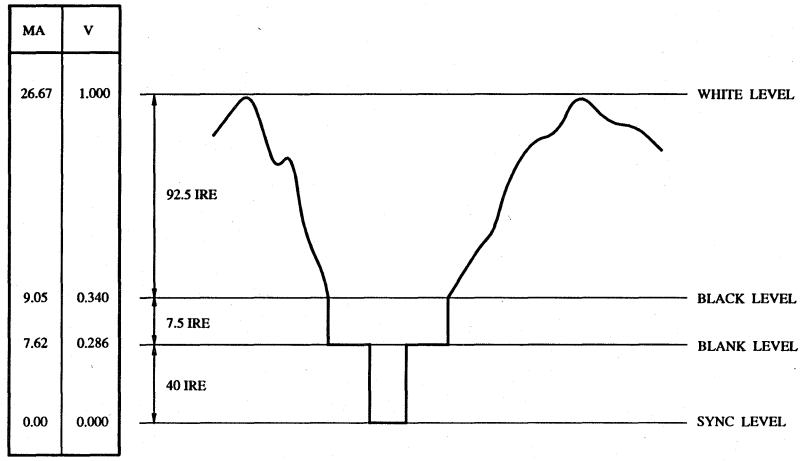


Figure 2. Video Input/Output Timing.



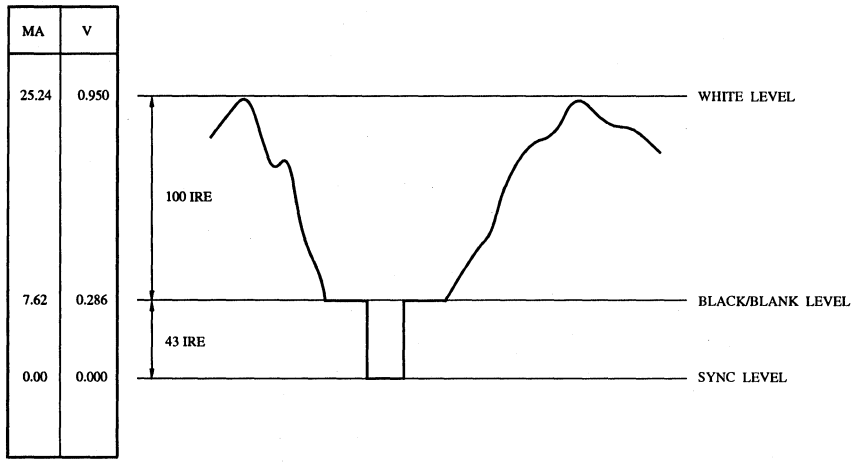
Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 140 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 26.67 mA, SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 140 Ω.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).



Note: 75 Ω doubly terminated load, SETUP = 0 IRE, VREF = 1.235 V, RSET = 140 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	25.24	1	1	$FF
DATA	data + 7.62	1	1	data
DATA - SYNC	data	0	1	data
BLACK	7.62	1	1	$00
BLACK - SYNC	0	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 25.24 mA, SETUP = 0 IRE, VREF = 1.235 V, RSET = 140 Ω.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. For proper operation, it must be initialized by the user after power-up. CR0 is the least significant bit and corresponds to D0.

CR7, CR6	Color mode select	These bits are used to control the various color modes, as shown in Table 3.
CR5	Setup select (0) 0 IRE (1) 7.5 IRE	Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal.
CR4	8-bit / 6-bit color select (0) 6-bit (1) 8-bit	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles).
CR3–CR0	CR3–CR0 outputs	These bits are output onto the CR3–CR0 pins.

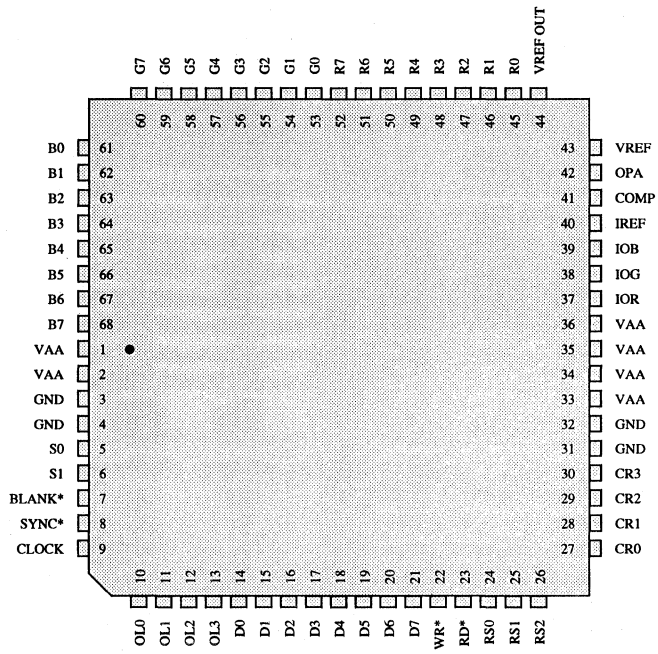
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, S0, S1, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Refer to the PC Board Layout Considerations section for critical layout criteria.
R0–R7, G0–G7, B0–B7	Red, green, and blue pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the red, green, and blue color palette RAMs is to be used to provide color information. They are latched on the rising edge of CLOCK. R0, G0, and B0 are the LSBs. Unused inputs should be connected to GND.
S0, S1	Color mode select inputs (TTL compatible). These inputs specify the mode of operation as shown in Table 3. They are latched on the rising edge of CLOCK.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the R0–R7, G0–G7, B0–B7, S0, and S1 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 5, 6, and 7).
IREF	When using a voltage reference (Figures 5 and 6), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: for SETUP = 7.5 IRE: RSET (Ω) = 3,195 * VREF (V) / Iout (mA) for SETUP = 0 IRE: RSET (Ω) = 3,025 * VREF (V) / Iout (mA) When using an external current reference (Figure 7), the relationship between IREF and the full-scale output current on each output is: for SETUP = 7.5 IRE: IREF (mA) = Iout (mA) / 3.195 for SETUP = 0 IRE: IREF (mA) = Iout (mA) / 3.025

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. If an external voltage reference is used (Figures 5 and 6), this pin should be connected to OPA. If an external current reference is used (Figure 7), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If a voltage reference is used (Figures 5 and 6), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 7), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 5 and 6. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
OPA	Reference amplifier output. If a voltage reference is used (Figures 5 and 6), this pin must be connected to COMP. When using an external current reference (Figure 7), this pin should be left floating.
VREF OUT	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating. See Figures 5 and 6. Up to four Bt473s may be driven by this output.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. See Figures 1 and 8.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. See Figures 1 and 8.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
CR0–CR3	Control outputs (TTL compatible). These outputs are used to control application-specific features. The output values are determined by the command register. See Figure 8.

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt473, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt473 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt473 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt473 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 5, 6, and 7. This bead should be located within 3 inches of the Bt473. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 5, 6, and 7 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt473 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt473 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt473 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt473 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

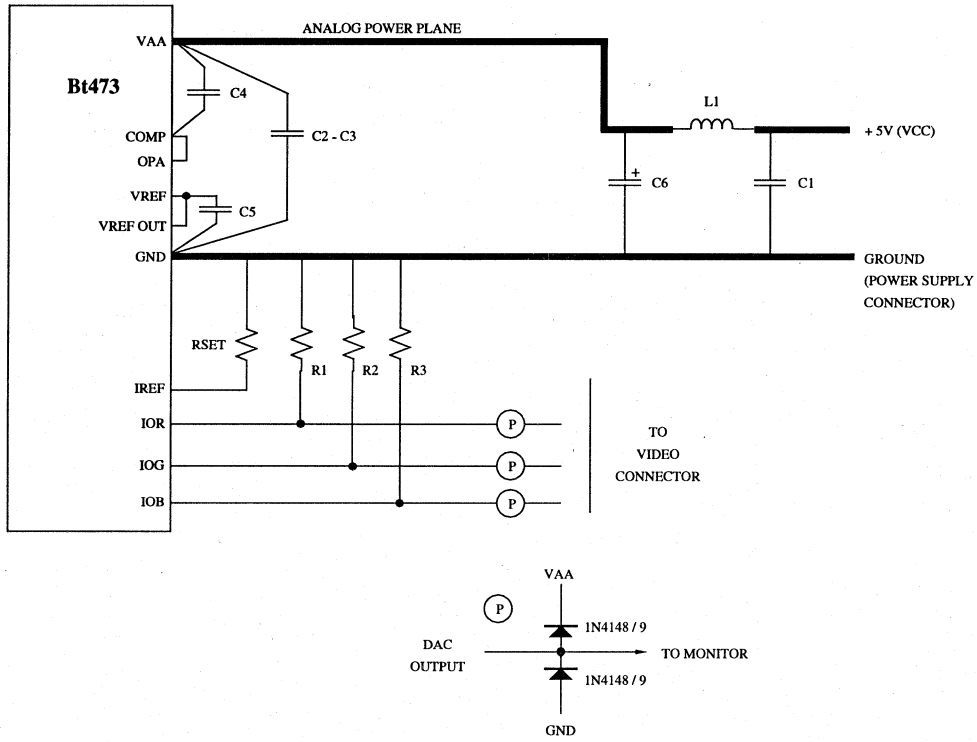
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt473 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt473 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 5, 6, and 7 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).



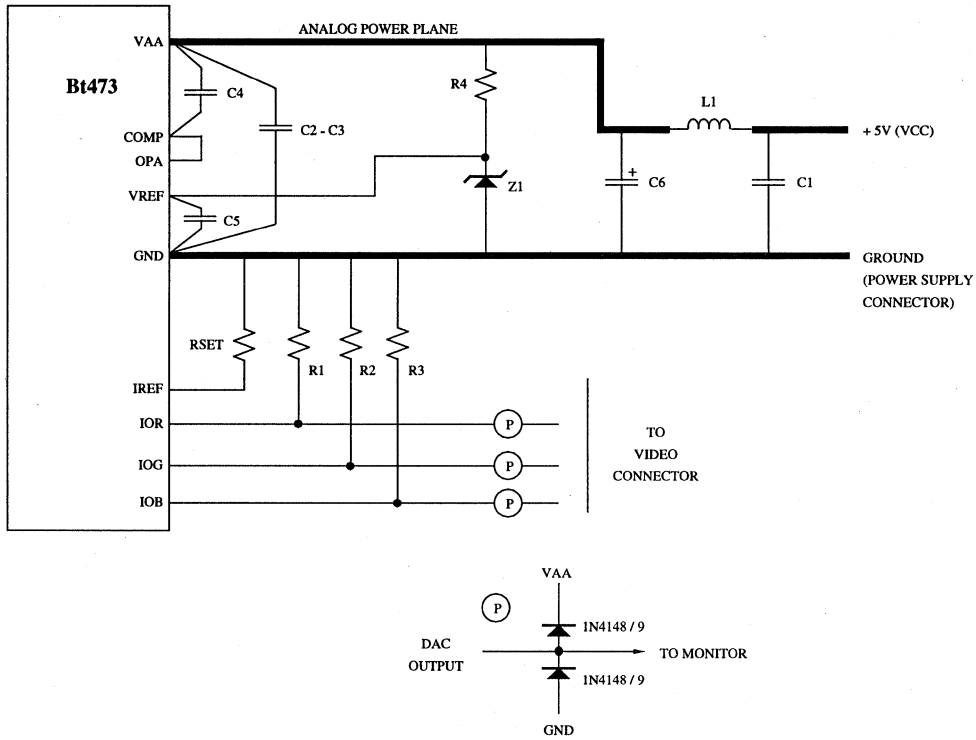
Note: For operation above 75 MHz, each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 5. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



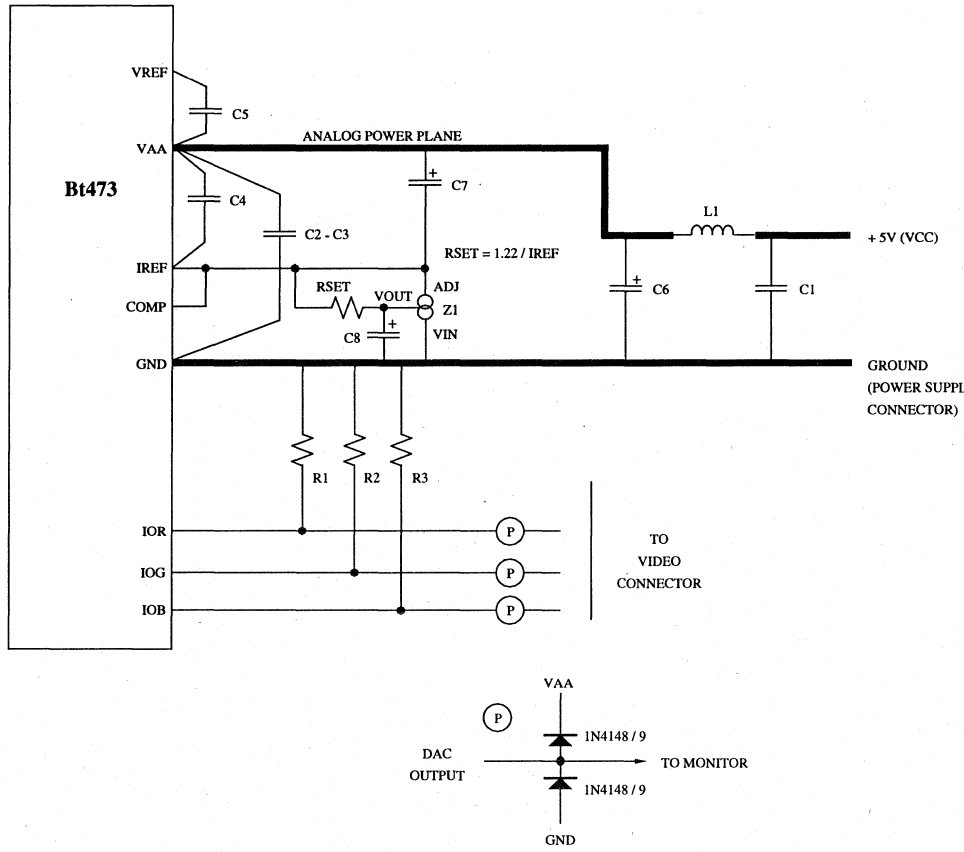
Note: For operation above 75 MHz, each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1k Ω 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 6. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: For operation above 75 MHz, each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 7. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When using multiple Bt473s, each Bt473 should have its own power plane ferrite bead.

Although the VREF OUT of a Bt473 may drive up to four Bt473s, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt473 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10x better power supply rejection on the analog outputs than an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

4

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
Using External Reference				±5	% Gray Scale
Using Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current (D0–D7)	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance	CAOUT			30	pF
(f = 1 MHz, IOUT = 0 mA)					
Voltage Reference Input Current	IVREF		10		µA
Reference Output Voltage	VREF OUT	1.08	1.2	1.32	V
Reference Output Current	IREF OUT		100		µA
Power Supply Rejection Ratio (Note 1) (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ±10% rather than the ±5% specified above.

Note 1: Guaranteed but not tested.

Analog Output Levels — PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V or external current reference with IREF = –8.88 mA.

AC Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	3			3			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0–CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	4*p14			4*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	12.5			15.15			ns
Clock Pulse Width High Time	15	4			5			ns
Clock Pulse Width Low Time	16	4			5			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time (Note 1)	19		13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	250		180	250	mA

See test conditions on next page.

AC Characteristics *(continued)*

		50 MHz Devices			35 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	3			3			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0–CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	4*p14			4*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	20			28			ns
Clock Pulse Width High Time	15	6			7			ns
Clock Pulse Width Low Time	16	6			9			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time (Note 1)	19		13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	220		180	220	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Timing Waveforms

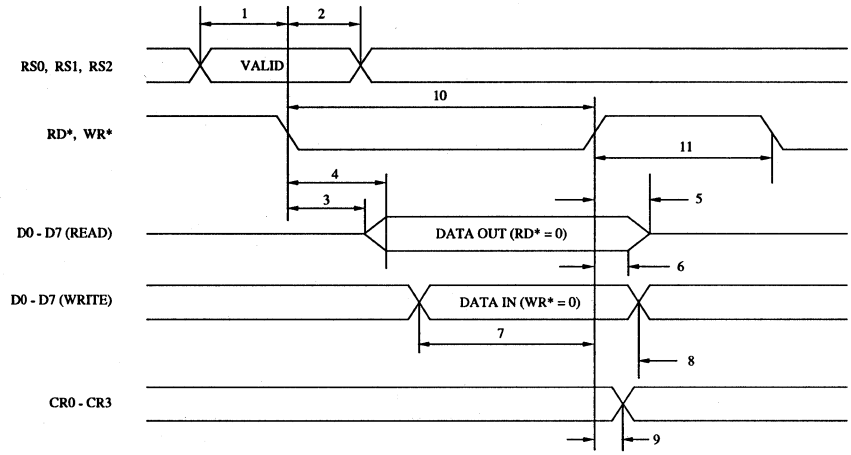
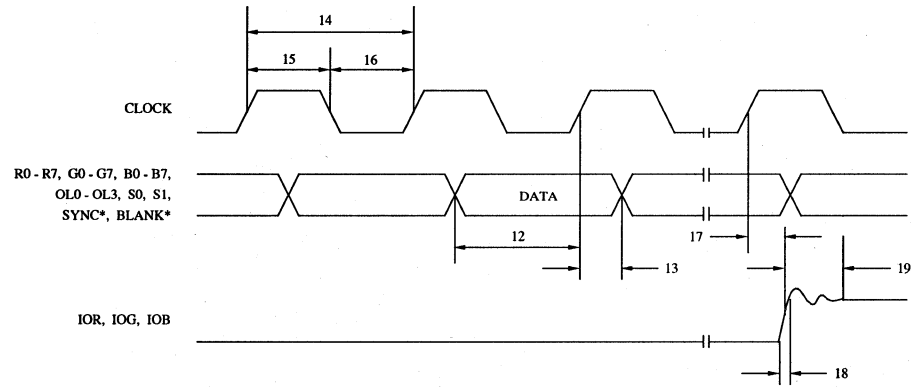


Figure 8. MPU Read/Write Timing.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 9. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt473KPJ80	80 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ66	66 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ50	50 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ35	35 MHz	68-pin Plastic J-Lead	0° to +70° C

Advance Information

This document contains information on a Rev. D product which is under development. The parametric information for Rev. D (110 MHz) devices are target parameters and are subject to change.

110 MHz

Bt473

110 MHz
Monolithic CMOS
Triple 8-bit
True-Color RAMDAC™

4

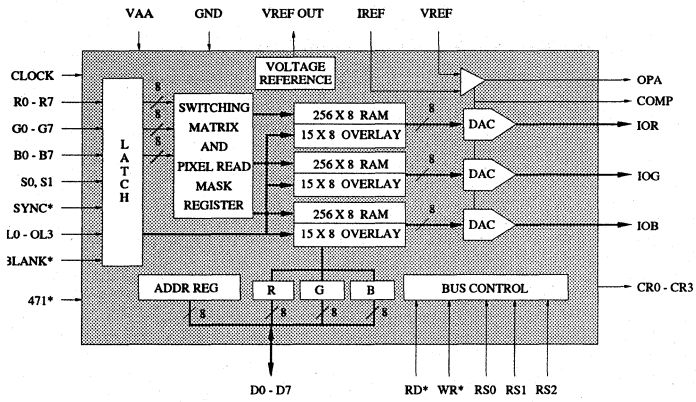
Distinguishing Features

- Bt471/478 Software Compatibility
- 110 MHz Operation
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 15 x 8 Overlay Registers
- RS-343A-Compatible Outputs
- Sync on All Three Channels
- Programmable Pedestai (0 or 7.5 IRE)
- On-Chip Voltage Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 68-pin PLCC Package
- Typical Power Dissipation: 1.1 W

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt473 true-color RAMDAC is designed specifically for true-color computer graphics. It has three 256 x 8 color lookup tables with triple 8-bit video D/A converters to support 24-bit true-color operation. In addition, 8-bit pseudo- color, 8-bit true-color, and 15-bit true-color operations are supported.

Features include a programmable pedestal (0 or 7.5 IRE) and optional on-chip voltage reference. The 15 overlay registers provide, for example, overlaying cursors, grids, menus, and EGA emulation. Also supported are a pixel read mask register and sync generation on all three channels.

An external current reference, an external voltage reference, or the internal voltage reference may be used.

The Bt473 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load. Differential and integral linearity errors are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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MPU Interface

As illustrated in the functional block diagram, the Bt473 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. (See Figure 1.)

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAMs
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register

Table 1. Control Input Truth Table.

Circuit Description *(continued)*

Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (such as, block fills of the color palette) should take place during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU. They are used to address color palette RAM locations and overlay registers, as specified in table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

8-Bit / 6-Bit Operation

The command register specifies whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros. In the 6-bit mode, the Bt473's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Bt471 Mode

The Bt473 can be forced into a Bt471 operating mode after power-up by holding the 471* external control pin low. In this mode, 8-bit pseudo-color pixel address data is enabled by R7–R0. This also forces 0 IRE setup and 6-bit DAC operation. The S0 and S1 inputs cannot override the enabled 8-bit pseudo-color (red) mode while the 471* pin is held low.

Color Modes

Four color modes are supported by the Bt473: 24-bit true color, 15-bit true color, 8-bit true color, and 8-bit pseudo color. The mode of operation is determined by the S0 and S1 inputs in conjunction with CR7 and CR6 of the command register. S0 and S1 are pipelined to maintain synchronization with the R0–R7, G0–G7, B0–B7, and OL0–OL3 pixel and overlay data inputs.

Table 3 lists the modes of operation.

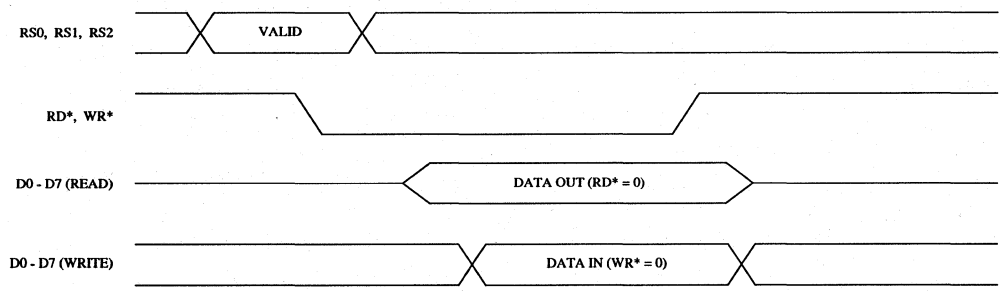


Figure 1. MPU Read/Write Timing.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10	x x x	0 0 0	1 1 1	red value green value blue value
ADDR0–7 (counts binary)	$00–$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAMs reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

OL3–OL0	S1, S0	CR7, CR6	Mode	R7–R0	G7–G0	B7–B0
1111 : 0001	xx : xx	xx : xx	overlay color 15 : overlay color 1	$xx : $xx	$xx : $xx	$xx : $xx
0000 0000 0000 0000	00 00 00 00	00 01 10 11	24-bit true color 24-bit true color 24-bit true color reserved	R7–R0 R7–R0 R7- R0 reserved	G7–G0 G7–G0 G7–G0 reserved	B7–B0 B7–B0 B7–B0 reserved
0000 0000 0000 0000	01 01 01 01	00 01 10 11	24-bit true-color bypass 24-bit true-color bypass 24-bit true-color bypass reserved	R7–R0 R7–R0 R7–R0 reserved	G7–G0 G7–G0 G7–G0 reserved	B7–B0 B7–B0 B7–B0 reserved
0000 0000 0000 0000	10 10 10 10	00 01 10 11	8-bit pseudo color (red) 8-bit pseudo color (green) 8-bit pseudo color (blue) 15-bit true color	P7–P0 ignored ignored 0rrrrrgg	ignored P7–P0 ignored gggbbbbb	ignored ignored P7–P0 ignored
0000 0000 0000 0000	11 11 11 11	00 01 10 11	8-bit true-color bypass (red) 8-bit true-color bypass (green) 8-bit true-color bypass (blue) 15-bit true-color bypass	rrrgggbb ignored ignored 0rrrrrgg	ignored rrrgggbb ignored gggbbbbb	ignored ignored rrrgggbb ignored

Table 3. Color Operation Modes.

Circuit Description *(continued)*

24-Bit True-Color Mode

Every clock cycle, 24 bits of RGB color information may be input to the Bt473. The 24 bits of pixel information are input by the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

24-Bit True-Color Bypass Mode

Every clock cycle, 24 bits of pixel information may be input to the Bt473. The 24 bits of pixel information are input by the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 drive the red DAC directly, G0–G7 drive the green DAC directly, and B0–B7 drive the blue DAC directly. The color palette RAMs and pixel read mask register are bypassed.

8-Bit Pseudo-Color Mode

Every clock cycle, 8 bits of pixel information may be input to the Bt473. The 8 bits of pixel information (P0–P7) are input by the R0–R7, G0–G7, or B0–B7 inputs, as specified by CR7 and CR6. All three color palette RAMs are addressed by the same 8 bits of pixel data (P0–P7). Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

8-Bit True-Color Bypass Mode

Every clock cycle, 8 bits of pixel information may be input to the Bt473 by the R0–R7, G0–G7, or B0–B7 inputs, as specified by CR7 and CR6:

R0–R7 Inputs Selected	G0–G7 Inputs Selected	B0–B7 Inputs Selected	Input Format
R7	G7	B7	R7
R6	G6	B6	R6
R5	G5	B5	R5
R4	G4	B4	G7
R3	G3	B3	G6
R2	G2	B2	G5
R1	G1	B1	B7
R0	G0	B0	B6

As specified in the above table, 3 bits of red, 3 bits of green, and 2 bits of blue data are input. The 3 MSBs of the red and green DACs are driven directly by the inputs, while the 2 MSBs of the blue DAC are driven directly. The 5 LSBs for the red and green DACs, and the 6 LSBs for the blue DAC, are logical zeros. The color palette RAMs and pixel read mask register are bypassed.

15-Bit True-Color Mode

Every clock cycle, 15 bits of pixel information may be input to the Bt473. The 15 bits of pixel information (5 bits each of red, green, and blue) are input by the R0–R7 and G0–G7 inputs, as specified in the pixel table below. Five LSBs from red, green, and blue address 32 locations of each corresponding RAM. R6–R2 address 32 locations of the red color palette RAM; R1, R0, G7, G6, and G5 address 32 locations of the green color palette RAM, and G5–G0 address 32 locations of the blue color palette RAM. The 3 MSBs of red, green, and blue are forced to zero. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

15-Bit True-Color Bypass Mode

Every clock cycle, 15 bits of pixel information (5 bits each of red, green, and blue) may be input to the Bt473 by the R0–R7 and G0–G7 inputs as specified below.

The 5 MSBs of the red, green, and blue DACs are driven directly by the inputs. The 3 LSBs are logical zeros. The color palette RAMs and pixel read mask register are bypassed.

Pixel Inputs	Input Format
R7	0
R6	R7
R5	R6
R4	R5
R3	R4
R2	R3
R1	G7
R0	G6
G7	G5
G6	G4
G5	G3
G4	B7
G3	B6
G2	B5
G1	B4
G0	B3

Circuit Description *(continued)*

Overlays

The overlay inputs, OL0–OL3, have priority regardless of the color mode, as detailed in Table 3.

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs. Thus, they are used only in the 24-bit true-color and 8-bit pseudo-color modes, since these are the only modes that use the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the 8-bit inputs before addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0, depending on the mode). Bit D0 also corresponds to data bus bit D0.

The Pixel read mask register is not initialized. For proper operation, it must be initialized by the user after power-up.

Programmable Setup

The command register specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be used.

Video Generation

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data (see Figure 2), add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt473 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

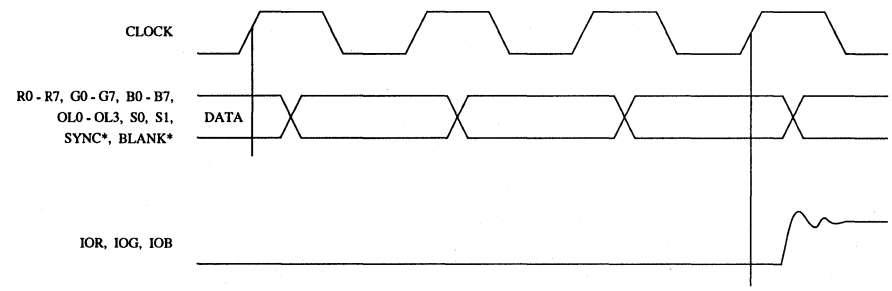
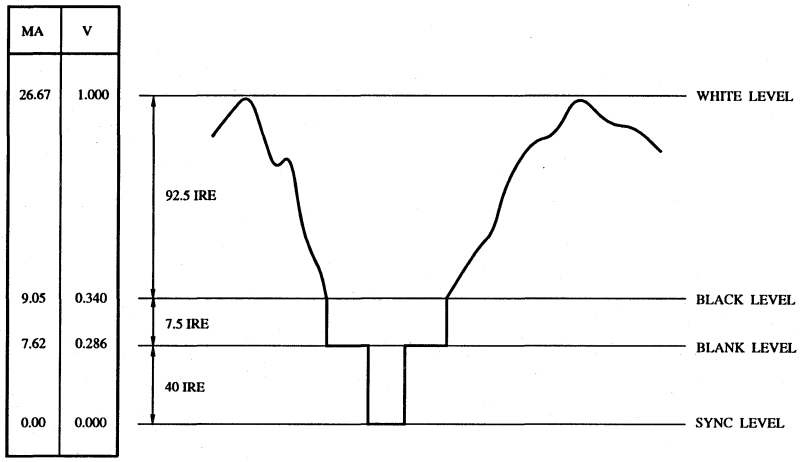


Figure 2. Video Input/Output Timing.

Circuit Description *(continued)*



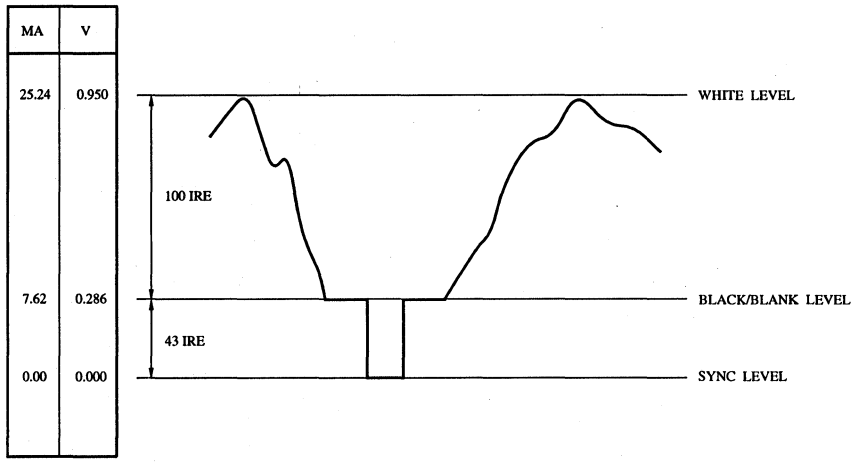
Note: 75 Ω doubly-terminated load, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 26.67 mA, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 143 Ω.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).



Note: 75 Ω doubly-terminated load, SETUP = 0 IRE, VREF = 1.235 V, and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	25.24	1	1	$FF
DATA	data + 7.62	1	1	data
DATA - SYNC	data	0	1	data
BLACK	7.62	1	1	$00
BLACK - SYNC	0	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 25.24 mA, SETUP = 0 IRE, VREF = 1.235 V, and RSET = 143 Ω.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power-up for proper operation. CR0 is the least significant bit and corresponds to D0.

CR7, CR6	Color mode select	These bits are used to control the various color modes, as specified in Table 3.
CR5	Setup select (0) 0 IRE (1) 7.5 IRE	This bit is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal.
CR4	8-bit / 6-bit color select (0) 6 bits (1) 8 bits	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and logical zeros during color read cycles).
CR3–CR0	CR3–CR0 outputs	These bits are output onto the CR3–CR0 pins.

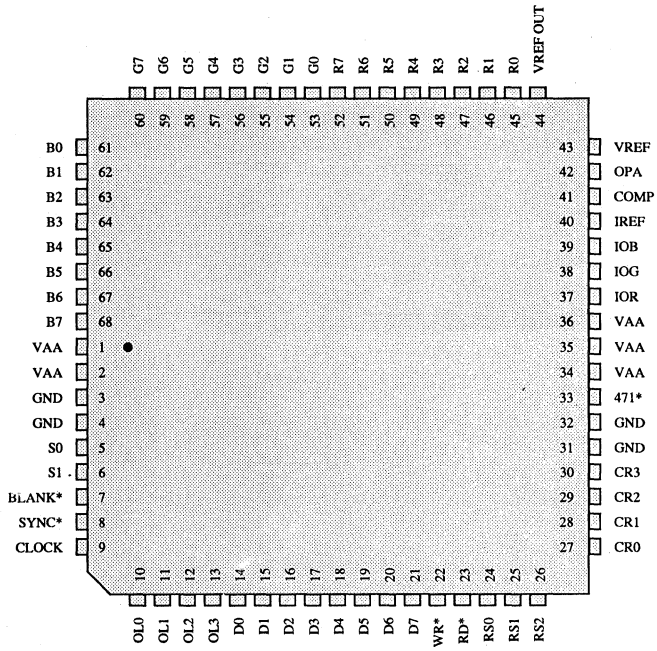
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as detailed in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). SYNC does not override any other control or data input; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, S0, S1, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Refer to the PC Board Layout Considerations section for critical layout criteria.
R0–R7, G0–G7, B0–B7	Red, green, and blue pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the red, green, and blue color palette RAMs is to be used to provide color information. These inputs are latched on the rising edge of CLOCK. R0, G0, and B0 are the LSBs. Unused inputs should be connected to GND.
S0, S1	Color mode select inputs (TTL compatible). These inputs specify the mode of operation as detailed in Table 3. They are latched on the rising edge of CLOCK.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as detailed in Table 3. When accessing the overlay palette, the R0–R7, G0–G7, B0–B7, S0, and S1 inputs are ignored. OL0–OL3 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figures 5, 6, and 7 in the PC Board Layout Considerations section).
IREF	Full-scale adjust control. When voltage reference is used (Figures 5 and 6), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = K*1000 * VREF (V) / Iout (mA) K is defined in the table and note below. Pedestal / K (with SYNC) / K (without SYNC): 7.5 IRE: 3.063 / 2.205 0 IRE: 2.898 / 2.040 When an external current reference is used (Figure 7), the relationship between IREF and the full-scale output current on each output is: IREF (mA) = Iout (mA) / K *Note :* The K values in this table represent an ideal DAC circuit. However, because of a small difference (~3 percent) between the actual drain-source voltages on the DAC output transistor and the rederence transistor, an RSET value of 143 Ω is recommended.

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. If an external voltage reference is used (Figures 5 and 6), this pin should be connected to OPA. If an external current reference is used (Figure 7), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. The PC Board Layout Considerations section contains critical layout criteria.
VREF	Voltage reference input. If a voltage reference is used (Figures 5 and 6), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 7), this pin should be biased with the VREF OUT pin. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 5, 6, and 7. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor. Refer to the PC Board Layout Considerations section for critical layout criteria.
OPA	Reference amplifier output. If a voltage reference is used (Figures 5 and 6), this pin must be connected to COMP. When an external current reference is used (Figure 7), this pin should be left floating.
VREF OUT	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating in external voltage reference mode. (See Figure 6.) Up to four Bt473s may be driven by this output.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. (See Figure 1, and Figure 8 in the Timing Waveforms section.)
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. (See Figures 1 and 8.)
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as shown in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
CR0–CR3	Control outputs (TTL compatible). These outputs are used to control application-specific features. The output values are determined by the command register. (See Figure 8.)
471*	This pin forces the device into a Bt471 operating mode (i.e., it enables 8-bit pseudo-color mode with R7–R0, 0 IRE setup, and 6-bit DAC operation). This pin must be held at a logical-zero level to maintain this mode of operation.

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt473, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt473 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt473 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt473 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 5, 6, and 7. This bead should be located within 3 inches of the Bt473. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optim83 ·œerformance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 5, 6, and 7 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt473 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt473 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

For 110 MHz operation, the clock signal requires a constant impedance line between the clock driver and the clock input pin. This signal should be driven by a dedicated driver, and should be terminated at the device input pin. At 110 MHz, CLOCK rise/fall times should be controlled to maximize the clock high and low times. This will help minimize duty cycle skew.

MPU Control Signal Interfacing

The Bt473 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt473 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt473 to minimize reflections. Unused analog outputs should be connected to GND.

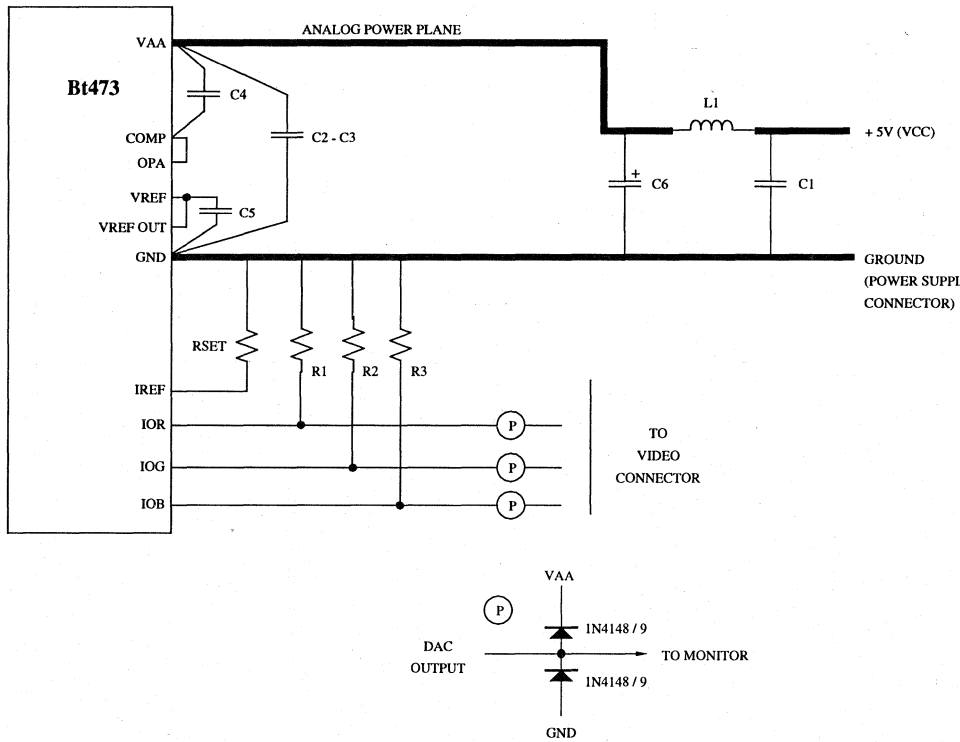
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt473 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors. The diode protection circuit shown in Figures 5, 6, and 7

PC Board Layout Considerations *(continued)*

can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).



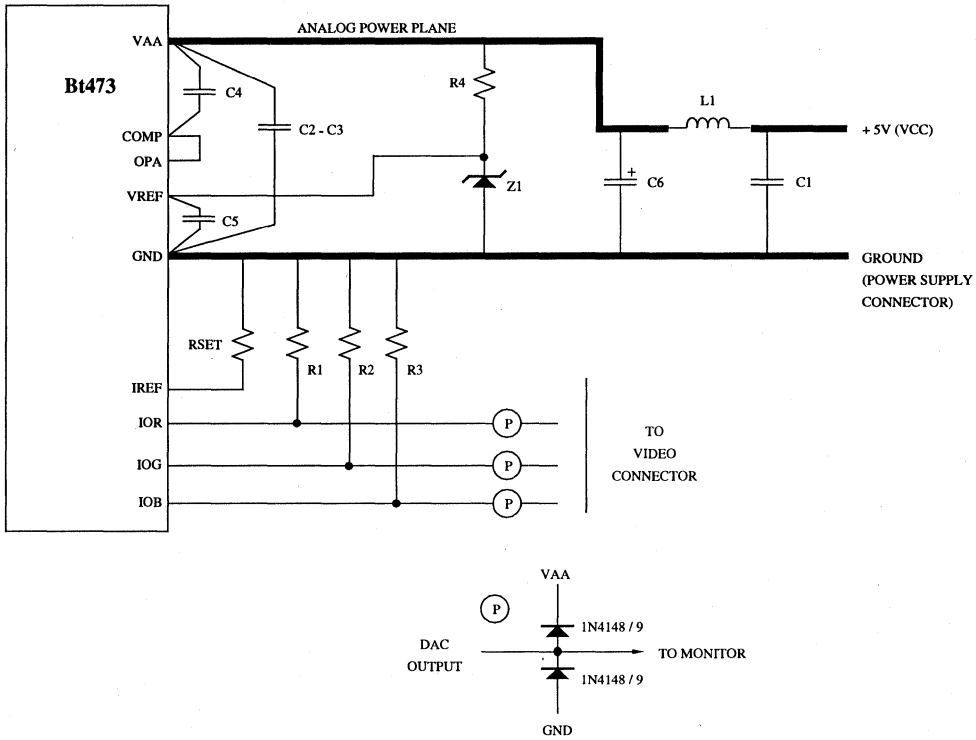
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 5. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



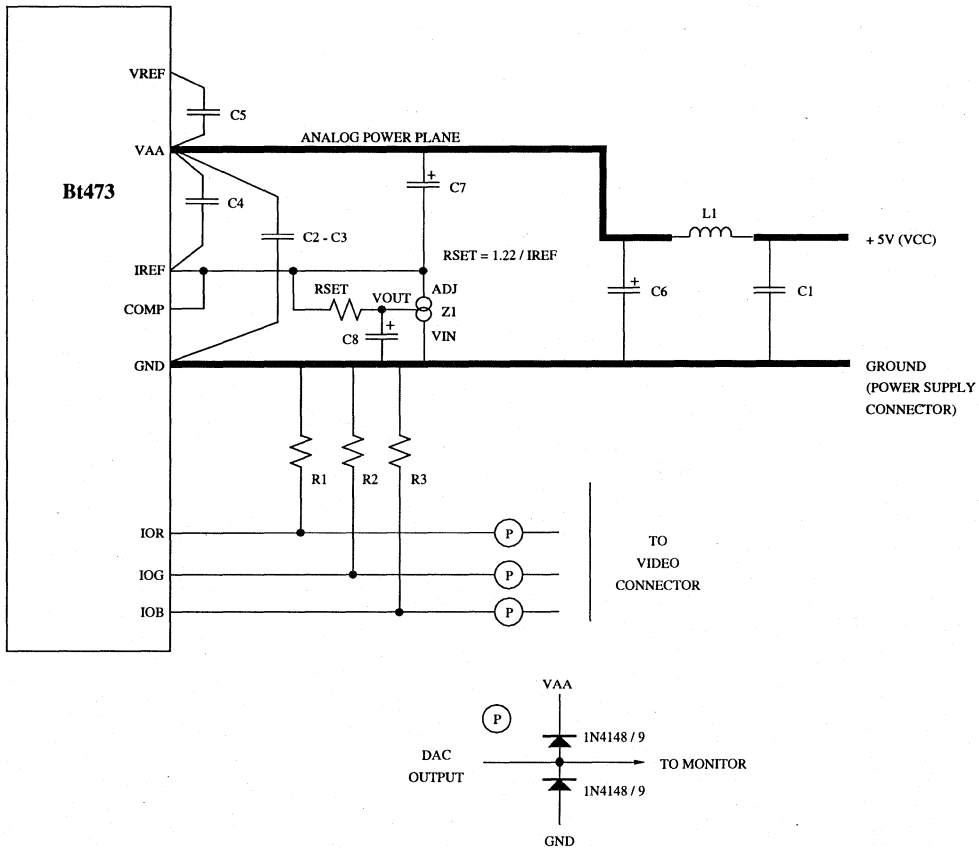
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1– C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 6. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 7. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When multiple Bt473s are being used, each Bt473 should have its own power plane ferrite bead.

Although the VREF OUT of a single Bt473 may drive multiple Bt473s, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt473 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
110, 80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.12	1.235	1.358	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A			–8.39		mA
PS/2 Compatible			–8.88		mA

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error					
Using External Reference				±5	% Gray Scale
Using Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current (D0–D7)	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
VREF Input Current	IREF IN		10		µA
VREF OUT Output Voltage	VREFOUT	1.08	1.2	1.32	V
VREF OUT Output Current	IREF OUT		100		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Analog Output Levels—PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2-compatible video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V; or external current reference with IREF = –8.88 mA.

AC Characteristics

Parameter	Symbol	110 MHz Devices Min	Typ	Max	Units
Clock Rate	Fmax			110	MHz
RS0–RS2 Setup Time	1	10			ns
RS0–RS2 Hold Time	2	10			ns
RD* Asserted to Data Bus Driven	3	3			ns
RD* Asserted to Data Valid	4			40	ns
RD* Negated to Data Bus 3-Stated	5			20	ns
Read Data Hold Time	6	3			ns
Write Data Setup Time	7	10			ns
Write Data Hold Time	8	10			ns
CR0–CR3 Output Delay	9			100	ns
RD*, WR* Pulse Width Low	10	50			ns
RD*, WR* Pulse Width High	11	6*p14			ns
Pixel and Control Setup Time	12	3			ns
Pixel and Control Hold Time	13	3			ns
Clock Cycle Time (p14)	14	9.1			ns
Clock Pulse Width High Time	15	4			ns
Clock Pulse Width Low Time	16	4			ns
Analog Output Delay	17			30	ns
Analog Output Rise/Fall Time	18		2		ns
Analog Output Settling Time (Note 1)	19		13		ns
Clock and Data Feedthrough (Note 1)			–30		dB
Glitch Impulse (Note 1)			150		pV-sec
DAC-to-DAC Crosstalk			–23		dB
Analog Output Skew			0	2	ns
Pipeline Delay		4	4	4	Clocks
VAA Supply Current (Note 2)	IAA				
At 0° C			260	300	mA
At 70° C			230	270	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Timing Waveforms

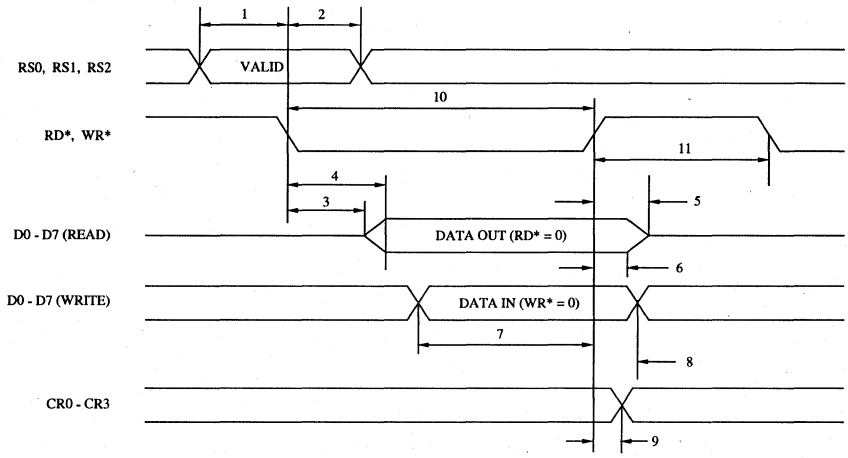
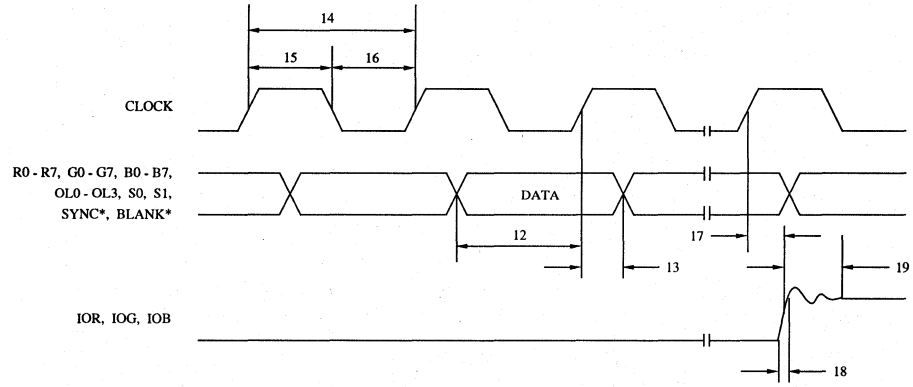


Figure 8. MPU Read/Write Timing Dimensions.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 9. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt473KPJ110	110 MHz	68-pin Plastic J-Lead	0° to +70° C

Bt475

Bt477

110 MHz
256-Word Color Palette
Personal System/2®
Power-Down RAMDAC™

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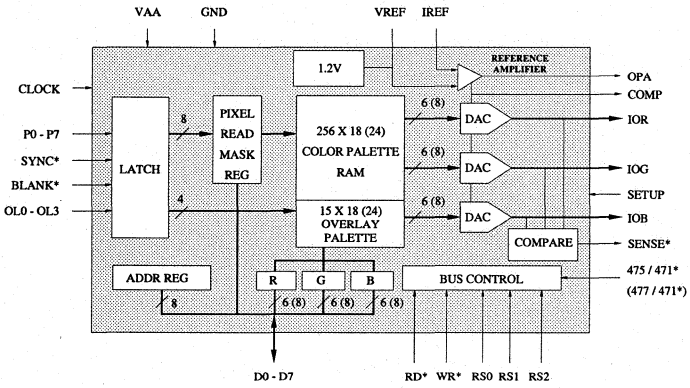
Distinguishing Features

- 110, 80, 66, 50, 35 MHz Operation
- Bt471/476/478 Pin Compatibility
- Power-Down Mode
- Antisparkle Circuitry
- Analog Output Comparators
- Triple 6-bit (8-bit) D/A Converters
- 256 x 18 (24) Color Palette RAM
- RS-343A/RS-170-Compatible Outputs
- 15 x 18 (24) Overlay Registers
- Programmable Pedestal
- Optional Internal Reference
- 44-pin PLCC Package

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Laptop Computers

Functional Block Diagram



Product Description

The Bt475 and Bt477 RAMDACs are designed specifically for Personal System/2®-compatible color graphics.

The Bt475 has a 256 x 18 lookup table RAM, 15 x 18 overlay registers, and triple 6-bit D/A converters.

The Bt477 has a 256 x 24 lookup table RAM, 15 x 24 overlay registers, and triple 8-bit D/A converters. Both 6-bit and 8-bit color modes are supported.

On-chip analog output comparators are included to simplify diagnostics and debugging with the result output onto the SENSE* pin. An on-chip voltage reference is also included to simplify use of the device.

A power-down mode is available to reduce power requirements when the analog outputs are not used. This is useful in laptop computer systems that need the option of driving an external RGB monitor.

When the 475/471* input pin (477/471* on the Bt477) is floating or a logical zero, the Bt475 and Bt477 behave as a Bt471 with antisparkle capabilities, on-chip reference, and analog comparators. When the pin is a logical one, the additional capabilities of the command register are available.

Note: "Personal System/2®"and "PS/2®" are registered trademarks of IBM.

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Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt475/477 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into an 18-bit or 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to se-

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register (Note 1)

Note 1: Available only when the 475/471* (477/471*) pin is a logical one.

Table 1. Control Input Truth Table.

lect the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Additional Information

When the color palette RAM is accessed, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While the overlay color registers are accessed, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic. These data transfers take place during the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU. They are used to address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

The pixel clock must be active for MPU accesses to the color palette RAM.

Bt471-Compatible Operation

If the 475/471* (477/471*) pin is a logical zero, the Bt475/477 operates as a Bt471 RAMDAC; the command register is disabled, and 6-bit operation is selected. Color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

In the 6-bit mode, the Bt477's full scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

If the 475/471* (477/471*) input is a logical one, the command register is available. On the Bt477, the 6-bit/8-bit select bit in the command register may be used to specify whether 6-bit or 8-bit color data values are being used.

8-bit / 6-bit Color Selection

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

In the 6-bit mode, the Bt477's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description *(continued)*

Power-Down Mode

The Bt475/477 incorporates a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt475/477 functions normally. The SLEEP enable bit is not initialized on power-up and must be a logical zero for normal operation.

While the SLEEP bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may still be read or written to while sleeping as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed.

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn the current reference off (IREF = 0 mA) during sleep mode.

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level of the SENSE comparator circuit. This output is used to determine the presence of a CRT monitor. Also with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For proper operation of the SENSE circuit, the following levels should be applied to the comparator through the IOR, IOG, and IOB outputs:

DAC Low Voltage ≤ 325 mV
DAC High Voltage ≥ 395 mV

There is an additional ±10-percent tolerance on the above levels when the internal voltage reference or an external current reference is used. SYNC* should be a logical zero for SENSE* to be stable. Also, the SENSE output can drive only one CMOS load.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits (Bt475) or 24 bits (Bt477) of color information to the three D/A converters. For proper operation, the pixel read mask register must be initialized by the user after power-up.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 1–3. Tables 4–6 detail how the SYNC* and BLANK* inputs modify the output levels.

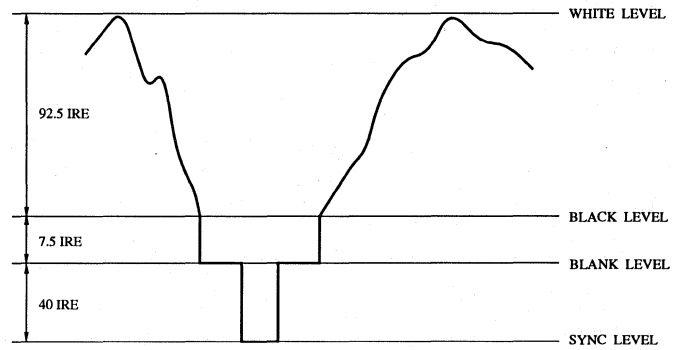
The SETUP input pin is logically ANDed with the SETUP command bit and is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used.

The analog outputs of the Bt475/477 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

OL0–OL3	P0–P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

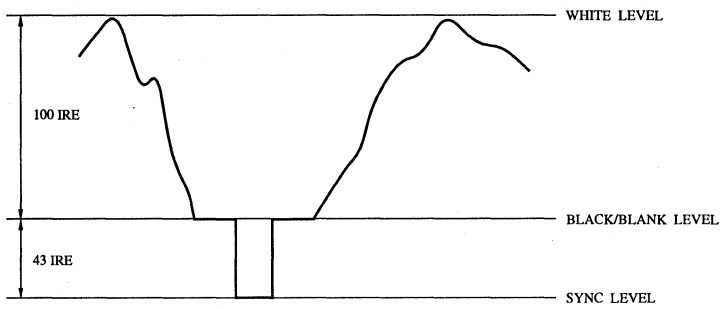
Figure 1. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 2. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE).

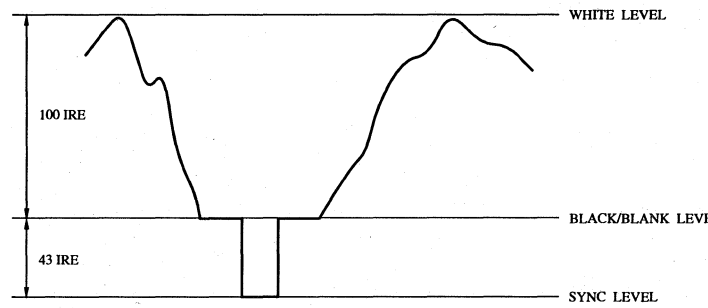
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Command Register

This register is operational only while the 475/471* (477/471*) pin is a logical one. It may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

D7	reserved (logical zero)	A logical zero must be written to this bit when writing to the command register to ensure proper operation.
D6	reserved (logical one)	A logical one must be written to this bit when writing to the command register to ensure proper operation.
D5	SETUP select (0) 0 IRE (1) 7.5 IRE	This bit specifies whether the blanking pedestal is 0 or 7.5 IRE. This bit is logically ANDed with the 475/471* (477/471*) input pin. Bit D5 controls the blanking pedestal only when in 475 (477) mode. The SETUP pin is disabled when it is operating inside this register.
D4	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output is to contain sync information.
D3	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output is to contain sync information.
D2	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output is to contain sync information.

Command Register (continued)

D1	6-bit / 8-bit select (0) 6-bit (1) 8-bit	On the Bt477, this bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. On the Bt475, this bit must be a logical zero to ensure proper 6-bit operation.
D0	SLEEP enable (0) normal operation (1) sleep mode	While this bit is a logical zero, the Bt475/477 functions normally. The SLEEP enable must be initialized after power-up for normal operation. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may be read or written to as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. About 1 second is required for the Bt475/477 to output valid video data after enabling normal operation (coming out of sleep mode). This time will vary according to the size of the COMP capacitor. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If the DACs are using an external current reference, external circuitry should turn the current reference off during sleep mode. To further reduce power consumption in SLEEP mode, the pixel clock should be disabled while in SLEEP.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 4, 5, and 6. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). SETUP is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Clock Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 - OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as detailed in Table 3. When the overlay palette is accessed, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external or the internal voltage reference is used (Figures 4 and 5 in the PC Board Layout Considerations section), this pin should be connected to OPA. If an external current reference is used (Figure 6 in the PC Board Layout section), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating. However, the bypass capacitor should still be connected. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 4 and 5. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry other than the decoupling capacitor (Figure 4).
OPA	Reference amplifier output. If an external or the internal voltage reference is used (Figures 4 and 5), this pin must be connected to COMP. When an external current reference is used (Figure 6), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figures 4, 5, and 6).
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>IREF</td><td>Full-scale adjust control. The IRE relationships in Figures 1, 2, and 3 are maintained regardless of the full-scale output current.

When an external or the internal voltage reference is used (Figures 4 and 5), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

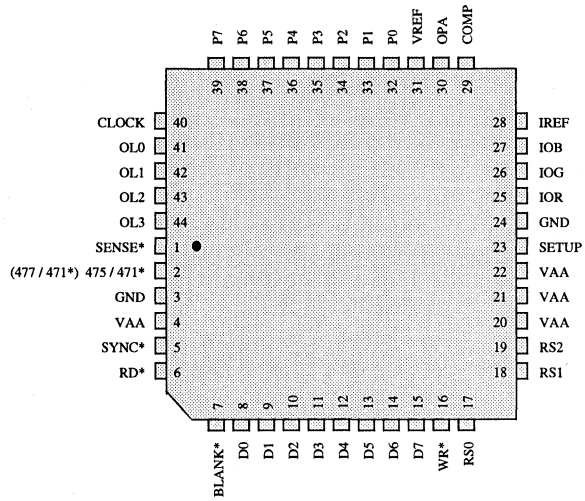
K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

When an external current reference is used (Figure 6), the relationship between IREF and the full-scale output current on each output is:

IREF (mA) = Iout (mA) / K

<table>
<tr><th>Part</th><th>Mode</th><th>Pedestal</th><th>K (with sync)</th><th>K (without sync)</th></tr>
<tr><td>Bt477</td><td>6-bit</td><td>7.5 IRE</td><td>3.013</td><td>2.170</td></tr>
<tr><td></td><td>8-bit</td><td>7.5 IRE</td><td>3.049</td><td>2.196</td></tr>
<tr><td></td><td>6-bit</td><td>0 IRE</td><td>2.852</td><td>2.010</td></tr>
<tr><td></td><td>8-bit</td><td>0 IRE</td><td>2.886</td><td>2.034</td></tr>
<tr><td>Bt475</td><td>(6-bit)</td><td>7.5 IRE</td><td>3.013</td><td>2.170</td></tr>
<tr><td></td><td></td><td>0 IRE</td><td>2.852</td><td>2.010</td></tr>
</table>
</td></tr>
<tr><td>WR*</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.</td></tr>
<tr><td>RD*</td><td>Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as shown in Tables 1 and 2. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>475/471*
(477/471*)</td><td>Bt475 (Bt477) or Bt471 select input (TTL compatible). When the 475/471* (477/471*) input pin is floating or a logical zero, the Bt475/477 behaves as a Bt471 with antisparkle capabilities. When the 475/471* (477/471*) input pin is a logical one, the extra capabilities of the Bt475/477 command register are available.</td></tr>
<tr><td>SENSE*</td><td>Sense output (CMOS levels). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level. SENSE* may not be stable while SYNC* is toggling. Also, the SENSE* output can drive only one CMOS load.</td></tr>
</table>

Pin Descriptions *(continued)*



Names in parentheses are pin names for the Bt477.

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt475 and Bt477, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt475 and Bt477 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt475 and Bt477 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt475 and Bt477 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within 3 inches of the Bt475 and Bt477. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 4, 5, and 6 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt475 and Bt477 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt475 and Bt477 require a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt475 and Bt477 use the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt475 and Bt477 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt475 and Bt477 to minimize reflections. Unused analog outputs should be connected to GND.

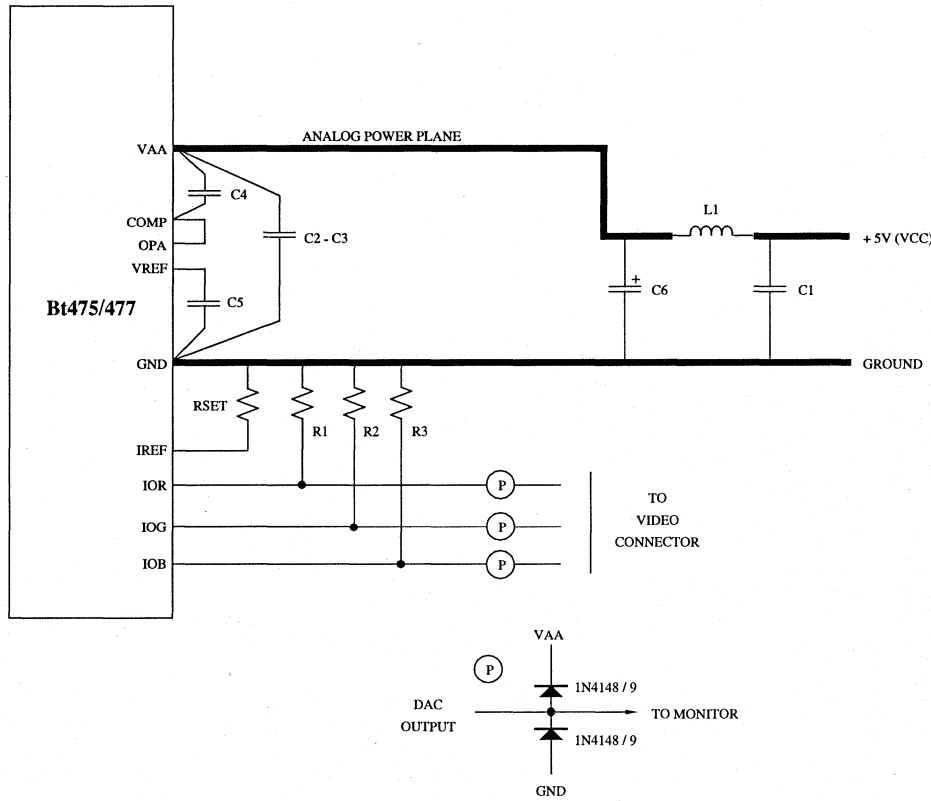
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt475 and Bt477 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



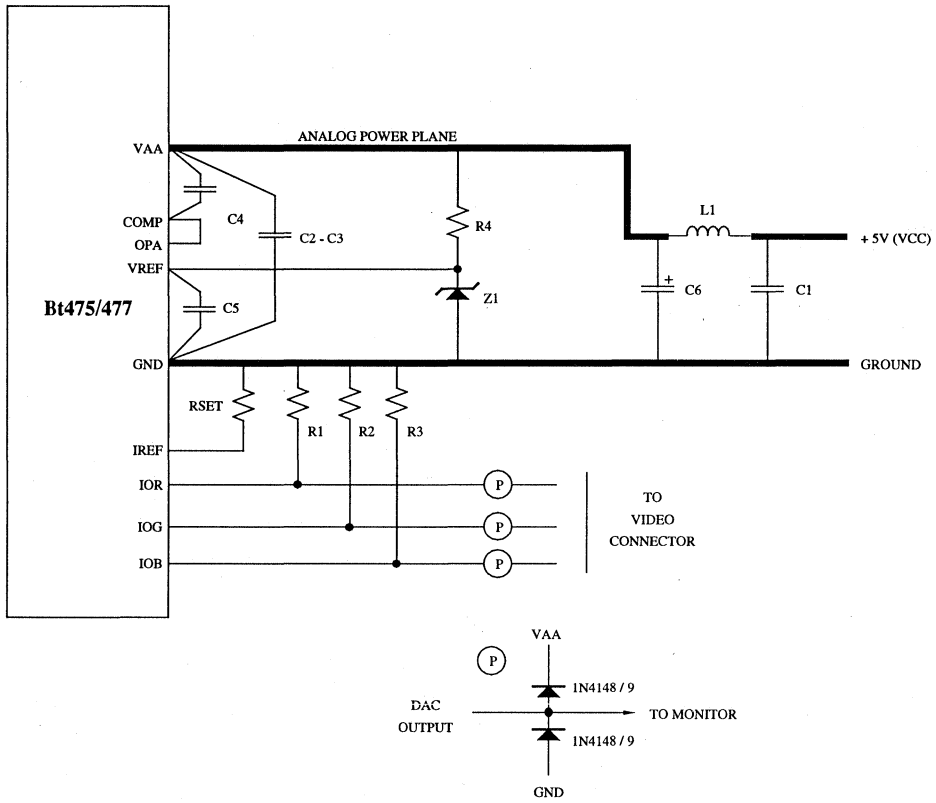
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 4. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



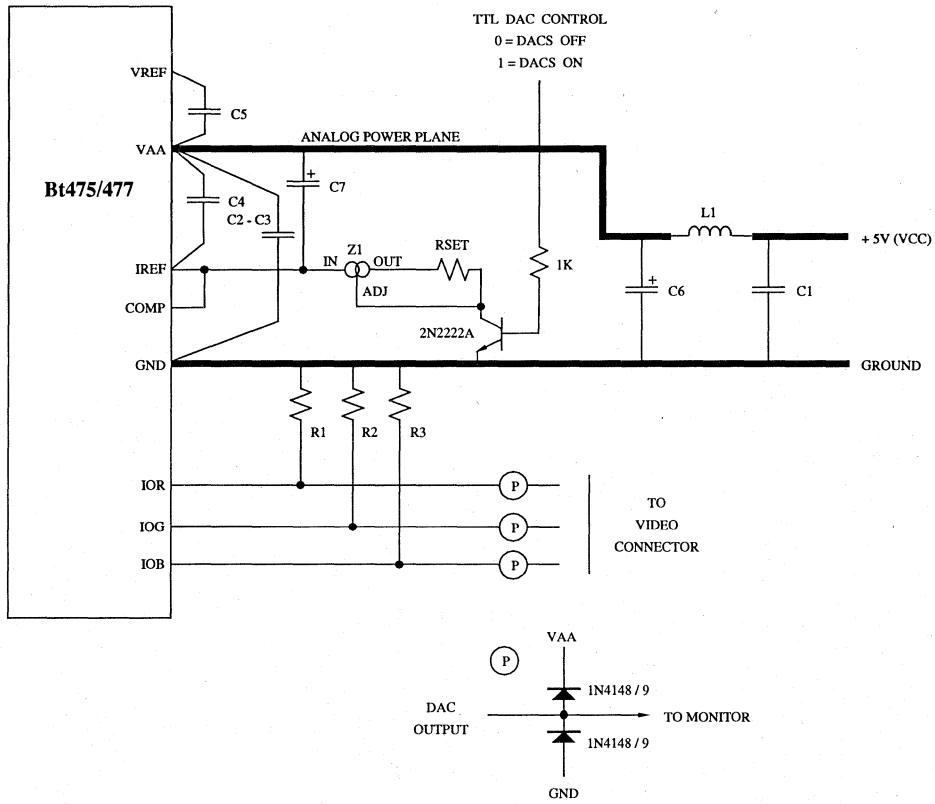
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	—
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 5. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM317LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 6. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When multipl112112:d475/477s are used, each Bt475/477 should share a common power plane with one ferrite bead. If the internal reference is used, each Bt475/477 should use its own.

Although the multiple Bt475/477s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAM-DAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt475/477 must have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

When an external current reference is used, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 6, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode. The SLEEP enable bit is not initialized on power-up and must be a logical zero for normal operation.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
110, 80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt475		6	6	6	Bits
Bt477		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt475				±1/4	LSB
Bt477				±1	LSB
Differential Linearity Error	DL				
Bt475				±1/4	LSB
Bt477				±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current					
White Level Relative to Black (Note 1)		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size					
Bt475			279.68		µA
Bt477			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Internal Reference Output	VREF	1.11	1.235	1.36	V
Power Supply Rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 475/471* (477/471*) pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: Since the Bt475 has 6-bit DACs (and the Bt477 when in the 6-bit mode), the output levels are approximately 1.5-percent lower than these values.

Note 2: Guaranteed by characterization, not tested.

AC Characteristics

		110 MHz Devices			80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			110			80			66	MHz
RS0–RS2 Setup Time	1	3			3			3			ns
RS0–RS2 Hold Time	2	3			3			3			ns
RD* Asserted to Data Bus Driven	3	5			5			5			ns
RD* Asserted to Data Valid	4			40			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20			20	ns
Read Data Hold Time	6	5			5			5			ns
Write Data Setup Time	7	10			10			10			ns
Write Data Hold Time	8	3			3			3			ns
RD*, WR* Pulse Width Low	9	50			50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			3			ns
Pixel and Control Hold Time	12	3			3			3			ns
Clock Cycle Time (p13)	13	9			12.5			15.15			ns
Clock Pulse Width High Time	14	4			4			5			ns
Clock Pulse Width Low Time	15	4			4			5			ns
Analog Output Delay	16			30			30			30	ns
Analog Output Rise/Fall Time	17			3			3			3	ns
Analog Output Settling Time (Note 1)	18		13			13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30			–30		dB
Glitch Impulse (Note 1)			75			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23			–23		dB
Analog Output Skew				2			2			2	ns
SENSE* Output Delay	19		1			1			1		µS
Pipeline Delay		4			4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)											
normal operation			220	280		180	240		180	240	mA
sleep enabled (Note 3)			1	1.5		1	1.5		1	1.5	mA

See test conditions and the notes at the end of this section.
See, also, Figures 7 and 8.

AC Characteristics *(continued)*

		50 MHz Devices			35 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	3			3			ns
RS0–RS2 Hold Time	2	3			3			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	3			3			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17			3			3	ns
Analog Output Settling Time (Note 1)	18		20			28		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA							
normal operation			180	240		180	240	mA
sleep enabled (Note 3)			1	1.5		1	1.5	mA

See test conditions and notes on next page.
See, also, Figures 7 and 8.

4

AC Characteristics *(continued)*

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 475/471* (477/471*) pin = logical one. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points are at 50 percent for inputs and outputs. Analog output load ≤ 10 pF. SENSE*, D0–D7 output load ≤ 75 pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Note 3: External current or voltage reference is disabled during sleep mode, and pixel clock is inhibited. Guaranteed by characterization, not tested.

Timing Waveforms

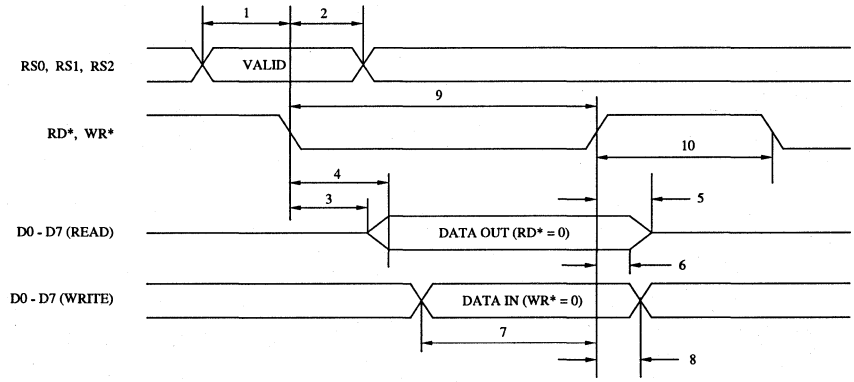
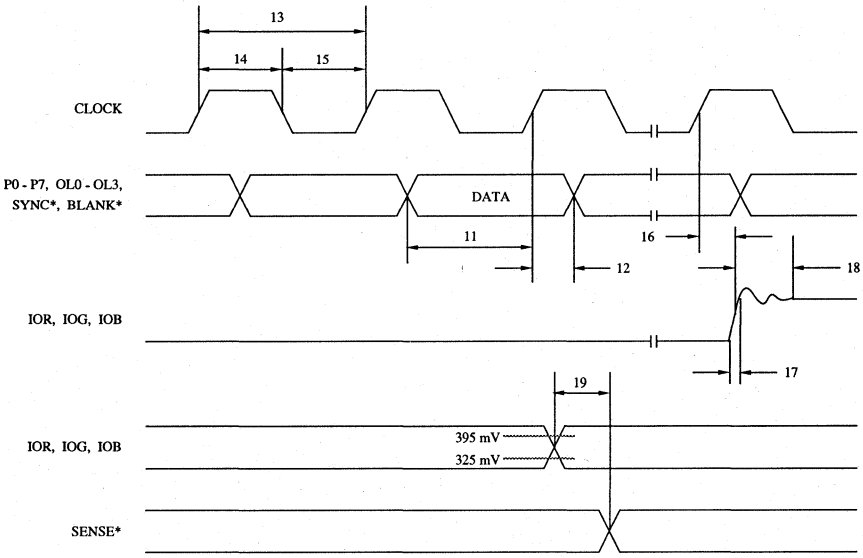


Figure 7. MPU Read/Write Timing.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full scale transition to the output remaining within ±1 LSB (Bt477) or ±1/4 LSB (Bt475).

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. Video Input/Output Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Speed	Package	Ambient Temperature Range
Bt475KPJ80	256 x 18	15 x 18	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ66	256 x 18	15 x 18	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ50	256 x 18	15 x 18	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ35	256 x 18	15 x 18	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ110	256 x 24	15 x 24	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ80	256 x 24	15 x 24	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ66	256 x 24	15 x 24	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ50	256 x 24	15 x 24	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ35	256 x 24	15 x 24	35 MHz	44-pin Plastic J-Lead	0° to +70° C

Preliminary Information

This document contains information on new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 85 and 75 MHz Operation
- Supports 8:8:8:8, 24-bit True Color and VGA Overlay
- Supports 8:8:8 24-bit True-Color Format
- Supports 5:6:5 XGA True-Color Format
- Supports 5:5:5 TARGA True-Color Format
- 32 x 32 x 2 User-Definable Hardware Cursor
- Bt471/475/476/477/478 Pin Compatible
- Power-On-Reset for Internal Registers
- Power-Down Mode
- Antisparkle Circuitry
- Analog Output Comparators
- Triple 6-bit (8-bit) D/A Converters
- 256 x 18 (24) Color Palette RAM
- 3 x 18 (24) Cursor Color Palette
- 15 x 18 (24) Overlay Registers
- Optional Internal Voltage Reference
- Programmable Pedestal
- Sync on all Three Channels
- Standard MPU Interface
- 44-pin PLCC Package

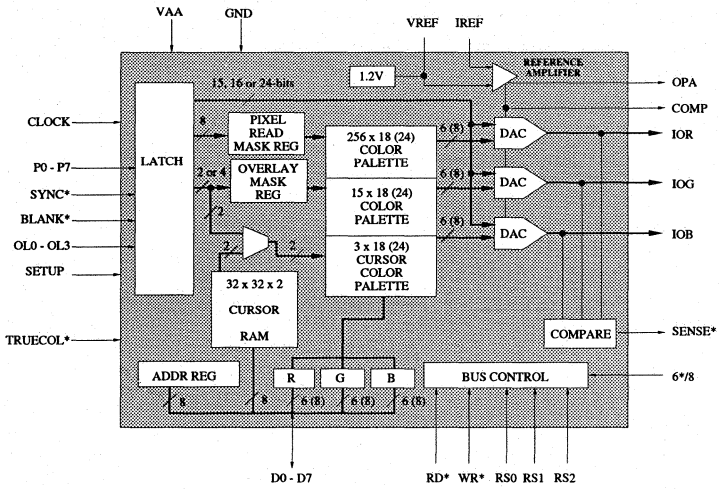
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Laptop Computers

Related Products

- Bt471
- Bt475
- Bt476
- Bt477
- Bt478

Functional Block Diagram



Bt481

Bt482

256-Word Color Palette 15-, 16-, and 24-bit True Color Power-Down RAMDACs™

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Product Description

The Bt481 and Bt482 RAMDACs are designed specifically for high-performance color graphics.

Both the Bt481 and Bt482 support three true-color modes: 15-bit (5:5:5, 32K colors) TARGA format, 16-bit (5:6:5, 65K colors) XGA format, and 24-bit (8:8:8, 16.8M colors) true-color format. They also support 8-bit pseudo-color format (256 colors).

The Bt482 has a 256 x 18(24) lookup table RAM, 15x18(24) overlay registers, 32 x 32 x 2 user-definable cursor, 4 x 24 cursor color palette and triple 8-bit D/A converters. Both 6-bit and 8-bit color modes are supported. The Bt481 is identical to the Bt482, but the Bt481 has no 32 x 32 x 2 cursor RAM. Both devices can support an external cursor. External cursor data is routed through the 3 x 24 cursor color palette to provide three modes for color selection. Mode 1 is a three-color cursor, Mode 2 is referred to as PM/Window or XGA cursor, and Mode 3 is referred to as an X-Windows cursor.

A power-down mode is available on both the Bt481 and the Bt482 to reduce power requirements when the analog outputs are not used. This is useful in laptop computer systems that require the option to drive an external RGB monitor.

Both the Bt481 and the Bt482 have on-chip analog output comparators to simplify diagnostics and debugging, with the result output onto the SENSE* pin. Also included

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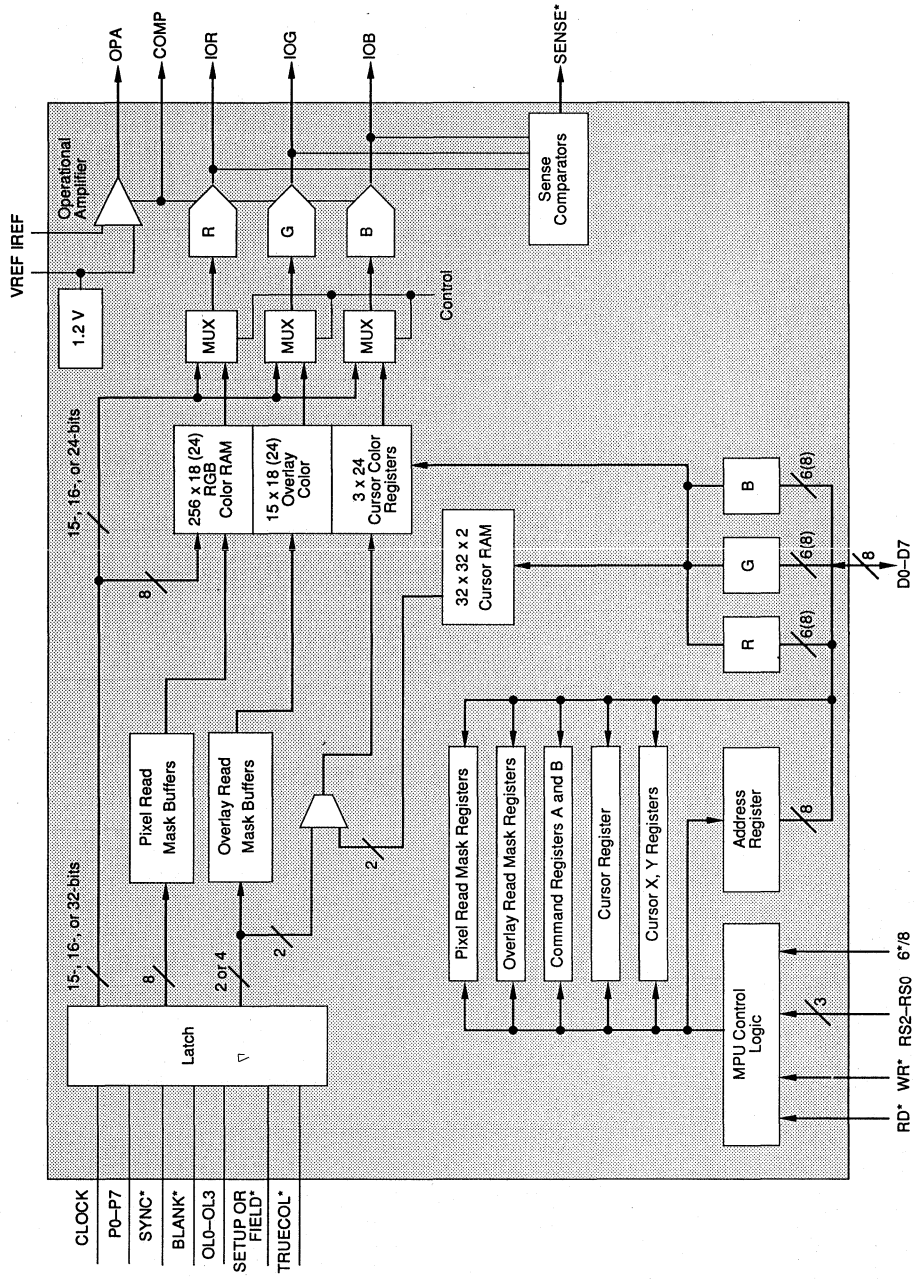
Product Description *(continued)*

is an on-chip voltage reference to simplify use of the device.

On power-up, the Bt481 and Bt482 behave as the Bt471 or Bt478, including their antisparkle capabilities, on-chip voltage reference, and analog output comparators. A power-on reset is available on the Bt481/482 devices to initialize internal registers.

The Bt481 and Bt482 generate RS-343-compatible video signals into a doubly-terminated 75 Ω load.



Detailed Block Diagram.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt481 and Bt482 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register addresses the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Overlay and Cursor Color Data

To write overlay or cursor color data, the MPU writes the address register (overlay write mode) with the address of the overlay or cursor color location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay or cursor color registers. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the overlay or cursor color location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written. In order to write the cursor color registers, bit CR3 in the cursor register must be a logical zero (see Table 2).

Reading Overlay and Cursor Color Data

To read overlay or cursor color data, the MPU loads the address register (overlay read mode) with the address of the overlay or cursor color location to be read. The contents of the overlay or cursor color register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay or cursor color location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay or cursor color registers. Following the blue read cycle, the contents of the overlay or cursor color location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read. In order to read the cursor color registers, bit CR3 in the cursor register must be a logical zero (see Table 2).

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (palette & cursor RAM write mode)
0	1	1	address register (palette & cursor RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay & cursor color write mode)
1	1	1	address register (overlay & cursor color read mode)
1	0	1	overlay registers
1	1	0	command register A

Table 1. Control Input Truth Table.

Circuit Description *(continued)*

	Value	RS2	RS1	RS0	CR3	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10					red value green value blue value
ADDR0–7 (counts binary)	$00–$FF 0000 0000 0000 0001 : 0000 1111 0001 0000 0001 0001 0001 0010 0001 0011 $00–$FF	0 1 1 : 1 1 1 1 1 1	0 0 0 : 0 0 0 0 0 0	1 1 1 : 1 1 1 1 1 1	x x x : x 0 0 0 0 1	color palette RAM reserved overlay color 1 : overlay color 15 reserved cursor color register 1 cursor color register 2 cursor color register 3 cursor RAM

Table 2. Address Register (ADDR) Operation.

15-, 16-, and 24/32-Bits-per-Pixel Operation

When the 15-, 16-, or 24/32-bit per pixel modes are activated (see Command Register A in the Internal Registers section), the inputs accept 16, 24, or 32 bits of pixel information from the 8-pin pixel port P0–P7. The 8-bit inputs form a 16- or 24-bit pixel (B15–0/B23–B0) to directly drive the 8-bit triple video DACs. The color lookup table and the read mask register are bypassed. Internally, the unused LSBs of all DACs are forced to zero in 15- or 16-bits-per-pixel modes. The 16- and 24-bit word (B15–0/B23–B0) is assigned to the DACs in the following format:

8:8:8:8 True-Color Format	5:6:5 XGA Format	5:5:5 TARGA Format	Comments
		B15	Ignored
B7 – B0	B15 – B11	B14 – B10	Red DAC
B15 – B8	B10 – B5	B9 – B5	Green DAC
B23 – B16	B4 – B0	B4 – B0	Blue DAC
B31 – B24			Palette or Masked

15-, 16-, and 24-Bits-per-Pixel Dual-Edge Clock

In the 15- and 16-bit-per-pixel dual-edge clock mode (see the command register bits A7–A4 description in the Internal Registers section), the least significant byte is latched on the rising edge of the pixel clock when BLANK* high is latched. Also in this mode, the most significant byte is latched on the falling edge of the pixel clock when BLANK* high is latched. Therefore, only one input clock period is required to load a 16-bit pixel.

In the 32-bit-per-pixel dual-edge clock mode, 32 bits of data, 24 bits of true color and 8 bits of palette index are latched on two rising and two falling edges. Therefore, only two input clock cycles are required to load a 32-bit pixel. If palette indexing is not required, logical zeros can be written for the palette overlay data, as *location zero in the palette RAM cannot be accessed in this mode.* Or palette overlay data can be masked out through the pixel read mask register. If the palette index data is not a logical zero or masked, the data will address any one of 255 locations in the palette RAM. Palette data has priority over bypass data.

15-, 16-, and 24-Bits-per-Pixel Single-Edge Clock

In the 15- and 16-bit-per-pixel single-edge clock mode (see Command Register A in the Internal Registers section), the inputs accept 16 bits of information by using two input clock cycles. The least significant byte is latched on the first rising edge of the input clock, and the most significant byte is latched on the second rising edge of the input clock. The bytes are synchronized with the BLANK* signal. The first byte latched after BLANK* goes high is the least significant byte. Since a pixel is latched in two clock cycles, the input clock must be twice as fast as the internal pipeline clock. The Bt481 and Bt482 each have an internal divider to generate the pipeline clock from the input clock.

In the 24-bit-per-pixel single-edge clock mode, the inputs accept 24 bits of pixel data by using three input clock cycles. The red byte is latched on the first rising edge of the pixel clock when BLANK* high is latched. The next two clock cycles latch the green and blue bytes. Since a 24-bit pixel is

latched in three input clock cycles, the input clock must be three times as fast as the internal pipeline clock. The Bt481 and Bt482 each have an internal divider to generate the pipeline clock from the pixel input clock. Palette data has priority over bypass data.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While the MPU is accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic. Data transfers take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU. These bits are used to address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode. *The pixel clock must be active for MPU accesses to the color palette RAM.*

Accessing Cursor Control Registers and Control Register B

A cursor register, CR; four cursor position registers; and a second control register, B, were defined to control the cursor, setup select, 6- or 8-bit select, and the sleep modes of the Bt481/482. Since there are only three register select lines (and all eight combinations have already been used), the cursor register; cursor X,Y registers; and Command Register B must be accessed indirectly.

For example, the cursor register is accessed with the following sequence of operations:

1. Set RS2 – RS0 = 110 in Command Register A.
2. Write a logical one to command register bit A0.
3. Set RS2 – RS0 = 000 in address register write mode.
4. Write address register to 0000 0011.
5. Set RS2 – RS0 = 010 in read mask register.
6. Read or write cursor register.

Table 3 contains specifications to indirectly address other registers.

Accessing Command Registers without the RS2 line

When the cursor or overlay functionality of the Bt481/482 is not used and the Register Select Line 2 (RS2) must be tied low at all times, the command registers of the Bt481/482 can still be accessed.

A flag will be set when the pixel read mask register (RS1 = 1 and RS0 = 0) is read four times consecutively. The next write to the pixel read mask register will be directed to Command Register A and can be used to set the bits in that register. Any access of the command register thereafter will also require four consecutive reads to the pixel read mask register. A write to any address or a read to any address other than the pixel read mask register will reset the flag.

When the extended registers are accessed (Bit A0 = 1), this feature is disabled.

4

Accessing the Cursor RAM Array (Bt482 only)

The 32 x 32 x 2 cursor RAM is accessed in a planar format. In the planar format only 7 address bits are used. The eighth bit determines which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 7.

After each access in the planar format, the address increments. The MPU uses ADDR, a binary address counter, to access the cursor RAM array (see Table 2). ADDR is the same binary counter used for RGB autoincrementing. Any write to ADDR after cursor autoincrementing has been initiated resets the cursor autoincrementing logic until cursor RAM array has again been accessed. Cursor autoincrementing will then begin from the address written. A read from the ADDR does not reset the cursor autoincrementing logic. To access the 32 x 32 x 2 cursor RAM, a logical one must be written to bit CR3 in the cursor register. The cursor register must be indirectly accessed.

Cursor Operation (Bt482 only)

The Bt482 has an on-chip, three-color, 32 x 32 x 2 pixel user-definable cursor. This cursor works with both interlaced and noninterlaced systems.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor position register (Xp,Yp) (see Figure 1). A (0,0) written to the cursor position registers will place the cursor completely offscreen. A (1,1) written to the cursor position registers will place the lower right pixel of the cursor on the upper left corner of the screen. Only one cursor pattern per frame is displayed at the location specified for both interlaced and noninterlaced display formats, regardless of the number of updates to (Xp,Yp). The cursor's vertical or horizontal location is not affected during any frame displayed. There are no restrictions on updating (Xp,Yp) other than both cursor position registers must be written when the cursor location is updated. Internal x and y position regis-

Circuit Description *(continued)*

	Value	RS2	RS1	RS0	Bit A0	Registers
ADDR 0–7 (counts binary)	0000 0000	0	1	0	1	Read Mask Register
	0000 0001	0	1	0	1	Overlay Mask Register
	0000 0010	0	1	0	1	Command Register B
	0000 0011	0	1	0	1	Cursor Register
	0000 0100	0	1	0	1	Cursor X Low Register
	0000 0101	0	1	0	1	Cursor X High Register
	0000 0110	0	1	0	1	Cursor Y Low Register
	0000 0111	0	1	0	1	Cursor Y High Register

Table 3. Indirect Register Addressing Truth Table.

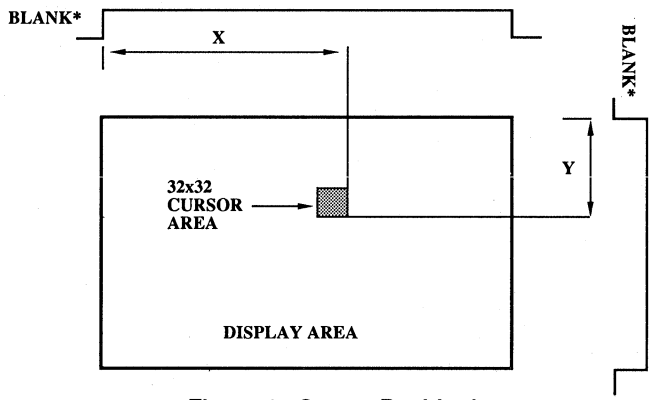


Figure 1. Cursor Positioning.

ters are loaded after the upper byte of Yp has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written. Cursor positioning is relative to BLANK* (see Figure 1). The reference point of the cursor, row 0, column 0, is in the lower right corner. The cursor Xp position is relative to the first rising edge of pixel clock when BLANK* is sampled at logical one. The cursor Yp position is relative to the first rising edge of pixel clock when BLANK* is sampled at logical one after the vertical blanking interval has been determined. If a BLANK* transition from logical zero to logical one does not occur within 2048 pixel clocks, vertical blanking has been asserted.

The cursor pattern can be displayed in an interlaced system if bit CR4 in the cursor register is a logical one. When bit CR4 in the cursor register has been set to logical one, the SETUP pin will become the FLD* pin. The SETUP can then be controlled only through bit B5 in Command Register B (see the Pin Description and Cursor Register sections). If Yp is greater than 32 ($0020) and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the FLD* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field, and the data in row 31 of the cursor RAM will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 31 of the cursor RAM will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to

Circuit Description *(continued)*

every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line, at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 32 ($0020), cursor display does not depend on whether Yp is odd or even. If the FLD* pin is a logical zero, the first line of the cursor is displayed on scan line one. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field, will correspond to subsequent scan lines in the even field. If the FLD* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line two. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

If bit CR4 is a logical zero, the cursor must be displayed in a noninterlaced system. Scan lines displayed in a frame correspond to sequential cursor lines in the cursor RAM relative to the first active cursor line in the frame.

Figure 2 is a visual explanation of planar pixel format and cursor RAM array pixel mapping.

External Cursor Support

The Bt481 does not have an onboard cursor RAM but can support an external cursor. The external cursor data can be input via the two MSB overlay pins (OL3 and OL2). When external cursor data is accepted, only the first four locations of the overlay palette can be addressed, since the MSB bits become cursor inputs. When a Bt481 is used, bits CR5, CR4, and CR3 in the cursor register are set to logical 1, 0, and 0, respectively. All cursor X,Y registers are no longer valid. The Bt481, like the Bt482, has a 4 x 24 cursor color register to support three cursor modes (see Cursor Color Support and Table 4). When a Bt482 is used, only one type of cursor can be used, either internal or external, at any given time. Bit CR5 in the cursor register controls cursor type.

Cursor Color Support

The cursor has three modes for color selection. Bits CR0 and CR1 in the cursor register determine which cursor mode is to be used. Mode 1 is a three-color cursor, Mode 2 is referred to as a PM/Window cursor, and Mode 3 is referred to as an X-Windows cursor (see Table 4).

Highlight Logic

The highlight logic is enabled in Cursor Mode 2 when cursor index data (plane 1 and plane 0) is logical one (see Table 5). When the highlight logic is enabled, the pixel highlighted will have a unique color because the highlight logic bit-wise complements the 24/18-bit palette or bypass data supplied to the DACs.

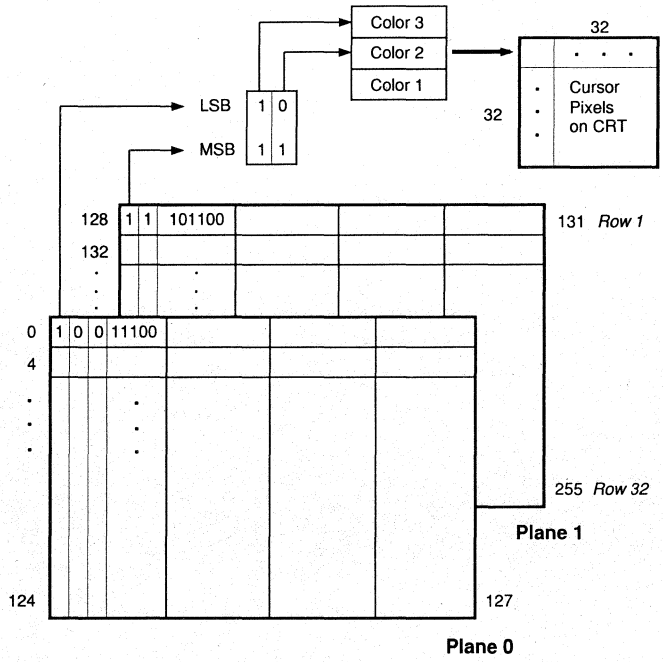


Figure 2. Planar Cursor Pixel Format and Mapping.

Circuit Description *(continued)*

Cursor Interlaced/Noninterlaced Display Operation

For the cursor display, the output sequence is dependent on the CR4 command bit and the FLD* input, e.g., when either interlaced or noninterlaced operation is selected, the current field is displayed.

Scan line 1 is always displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 2 immediately follows scan line 1. In the interlaced mode, scan line 2 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed and the FLD* pin has been toggled.

Only the ODD lines or only the EVEN lines will be displayed, if the FLD* does not change.

Figure 3 shows the interlaced and noninterlaced display scan. Noninterlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

Plane 1	Plane 0	MODE 1	MODE 2	MODE 3
0	0	Palette/OL Data	Cursor Color 1	Palette/OL Data
0	1	Cursor Color 1	Cursor Color 2	Palette/OL Data
1	0	Cursor Color 2	Palette/OL Data	Cursor Color 1
1	1	Cursor Color 3	Palette/OL Data Complement	Cursor Color 2

Table 4. Cursor Color Modes. (Planes 1 and 0 refer to the Internal Cursor RAM.)

Cursor Mode	CR5	OL3–OL0	P0–P7	Addressed by Pixel Port
	1	0000	$xx	palette data/bypass
	1	0001	$xx	overlay color 1
	1	0010	$xx	overlay color 2
	1	0011	$xx	overlay color 3
Mode 1	1	00xx	$xx	palette/OL data
Mode 1	1	01xx	$xx	cursor color register 1
Mode 1	1	10xx	$xx	cursor color register 2
Mode 1	1	11xx	$xx	cursor color register 3
Mode 2	1	00xx	$xx	cursor color register 1
Mode 2	1	01xx	$xx	cursor color register 2
Mode 2	1	10xx	$xx	palette/OL data
Mode 2	1	11xx	$xx	palette/OL data complement
Mode 3	1	00xx	$xx	palette/OL data
Mode 3	1	01xx	$xx	palette/OL data
Mode 3	1	10xx	$xx	cursor color register 1
Mode 3	1	11xx	$xx	cursor color register 2

The cursor data has priority over the overlay data. OL3 and OL2 are used for external cursor support.

Table 5. External Cursor Color and Overlay Control Truth Table (Pixel/OL Read Mask Register = $FF).

Circuit Description *(continued)*

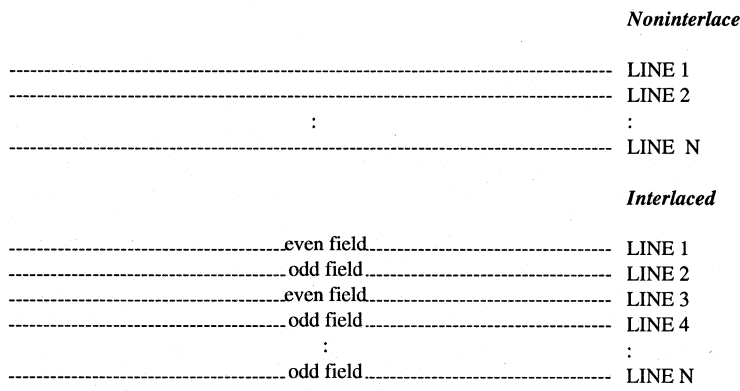


Figure 3. Interlaced / Noninterlaced Display Operation.

6-Bit/8-Bit Color Selection

The command register bit B1 or the 6*/8 pin can be used to specify whether the MPU is reading and writing 6 bits or 8 bits of color information each cycle. The 6*/8 bit (bit B1 in Command Register B) and the 6*/8 pin (pin #2) are logically ANDed. If the 6*/8 bit is a logical one, the 6*/8 pin controls 6- or 8-bit operation. While the 6*/8 bit remains at logical zero, the MPU will read and write 6 bits of color information each cycle. For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus; D0 is the LSB, and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Accessing the cursor RAM array does not depend on the resolution of the DACs. If the 6*/8 pin is held low (6-bit operation), the Bt481/482 will emulate a Bt471.

In the 6-bit mode, the Bt481/482's full-scale output current will be about 1.5 percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are always a logical zero when in the 6-bit mode.

Power-Down Mode

The Bt481 and Bt482 incorporate a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt481/482 functions normally.

While the SLEEP bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may still be read or written to while the SLEEP bit is a logical one if the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is complete. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn off the current reference (IREF = 0 mA) during sleep mode.

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level of the SENSE comparator circuit. This output is used to determine the presence of a CRT monitor and, with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For proper operation of the SENSE circuit, the following levels should be applied to the comparator with the IOR, IOG, and IOB outputs:

DAC Low Voltage ≤ 310 mV (see Note)
DAC High Voltage ≥ 430 mV (see Note)

There is an additional ±10 percent tolerance on the above levels when the internal voltage reference or an external current reference is used. SYNC* should be a logical zero for SENSE* to be stable.

Note: SENSE values are subject to change upon completion of characterization.

Circuit Description *(continued)*

Controller Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 6. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask register are bit-wise logically ANDed with the OL0–OL3 inputs. Bit D0 of the overlay read mask register corresponds to overlay input OL0, and bit D3 of the overlay read mask register corresponds to overlay input OL3. Bits D4–D7 of the overlay read mask register are ignored. Two consecutive write operations must be performed to write to the overlay read mask register. The first write is to the overlay read mask, and the second is to the pixel read mask. All 12 bits will be updated concurrently, synchronous to the pixel clock. Command Register B in the Internal Register section contains information regarding the accessability of the overlay read mask register. The addressed locations provide 18 bits or 24 bits of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 4–6. Tables 7–9 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input pin is logically ORed with the SETUP command bit and is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. If bit CR4 in the cursor register is set to logical one, the SETUP pin will become the field input (see Cursor Register in the Internal Register section) in order to support an interlaced cursor. The blanking pedestal can then be controlled only with the SETUP command bit (see Command Register B in the Internal Register section).

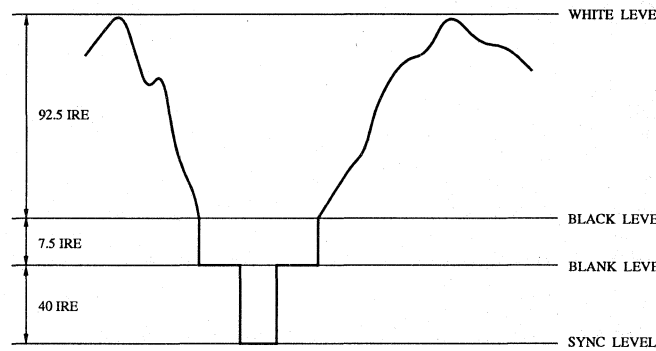
The analog outputs of the Bt482 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

CR5	OL0–OL3	P0–P7	Addressed by Pixel Port
0	$0	$00	color palette RAM location $00
0	$0	$01	color palette RAM location $01
:	:	:	:
0	$0	$FF	color palette RAM location $FF
0	$1	$xx	overlay color 1
:	:	$xx	:
0	$F	$xx	overlay color 15

Table 6. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load; SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 4. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

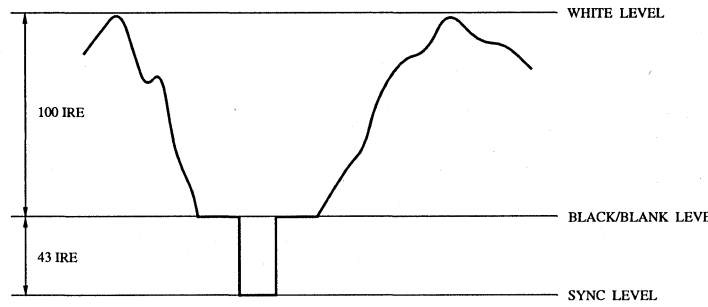
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load; SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 143 Ω.

Table 7. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load; SETUP = 0 IRE. VREF = 1.235V and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 5. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE).

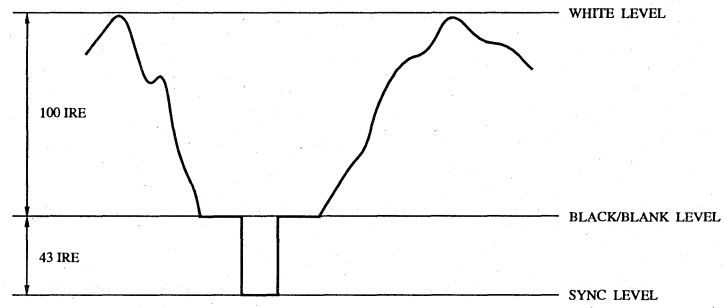
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 143 Ω.

Table 8. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50 Ω load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 176 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 6. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 176 Ω.

Table 9. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Command Register A

This register may be written to or read by the MPU at any time. All bits are initialized to logical zero on power-up.

A7	A6	A5	A4	
0	x	x	x	Pseudo Color (256 Colors)
1	0	0	0	5:5:5 Dual-Edge Clock (33K Colors)
1	1	0	0	5:6:5 Dual-Edge Clock (65K Colors)
1	0	1	0	5:5:5 Single-Edge Clock (33K Colors)
1	1	1	0	5:6:5 Single-Edge Clock (65K Colors)
1	0	0	1	8:8:8:OL Dual-Edge Clock (16.8M Colors)
1	1	1	1	8:8:8 Single-Edge Clock Only (16.8M Colors)

A logical one on Bit A7 enables 15-, 16-, and 24/32-bit modes when used with Bits A6, A5, and A4. If A7 is a logical zero, pseudo-color mode is enabled regardless of the state of A6, A5, or A4.

Bit A6 determines whether the device is in 15- or 16-bit-per-pixel mode.

Bit A5 determines whether the data is input on the rising edge of the input clock, or on the rising and falling edges of the input clock. A logical zero written to this bit indicates a dual-edge clock, and a logical one indicates a single-edge clock.

Bit A4 indicates a 24- or 32-bit input, i.e., a 24-bit true-color bypass, only, or a 24-bit true-color bypass and an 8-bit VGA passthrough. Bit A5 determines whether the pixels are input 8 bits at a time on every rising edge, or 8 bits at a time on rising and falling edges of the input clock. When bits A4 and A6 are set to logical one, the inputs are 24-bit true-color bypass, operating in single-edge clock mode.

A3, A2, A1 Reserved (logical zero)

A logical zero must be written to these bits to ensure proper operation.

A0 Extended Register Select

(0) Extended register set cannot be accessed.
(1) Extended register set can be accessed.

A logical one written to this bit allows the user to indirectly access the extended register set. Included in the extended register set are the cursor register and the cursor X,Y registers.

Internal Registers *(continued)*

Command Register B

This register is operational only while bit A0 in Command Register A is a logical one. This register is initialized on power-up. On power-up, bits B7, B6, B5, and B0 are set to logical zero; bits B4, B3, B2, and B1 are set to logical one to enable the Bt481/482 to emulate the Bt478. While the 6*/8 pin is held low, this register will be functionally ignored.

B7	Reserved (logical zero)	A logical zero must be written to this bit to ensure proper operation.
B6	Overlay Register Mask Select (0) Overlay register mask inhibited (1) Overlay register mask enabled	A logical *zero* written to this bit *inhibits* address of the overlay registers only during true-color operations. A logical *one* written to this bit *enables* address of the overlay registers only during true-color operations.
B5	SETUP select (0) 0 IRE (1) 7.5 IRE	This bit specifies the blanking pedestal to be either 0 or 7.5 IRE. When the interlaced mode is set (bit CR4 = 1), only this bit will be able to control the SETUP select; the SETUP pin will become the field input (ODD/EVEN). While the 6*/8 pin is held low, the SETUP pin will act as the pedestal control rather than the field input.
B4	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output contains sync information.
B3	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output contains sync information.
B2	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output contains sync information.
B1	6-bit/8-bit select (0) 6-bit (1) 8-bit	On the Bt481 and Bt482, this bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. The 6*/8 bit and 6*/8 pin are logically ANDed.
B0	SLEEP enable (0) normal operation (1) sleep mode	While this bit is a logical zero, the Bt482 functions normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data and may be read or written to while the pixel clock is running. The RAM automatically powers-up during MPU read/write cycles and shuts down when the MPU access is completed. About 1 second is required for the Bt482 to output valid video data after enabling normal operation (coming out of sleep mode). This time will vary depending on the size of the COMP capacitor. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn the current reference off during sleep mode.

Internal Registers *(continued)*

Cursor Register

This register is operational only when Bit A0 in Command Register A is a logical one. All bits are initialized to logical zero on power-up.

CR7, CR6	Reserved (logical zero)	A logical zero must be written to these bits to ensure proper operation.
CR5	Cursor Select (0) Internal Cursor Selected (1) External Cursor Mode/Overlay	This bit determines whether the internal cursor is used or external cursor data is input with the two MSB overlay pins of the Bt482 (OL3 and OL2). When the internal cursor is enabled, all 15 locations of the overlay palette can be selected. When an external cursor is enabled, only the first four locations of the overlay palette can be selected.
CR4	Display Mode Select (0) Noninterlaced (1) Interlaced	When this bit is a logical zero, the display format is noninterlaced. When it is a logical one, the display format is interlaced, and the odd/even fields are input with the SETUP pin. The mode must be set properly to ensure proper operation of the internal cursor.
CR3	Cursor RAM or Cursor Palette Select (0) Cursor Color Palette Selected (1) Cursor RAM Selected	A logical one written to this bit enables the user to access the 32 x 32 x 2 cursor RAM. A logical zero written to this bit enables the user to access the three cursor color palette locations.
CR2	Reserved (logical zero)	A logical zero must be written to this bit to ensure proper operation.
CR0, CR1	Cursor Mode Select (00) Cursor Disabled (01) 3-Color Cursor (10) 2-Color/Complement Cursor (11) 2-Color/X-Windows Cursor	These bits determine the functionality of the onboard 32 x 32 x 2 cursor.

Internal Registers *(continued)*

Cursor (x,y) Registers

These registers specify the (x,y) coordinate of the 32 x 32 x 2 hardware cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 32 (or $0020)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 ($0FFF) may be written into the cursor (x) register. If Xp is equal to zero, the cursor will be entirely offscreen (see Cursor Operation in the Circuit Description section).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 32 (or $0020)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to zero, the cursor will be entirely offscreen (see Cursor Operation in the Circuit Description section).

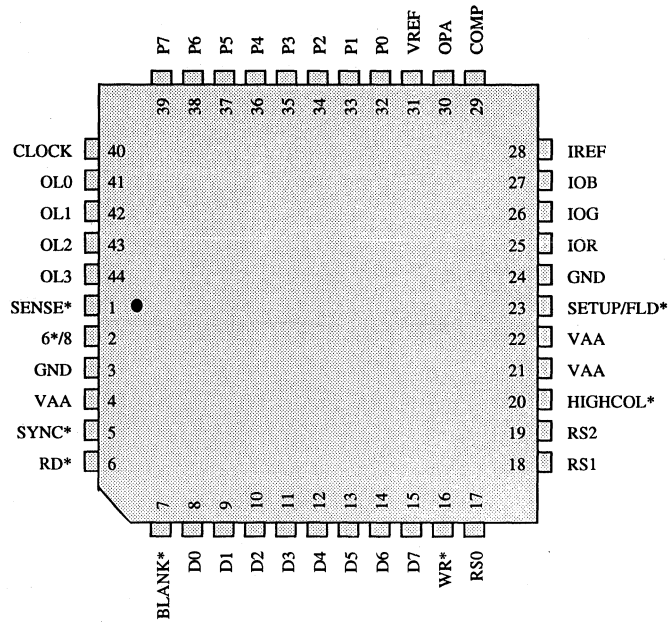
Pin Descriptions

Pin Name & Number		Description
BLANK*	(7)	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as specified in Tables 7–9. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP or FLD*	(23)	SETUP is setup control input (TTL compatible). This input is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. FLD* is odd/even field input (TTL Compatible). This signal should be changed only during vertical blanking. This input ensures proper operation of the onboard cursor when interlaced operation (command register bit CR4 = 1) is selected. When it is a logical zero, an even field is specified. When this input is a logical one, an odd field is specified. If CR4 = 1, SETUP can be controlled only through Bit B5 in Command Register B. This input becomes the SETUP control if noninterlaced operation is selected (CR4 = 0). This pin should not be left floating.
SYNC*	(5)	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 4–6). SYNC* does not override any other control or data input, as shown in Tables 7–9; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	(40)	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0–P7	(32–39)	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	(41–44)	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as specified in Table 6. When the overlay palette is accessed, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND. OL2 and OL3 are used for external cursor inputs when external cursor is selected.
COMP	(29)	Compensation pin. If an external or the internal voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. The PC Board Layout Considerations section contains critical layout criteria.
VREF	(31)	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.235 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor should decouple this input to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry other than the decoupling capacitor. The PC Board Layout Considerations section contains further information.
OPA	(30)	Reference amplifier output. If an external or the internal voltage reference is used, this pin must be connected to COMP. When an external current reference is used, this pin should be left floating. The PC Board Layout Considerations section contains further information.
IOR, IOG, IOB	(25–27)	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.
VAA	(4, 21, 22)	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

Pin Name & Number	Description
GND (3, 24)	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
IREF (28)	Full-scale adjust control. The IRE relationships in Figures 4–6 are maintained, regardless of the full-scale output current. When an external or the internal voltage reference is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA) K is defined in the table below. It is recommended that a 143 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 176 Ω RSET resistor is recommended. When an external current reference is used, the relationship between IREF and the full-scale output current on each output is: IREF (mA) = Iout (mA) / K **Mode / Pedestal / K (with sync) / K (no sync)** 6-bit / 7.5 IRE / 3.078 / 2.211 8-bit / 7.5 IRE / 3.102 / 2.230 6-bit / 0 IRE / 2.910 / 2.044 8-bit / 0 IRE / 2.934 / 2.063 See the PC Board Layout Considerations section for further information.
WR* (16)	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD* (6)	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2 (17–19)	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as detailed in Tables 1 and 2.
D0–D7 (8–15)	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
6*/8 (2)	6-bit/8-bit select input (TTL Compatible). This pin specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, MPU Bit D7 is the most significant bit during read/write cycles. For 6-bit operation, MPU Bit D5 is the most significant bit during read/write cycles. (D7 and D6 are ignored during write cycles and are logical zero during read cycles.)
SENSE* (1)	Sense output (CMOS compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level. SENSE* may not be stable while SYNC* is toggling.
TRUECOL* (20)	True-color mode select input (TTL compatible). This signal is inverted and logically ORed with Bit A7 in Command Register A. A logical zero will enable the true-color modes. By programming the proper command register bits, the user can choose either 5:5:5, 5:6:5, 8:8:8, or 8:8:8:OL and determine whether the pixels are input on a single clock edge or a dual clock edge (see the Command Register section for details). The TRUECOL* pin should be tied to VAA to disable the hardware selection of the true-color mode.

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt481/482, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16). This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt481/482 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt481/482 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt481/482 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 7–9. This bead should be located within 3 inches of the Bt481/482. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 7–9 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt481/482 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt481/482 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevinen equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt481/482 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt481/482 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt481/482 to minimize reflections. Unused analog outputs should be connected to GND.

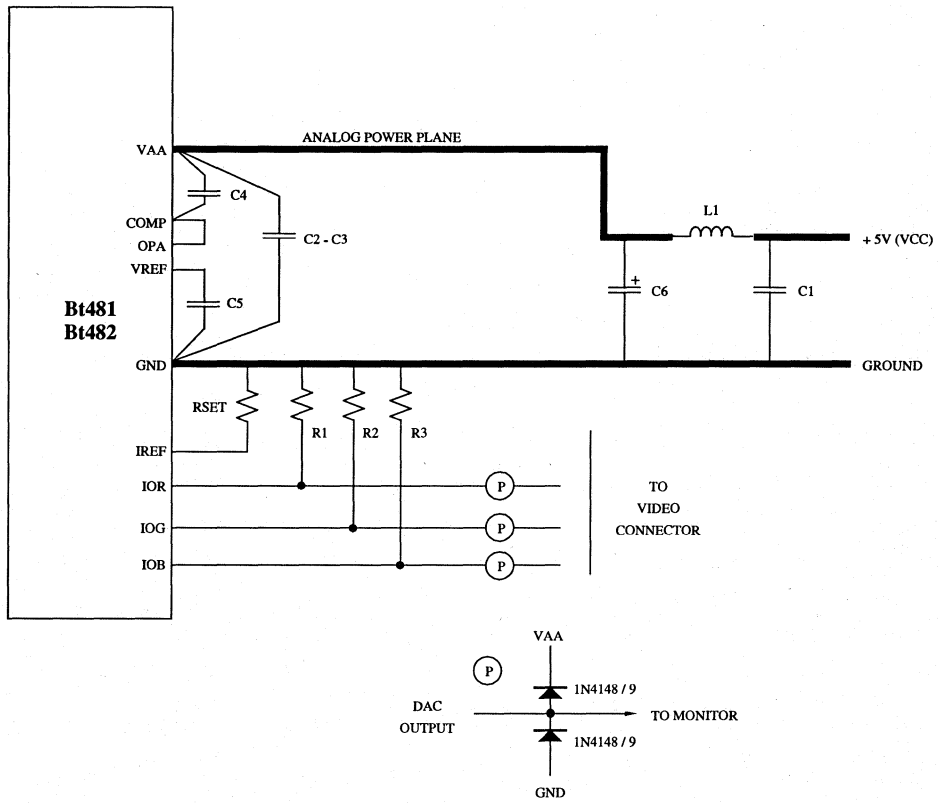
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt481/482 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 7–9 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



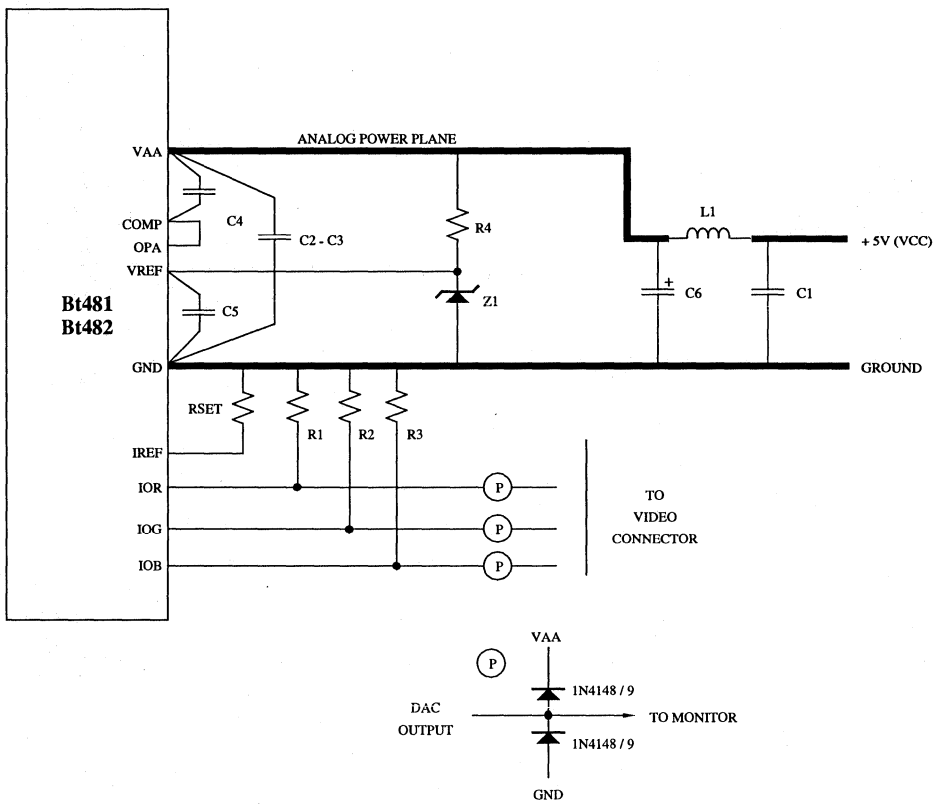
Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481/482.

Figure 7. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



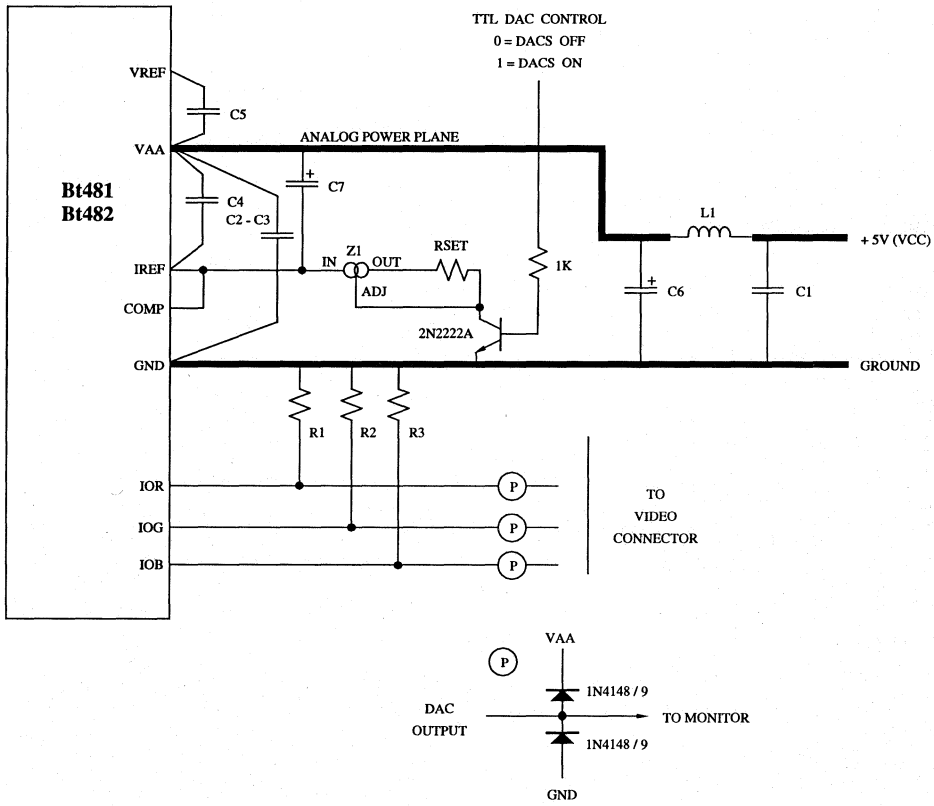
Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481/482.

Figure 8. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM317LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481/482.

Figure 9. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When multiple Bt482s are used, each Bt482 should have its own power plane ferrite bead. If the internal reference is used, each Bt482 should use its own internal reference.

Although the multiple Bt482s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt482 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about ten times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

When an external current reference is used, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 9, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
85 and 75 MHz Parts		4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt482 and Bt481		6	6	6	Bits
Bt482 and Bt481		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt482 and Bt481				±1	LSB
Differential Linearity Error	DL				
Bt482 and Bt481				±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		5		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT		5		pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Black					
(Note 1)		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size					
Bt482 and Bt481			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance	CAOUT		18		pF
(f = 1 MHz, IOUT = 0 mA)					
Internal Reference Output	VREF	TBD	TBD	TBD	V
Power Supply Rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" and external voltage reference with RSET = 143 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 6*/8 pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: When the Bt482 or Bt481 is in the 6-bit mode, the output levels are approximately 1.5 percent lower than these values.

Note 2: Guaranteed by characterization, not tested.

AC Characteristics

Parameter	Symbol	85 MHz Devices Min	85 MHz Devices Typ	85 MHz Devices Max	75 MHz Devices Min	75 MHz Devices Typ	75 MHz Devices Max	Units
Input Clk Rate Pseudo Color	Fmax			85			75	MHz
Input Clk Rate 15-, 16-bit dual-edge clk	Fmax			50			50	MHz
Input Clk Rate 15-, 16-bit single-edge clk	Fmax			85			85	MHz
Input Clk Rate 32-bit dual-edge clk	Fmax			50			50	MHz
Input Clk Rate 24-bit single-edge clk	Fmax			85			85	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	2			2			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	2			2			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time (Pseudo Color and 15-, 16-, and 24-bit Single-Edge Clock Mode)	12	3			3			ns
Pixel and Control Setup Time	20	–1			–1			ns
Pixel and Control Hold Time (15-, 16-, and 32-bit Dual-Edge Clock Mode, LSB and MSB)	21	7			7			ns
Clock Cycle Time (p13)	13	11.77			13.33			ns
Pseudo Color Mode								
Clock Pulse Width High Time (Note 1)	14	4			4			ns
Clock Pulse Width Low Time (Note 1)	15	4			4			ns
Single Edge True Color Modes								
Clock Pulse Width High Time (Note 1)	14	5			5			ns
Clock Pulse Width Low Time (Note 1)	15	5.5			5.5			ns
Clock Cycle Time (Dual-Edge Clock)	13	20			20			ns
Clock Pulse Width High Time	14	9			9			ns
Clock Pulse Width Low Time	15	9			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time (Note 2)	18		13			13		ns
Clock and Data Feedthrough (Note 2)			–30			–30		dB
Glitch Impulse (Note 2)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
VAA Supply Current (Note 3)	IAA							
normal operation				270			270	mA
sleep enabled (Note 4)			2			2		mA

AC Characteristics *(continued)*

Parameter	85 MHz Devices Min	85 MHz Devices Typ	85 MHz Devices Max	75 MHz Devices Min	75 MHz Devices Typ	75 MHz Devices Max	Units
Pipeline Delay							Clocks
Pseudo Color	7	7	7	7	7	7	
5:5:5 Dual-Edge Clock Mode	7	7	7	7	7	7	
5:6:5 Dual-Edge Clock Mode	7	7	7	7	7	7	
8:8:8:8 Dual-Edge Clock Mode	8	8	8	8	8	8	
5:5:5 Single-Edge Clock Mode	8	8	8	8	8	8	
5:6:5 Single-Edge Clock Mode	8	8	8	8	8	8	
8:8:8 Single-Edge Clock Mode	9	9	9	9	9	9	

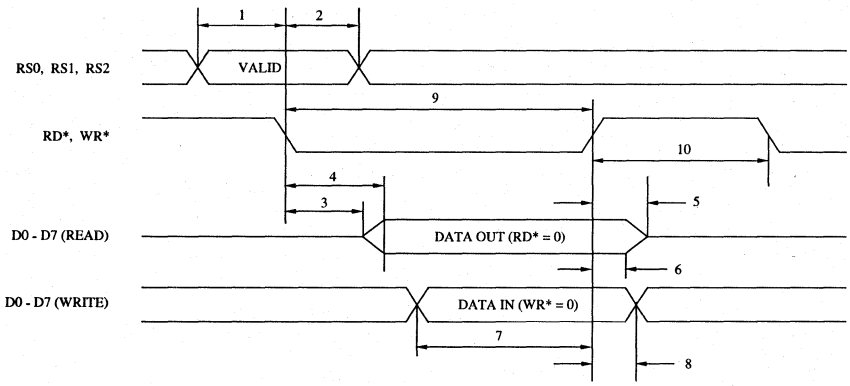
Test conditions (unless otherwise specified): "Recommended Operating Conditions" and external voltage reference with RSET = 143 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 6*/8 pin = logical one. TTL input values are 0–3 V with input rise/fall times ≤ 3 ns, measured between the 10-percent and 90-percent points. Timing reference points are at 50 percent for inputs and outputs unless otherwise noted. Analog output load ≤ 10 pF. SENSE*, D0–D7 output load ≤ 75 pF. See the timing notes on the following page. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: These pulse widths are specified at VIL = 0.8 V for clock pulse width low and VIH = 2.0 V for clock pulse width high.

Note 2: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2 x clock rate.

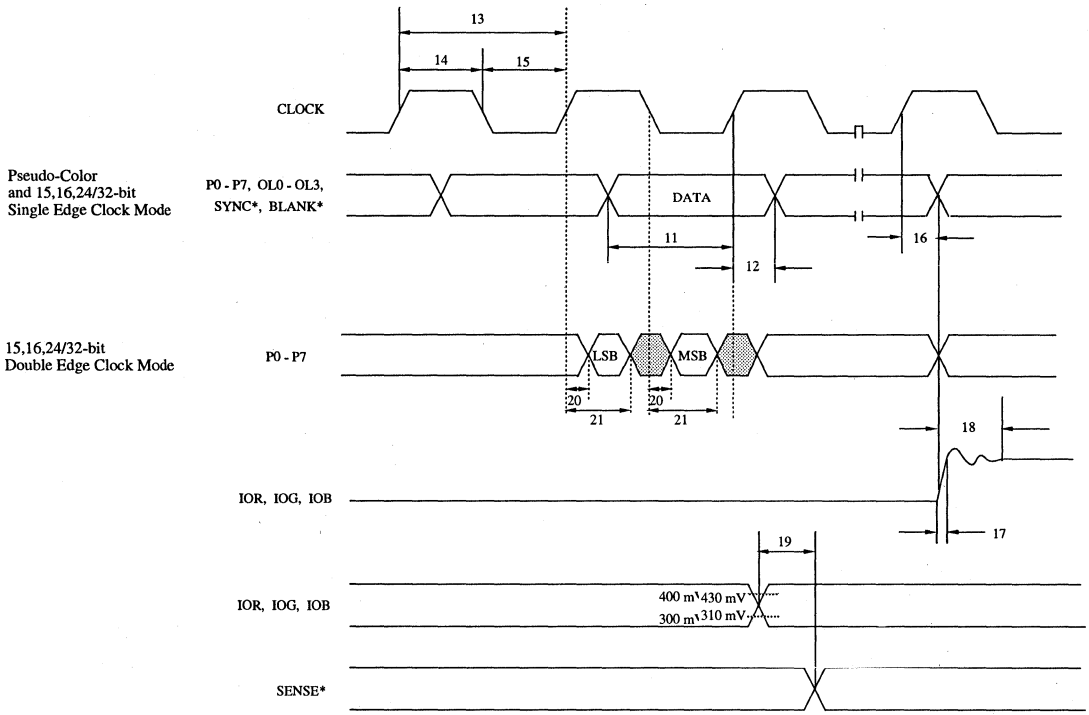
Note 3: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Note 4: External current or voltage reference disabled during sleep mode. Test Conditions: +25° to +70° C, pixel and data ports at 0.4 V.



MPU Read/Write Timing.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

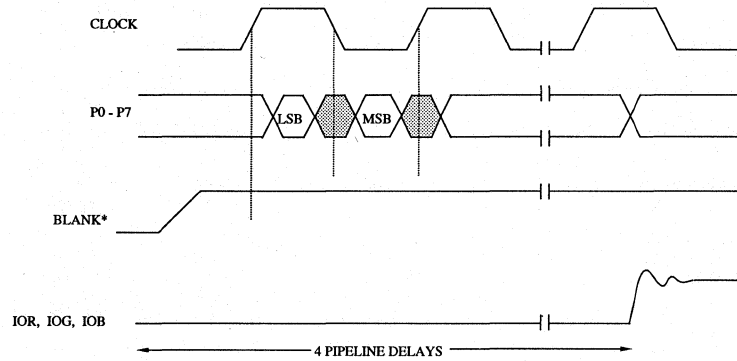
Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

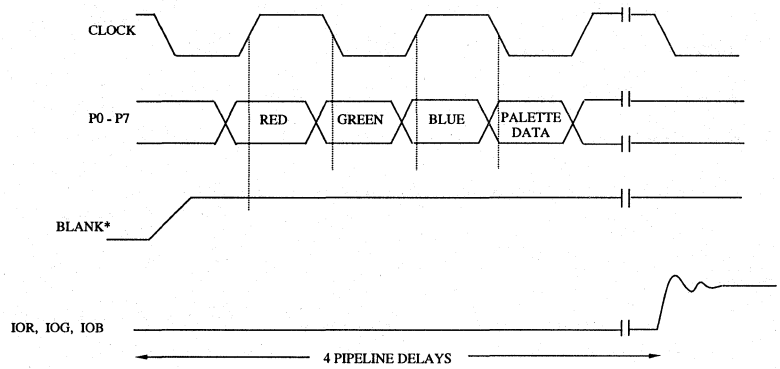
Video Input/Output Timing.

Timing Waveforms

15,16-bit
Dual Edge Clock Mode

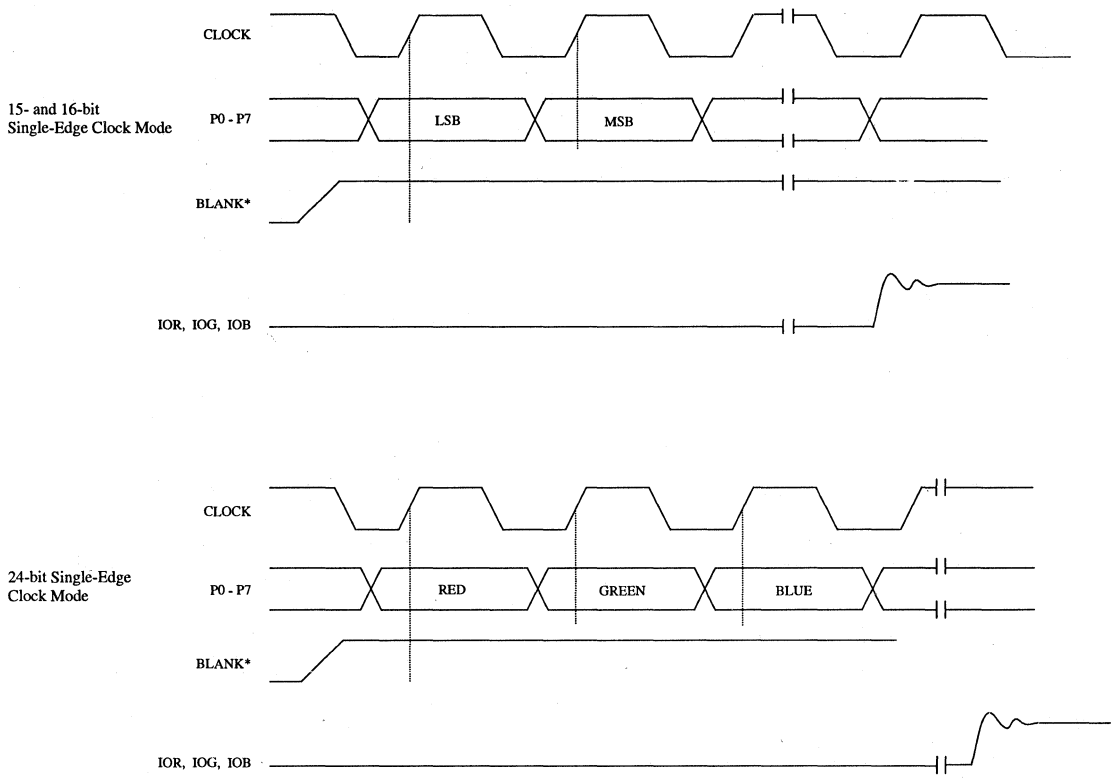


24/32-bit
Dual Edge Clock Mode



15-, 16-, and 32-bit-per-Pixel Timing, Dual-Edge Clock Mode.

Timing Waveforms



15-, 16-, and 24-bit-per-Pixel Timing, Single-Edge Clock Mode.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Speed	Package	Ambient Temperature Range
Bt481KPJ85	256 x 24	15 x 24	85 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt481KPJ75	256 x 24	15 x 24	75 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt482KPJ85	256 x 24	15 x 24	85 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt482KPJ75	256 x 24	15 x 24	75 MHz	44-pin Plastic J-Lead	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt484

85 MHz
Monolithic CMOS
True-Color
RAMDAC™

4

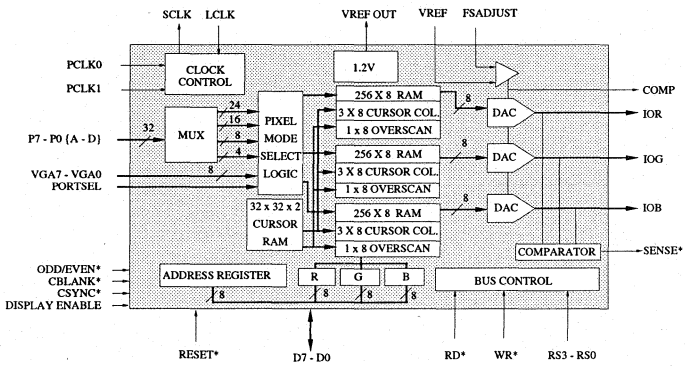
Distinguishing Features

- 85, 75 MHz Pipelined Operation
- 8:1, 4:1, 2:1, 1:1 Multiplexed Pixel Ports
- Separate 8-bit VGA Port
- 32 x 32 x 2 Programmable Cursor
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 3 x 8 Cursor Color Palette
- Optional Sync on All Three Channels
- 0 or 7.5 IRE Blanking Pedestal
- Voltage Reference
- Analog Output Comparators
- Antisparkle Circuitry
- Power-Down Mode
- 84-pin PLCC Package
- VRAM Shift Clock
- VGA Support in a True-Color Window

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt484 RAMDAC is designed specifically for high-performance color graphics.

Included are four byte-wide pixel input ports (multiplexed 4:1), three 256 x 8 color lookup tables with triple 8-bit video D/A converters (configurable for either 6-bit or 8-bit D/A converter operation), and a programmable 32 x 32 x 2 cursor with its own color palette.

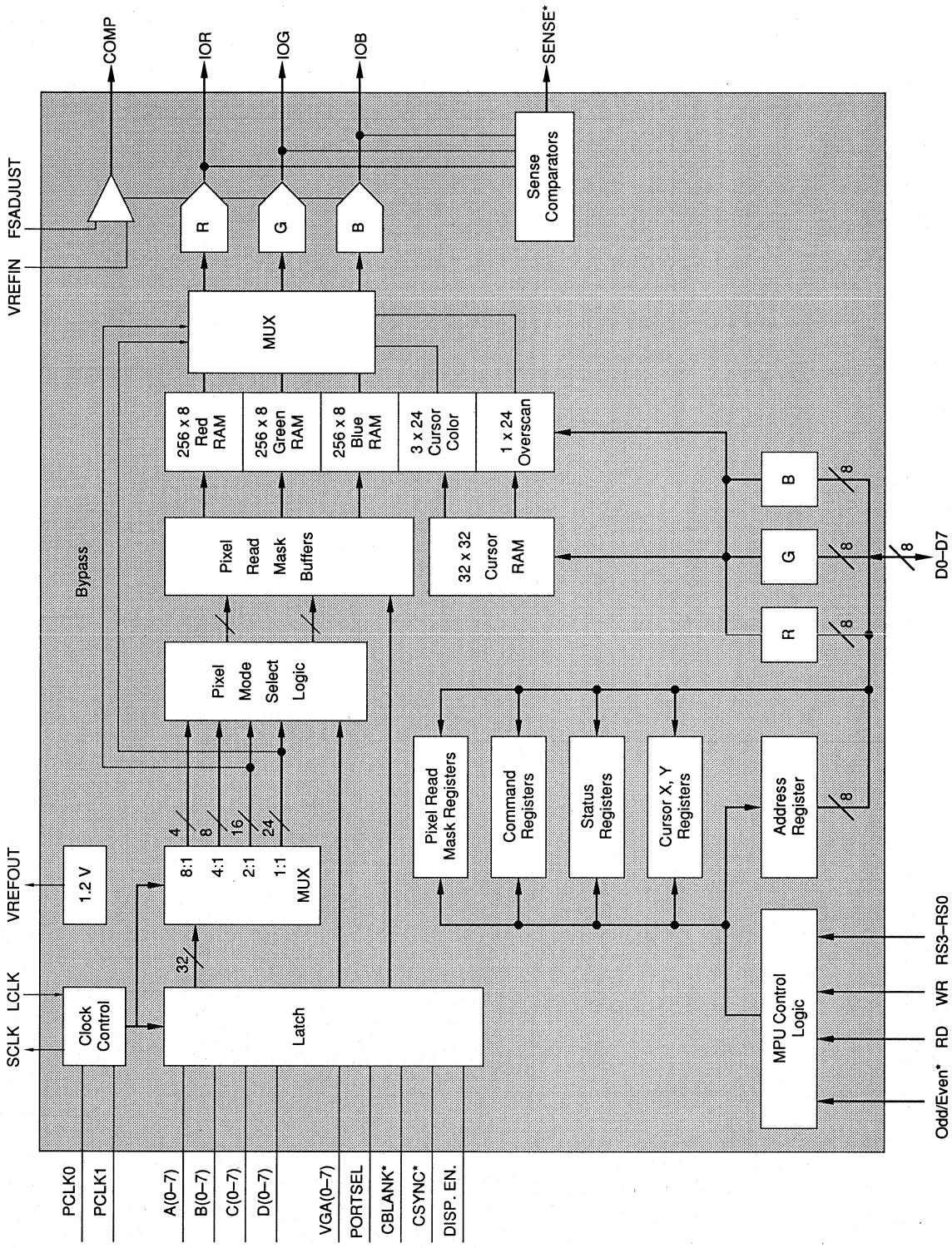
The Bt484 may alternately be configured for a lower performance VGA mode, where 8 bits of VGA pixel data (from a VGA controller) are input through a separate VGA pixel port.

Several operational modes are supported by the 32 pins allocated for the P7:P0 port, including 8-bit pseudo color, 16- and 24-bit true color, and various packed and sparse pixel formats. The color palette may be bypassed in any of the operational modes, except VGA.

The Bt484 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load.

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L484001 Rev. D

Brooktree®



Bt484 Detailed Block Diagram.

Circuit Description

MPU Interface

As illustrated in the detailed block diagram, a standard MPU bus interface is supported, giving the MPU direct access to the color palette RAM. MPU data is transferred into and out of the RAMDAC with the D0–D7 data pins. The read/write timing is controlled by the RD* and WR* inputs.

The RS0–RS3 select inputs specify which control register the MPU is accessing, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers. D0 corresponds to ADDR0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written. The Timing Waveforms section contains further information.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Cursor and Overscan Color Data

To write cursor color data, the MPU writes the address register (cursor color write mode) with the address of the cursor color location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the cursor color registers. After the blue write cycle, the three bytes of red, green, and blue color information are concatenated into a 24-bit word and written to the cursor color location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Cursor Color Data

To read cursor color data, the MPU loads the address register (cursor color read mode) with the address of the cursor color location to be read. The contents of the cursor color register at the specified address are copied into the RGB registers, and the address register is incremented to the next cursor color location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to

RS3–RS0	Access	Addressed by MPU
0000	R/W	address register; palette/cursor RAM write
0001	R/W	6/8-bit color palette data
0010	R/W	pixel mask register
0011	R/W	address register; palette/cursor RAM read
0100	R/W	address register; cursor/overscan color write
0101	R/W	cursor overscan and color data
0110	R/W	command register 0
0111	R/W	address register; cursor/overscan color read
1000	R/W	command register 1
1001	R/W	command register 2
1010	read only	status register
1011	R/W	cursor RAM array data
1100	R/W	cursor x-low register
1101	R/W	cursor x-high register
1110	R/W	cursor y-low register
1111	R/W	cursor y-high register

Table 1. Control Input Truth Table (RS3 = MSB and RS0 = LSB).

ADDR 0–7 (counts binary)	ADDRa,b (counts modulo 3)	RS3	RS2	RS1	RS0	Addressed by MPU
$00–$FF	00	0	0	0	1	color palette RAM (red component)
	01	0	0	0	1	color palette RAM (green component)
	10	0	0	0	1	color palette RAM (blue component)
xxxx xx00	00	0	1	0	1	overscan color (red component)
	01	0	1	0	1	overscan color (green component)
	10	0	1	0	1	overscan color (blue component)
xxxx xx01	00	0	1	0	1	cursor color 1 red component
	01	0	1	0	1	cursor color 1 green component
	10	0	1	0	1	cursor color 1 blue component
xxxx xx10	00	0	1	0	1	cursor color 2 red component
	01	0	1	0	1	cursor color 2 green component
	10	0	1	0	1	cursor color 2 blue component
xxxx xx11	00	0	1	0	1	cursor color 3 red component
	01	0	1	0	1	cursor color 3 green component
	10	0	1	0	1	cursor color 3 blue component
$00–$7F	N/A	1	0	1	1	cursor RAM array, plane 0
$80–$FF	N/A	1	0	1	1	cursor RAM array, plane 1

When addressing the cursor color register or overscan register, the 6 MSBs of the address register are don't-care conditions. Therefore, when the address register is read and the previous access was to the cursor color registers or overscan register, address register bits [7–2] are returned as either ones or zeros.

Table 2. Address Register Operation and Auto Incrementing.

select the cursor color registers. Following the blue read cycle, the contents of the cursor color location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB registers and lookup table RAMs occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Circuit Description *(continued)*

Accessing the Cursor RAM Array

The 32 x 32 x 2 cursor RAM is accessed in a planar format. In the planar format only 7 address bits are used. The eighth bit determines which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 7.

After each access in the planar format, the address increments. The MPU uses ADDR, a binary address counter, to access the cursor RAM array (see Table 2). ADDR is the same binary counter used for RGB auto-incrementing. Any write to ADDR after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the ADDR does not reset the cursor, auto-incrementing logic. The color palette RAM and the cursor RAM share the same external address register, and MPU addressing for this and all other registers is determined by the external register select lines RS3–RS0 (see Table 1).

6-Bit / 8-Bit Operation

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus with D0 the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are a logical zero.

Accessing the cursor RAM array does not depend on the resolution of the DACs.

In the 6-bit mode, the Bt484's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Power-Down Mode

The Bt484 incorporates a power-down capability controlled by command bit CR00. While command bit CR00 is a logical zero, the Bt484 functions normally.

While command bit CR00 is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the MPU may read or write to the RAM while the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. The DACs output no current, and the three command registers may still be written to or read by the MPU. The output DACs require about 1 second to turn off (sleep mode) or turn on (normal), depending on the compensation capacitor used (see Video Generation for further information).

When using an external voltage reference, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

Circuit Description *(continued)*

Frame Buffer Clocking

The video DRAM shift clock (SCLK) is generated by the Bt484. SCLK is one eigth, one fourth, or one half the pixel clock rate, depending on whether multiplexing is 8:1, 4:1, or 2:1, respectively. In the 1:1/VGA mode, SCLK = LCLK.

P0–P7 (A–D) are pixel data, 8 bits per pixel (4:1 MUX) and 4 bits per pixel (8:1 MUX) for 4 and 8 horizontally consecutive output pixels. P0–P7 (A–D) are always latched on the rising edge of LCLK.

The pixel clock is specified to be either PCLK 0 or PCLK 1 by command bit CR24.

Frame Buffer Pixel Port Interface

There are four 8-bit pixel ports, (A–D), used to interface to the frame buffer memory.

Video input data ports A through D are designated in the following manner to represent the order of pixel data presentation: Port A always corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by B, then C, and finally D, repeating the pattern ABCD, ABCD, until the first scan line is completely displayed.

For the cursor display, the output sequence depends on the CR23 command bit and the ODD/EVEN* input. For example, when either interlaced or noninterlaced operation is selected, the current field is displayed.

Scan line 1 is displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 2 immediately follows scan line 1. In the interlaced mode, scan line 2 is considered to be the first line of the ODD field, and is displayed only after the entire EVEN field has been displayed and the ODD/EVEN pin has been toggled.

Only the ODD lines or only the EVEN lines will be displayed if the ODD/EVEN does not change.

Figure 1 shows the interlaced and noninterlaced display scan. Noninterlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

Pixel Read Mask Register

Each pixel clock cycle, P0–P7 pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true-color bypass is enabled. The pixel mask register is not initialized at the power-up/reset and should be initialized by the user to logical ones for proper operation.

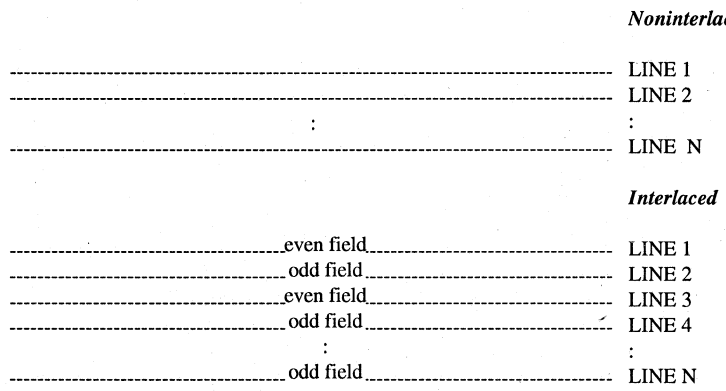


Figure 1. Interlaced / Noninterlaced Display Operation.

Circuit Description *(continued)*

Modes of Operation

4-Bits/Pixel Operation (8:1 MUX)

The 32 input bits are multiplexed 8:1 and are configured for 4 bits/pixel. There are eight independent 4-bit pixel ports, P7:4 (A–D) and P3:0 (A–D). The pixel bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every eight PCLK cycles. SCLK will be equal to the PCLK selected, divided by 8. The 4 bits from each port will select 1 of 16 locations in the palette (in the order presented in Table 3).

8-Bits/Pixel Operation (4:1 MUX)

The 32 input bits are multiplexed 4:1 and are configured for 8 bits/pixel. There are four independent 8-bit pixel ports, (A–D). The pixel bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every four PCLK cycles. SCLK will be equal to the PCLK selected, divided by 4. The 8 bits from each port will select 1 of 256 locations in the palette (in the order presented in Table 3).

16-Bits/Pixel Operation (2:1 MUX)

The 32 input bits are multiplexed 2:1 and are configured for 16 bits/pixel. Through bit CR12 in Command Register 1, 2:1 multiplexing is specified. There are two independent 16-bit pixel ports, (B–A) and (D–C). The bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every two PCLK cycles. SCLK will be equal to the PCLK selected, divided by 2. The pixel bits multiplexed in this mode are from the same ports of RGB color formats of 5:5:5 or 5:6:5. P7D and P7B are ignored internally when the 5:5:5 color format is selected (in the order presented in Table 3).

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and are transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the most significant bits of the respective palette address; the least significant bits are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the least significant bits of the respective palette address; the most significant bits are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors, respectively. The DACs can be configured for 6 or 8 bits of resolution in this mode.

16-Bits/Pixel Operation (1:1 MUX)

The 1:1 multiplexing mode is selected through CR12 in Command Register 1. If this mode is selected, two 16-bit pixel ports, (B–A) and (D–C), are latched on the rising edge of LCLK and are multiplexed 1:1. Selection between the two ports is made by bit CR10 in Command Register 1. One rising edge of LCLK should occur every PCLK cycle. SCLK is equal to the PCLK selected.

Bit P7D is used to switch between the two ports on a pixel-by-pixel basis when 5:5:5 RGB color format (bit CR13 in Command Register 1) and real-time pixel port switching (bit CR11 in Command Register 1) is enabled. If PORTSEL is a logical zero, the VGA port is multiplexed regardless of the state of P7D. Bit P7B is ignored internally when in 5:5:5 mode. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

Bits P7B and P7D are ignored internally if 5:5:5 RGB color format is selected and real-time pixel port switching is disabled. Programming bit CR10 in Command Register 1 determines switching for both 5:5:5 and 5:6:5 RGB color formats.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the most significant bits of the respective palette address; the least significant bits are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the

PORTSEL	CR11	CR10	P7D	CR12	CR13	CR16	CR15	Ports MUXed	MUX Rate	Operating Modes
0	x	x	x	x	x	0	0	VGA(7:0)	1:1	VGA
1	x	x	Data	x	x	1	1	P7:4(A) P3:0(A) P7:4(B) P3:0(B) P7:4(C) P3:0(C) P7:4(D) P3:0(D)	8:1	4-Bits/Pixel
1	x	x	Data	x	x	1	0	P7:0(A) P7:0(B) P7:0(C) P7:0(D)	4:1	8-Bits/Pixel
1	x	x	x	0	0	0	1	P7:0(B-A) P7:0(D-C)	2:1	16-Bits/Pixel (5:5:5) (see Table 4)
1	x	x	Data	0	1	0	1	P7:0(B-A) P7:0(D-C)	2:1	16-Bits/Pixel (5:6:5) (see Table 5)
1	0	0	x	1	0	0	1	P7:0(B-A)	1:1	16-Bits/Pixel (5:5:5)
1	0	1	x	1	0	0	1	P7:0(D-C)	1:1	16-Bits/Pixel (5:5:5)
1	1	x	0	1	0	0	1	P7:0(B-A)	1:1	16-Bits/Pixel (5:5:5) (Note 1) (see Table 4)
1	1	x	1	1	0	0	1	P7:0(D-C)	1:1	16-Bits/Pixel (5:5:5) (Note 1) (see Table 4)
1	x	0	x	1	1	0	1	P7:0(B-A)	1:1	16-Bits/Pixel (5:6:5) (see Table 5)
1	x	1	Data	1	1	0	1	P7:0(D-C)	1:1	16-Bits/Pixel (5:6:5) (see Table 5)
1	x	x	x	x	x	0	0	P7:0(C-A)	1:1	24-Bits/Pixel (see Table 6)

Note 1: At this time, the Bt484 is not operable above 50 MHz in the 16-bits-per-pixel 1:1-multiplexed mode when pixel pin P7D is the real-time switch.

Table 3. Modes of Operation (Pixel Port Configuration).

least significant bits of the respective palette address; the most significant bits are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors, respectively. The DACs can be configured for 6 or 8 bits of resolution in this mode.

Bit	MSB															LSB
Format	S	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B
Port 1	S	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	S	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

If bit CR11 in Command Register 1 is a logical zero, then S=CR10 bit, 16-bit/pixel port switch control (1:1 multiplexing, CR12 = 1). If bit CR11 in Command Register 1 is a logical one, then S=P7D bit, real-time pixel port switch (1:1 multiplexing, CR12 = 1).

Table 4. 5:5:5 RGB Color Format for Both 2:1 and 1:1 Multiplexing Modes.

Bit	MSB															LSB
Format	R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B
Port 1	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	P7D	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

Table 5. 5:6:5 RGB Color Format for Both 2:1 and 1:1 Multiplexing Modes.

Bit	MSB																						LSB
Format	R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B
Port	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A

Note: P7:0(D) are ignored.

Table 6. 24-Bits/Pixel RGB Color Format.

24-Bits/Pixel Operation (1:1 MUX)

When 24-bits-per-pixel is selected, there is one 24-bit pixel port. The pixel bits, P7:0 (C–A), are latched on the rising edge of LCLK and are multiplexed 1:1. One rising edge of LCLK should occur every PCLK cycle. SCLK is equal to the PCLK selected. The RGB color format in this mode is 8:8:8.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When 8:8:8 color format is selected, the display can contain 16.8 million simultaneous colors. The DACs should be configured for 8 bits of resolution in this mode (CR14=1 and CR01=1).

VGA Port

An 8-bit pixel port is provided to support VGA pixel data. The data is latched on the rising edge of LCLK. One rising edge of LCLK should occur every PCLK cycle. SCLK will equal the PCLK selected. A logical zero on the PORTSEL pin ensures that the VGA port is selected. A logical one on the PORTSEL pin selects the pixel port. To use the VGA PORTSEL feature the RAMDAC *must* be configured in the 1:1 multiplexing mode through the RAM (CR14 = 0) or pallette bypass (CR14 = 1). After the RAMDAC has been properly configured, the VGA PORTSEL can then be used to select

	MSB							LSB	
Pixel Mask Register	7	6	5	4	3	2	1	0	Register Bits
VGA Data	7	6	5	4	3	2	1	0	Palette Index
4 Bits/Pixel	x	x	x	x	3	2	1	0	Palette Index
8 Bits/Pixel	7	6	5	4	3	2	1	0	Palette Index
16 Bits/Pixel	7	6	5	4	3	x	x	x	Red Palette Index
5:5:5 Format	7	6	5	4	3	x	x	x	Green Palette Index
SPARSE	7	6	5	4	3	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	4	3	2	1	0	Red Palette Index
5:5:5 Format	x	x	x	4	3	2	1	0	Green Palette Index
CONTIGUOUS	x	x	x	4	3	2	1	0	Blue Palette Index
16 Bits/Pixel	7	6	5	4	3	x	x	x	Red Palette Index
5:6:5 Format	7	6	5	4	3	2	x	x	Green Palette Index
SPARSE	7	6	5	4	3	x	x	x	Blue Palette Index
16-Bits/Pixel	x	x	x	4	3	2	1	0	Red Palette Index
5:6:5 Format	x	x	5	4	3	2	1	0	Green Palette Index
CONTIGUOUS	x	x	x	4	3	2	1	0	Blue Palette Index
24 Bits/Pixel	7	6	5	4	3	2	1	0	Red Palette Index
8:8:8 Format	7	6	5	4	3	2	1	0	Green Palette Index
	7	6	5	4	3	2	1	0	Blue Palette Index

Table 7. Pixel Index Masking.

between the pixel port and the VGA port on a pixel-by-pixel basis. The PORTSEL pin can also be used to switch between VGA and the pixel ports in 2:1, 4:1, or 8:1 MUX modes on a frame-by-frame basis. The VGA pixels address the color palette when selected. Only PCLK0 should be used when switching between the VGA and pixel ports on a pixel-by-pixel basis. PCKL1 should be used when switching between the VGA and pixel ports on a frame-by-frame basis. The 8-bit VGA data forms a common index into the palette, selecting 1 of 256 colors. Valid data begins at address zero.

Pixel Read Mask Register

The pixel data can be masked with the 8-bit pixel mask register before being transferred to the color palette. The pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true-color bypass is enabled. The pixel read mask register is not initialized at the power-up/reset and must be initialized by the user to logical ones for proper operation (see Table 7).

Cursor Operation

The Bt484 has an on-chip, three-color, 32 x 32 x 2 pixel user-definable cursor. This cursor can be used with both interlaced and noninterlaced systems.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor position register (Xp,Yp) (see Figure 2). A (0, 0) written to the cursor position registers will place the cursor off the screen. A (1, 1) written to the cursor position registers will place the lower right pixel of the cursor on the upper left corner of the screen. Only one cursor pattern per frame is displayed at the location specified for both interlaced and noninterlaced display formats, regardless of the number of updates to (Xp,Yp). The cursor's vertical or horizontal location is not affected during any frame displayed. There are no restrictions on updating (Xp, Yp) other than that both cursor position registers must be written when the cursor location is updated. Internal x- and y-position registers

Circuit Description *(continued)*

are loaded after the upper byte of Yp has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written.

Cursor positioning is relative to CDE. The cursor position is not dependent upon CBLANK* (see Figure 2). The reference point of the cursor (row 0, column 0) is in the lower right corner. The cursor Xp position is relative to the first rising edge of LCLK when CDE is sampled at logical one. The cursor Yp position is relative to the first rising edge of LCLK when CDE is sampled at logical one after the CDE vertical blanking interval has been determined (see Figure 2). If a CDE transition from logical zero to logical one (as determined by LCLK) does not occur within 2048 PCLKs (2048 LCLKs when in 1:1 MUX mode), CDE is in vertical blanking. In 8:1, 4:1, or 2:1 MUX modes, cursor timing is based on the PCLK selected. When the MUX rate is 1:1, cursor timing is based on LCLK.

The cursor pattern can be displayed in an interlaced system if bit CR23 in Command Register 2 is a logical one. If Yp is greater than 32 ($0020), and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the ODD/EVEN* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field, and the data in row 31 of the cursor RAM array will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, then the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 31 of the cursor RAM array will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 32 ($0020), cursor display does not depend on whether Yp is odd or even. If the ODD/EVEN* pin is a logical zero, the first line of the cursor is displayed on scan line 1. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field will correspond to subsequent scan lines in the even field. If the ODD/EVEN* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line 2. Each subsequent scan line displayed in

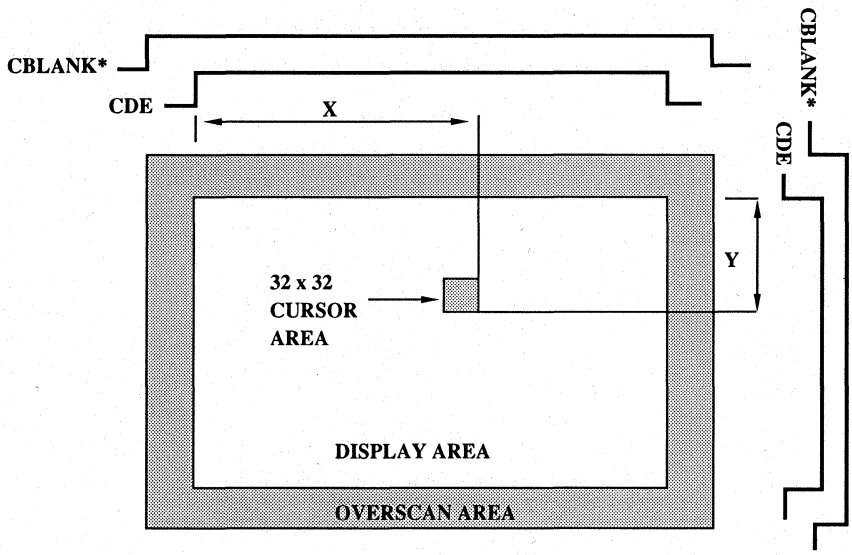


Figure 2. Cursor Positioning.

the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field. If bit CR23 is a logical zero, the cursor must be displayed in a noninterlaced system. Scan lines displayed in a frame correspond to sequential cursor lines in the cursor RAM relative to the first active cursor line in the frame.

Figure 3 is a visual explanation of planar pixel format and cursor RAM array pixel mapping.

Cursor Color Support

The cursor has three modes for color selection. Bits CR21 and CR20 in Command Register 2 determine which cursor mode is to be used. Mode 1 is a three-color cursor, mode 2 is referred to as a PM/Window cursor, and mode 3 is referred to as an X-Windows cursor (see Table 8).

Highlight Logic

The highlight logic is enabled in cursor mode 2 when both plane data (plane 1 and plane 0) are logical ones (see Table 8). When the highlight logic is enabled, it ensures that the pixel highlighted has a unique color. This is because the highlight logic bit-wise complements the 24- or 18-bit palette or bypass data supplied to the DACs.

Video Generation

The CSYNC* and CBLANK* inputs are latched on the rising edge of LCLK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, and produce the specific output levels required for video applications, as illustrated in Figures 4 and 5. Tables 9 and 10 detail how the CSYNC* and BLANK* inputs modify the output levels.

The CR05 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command bits CR02, CR03, and CR04 specify whether the RGB outputs contain sync information.

SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, or IOB outputs have exceeded the internal voltage reference level of the SENSE* comparator circuit. This output is used to determine the presence of a CRT monitor, and through diagnostic code, the difference between a loaded or an unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For the proper operation of the SENSE circuit, the following levels should be applied to the comparator by the IOR, IOG, and IOG outputs:

DAC Low Voltage ≤ 310 mV

Plane 1	Plane 0	MODE 1	MODE 2	MODE 3
0	0	Palette Data	Cursor Color 1	Palette Data
0	1	Cursor Color 1	Cursor Color 2	Palette Data
1	0	Cursor Color 2	Palette Data	Cursor Color 1
1	1	Cursor Color 3	Complement Palette Data	Cursor Color 2

Table 8. Overlay Color Modes.

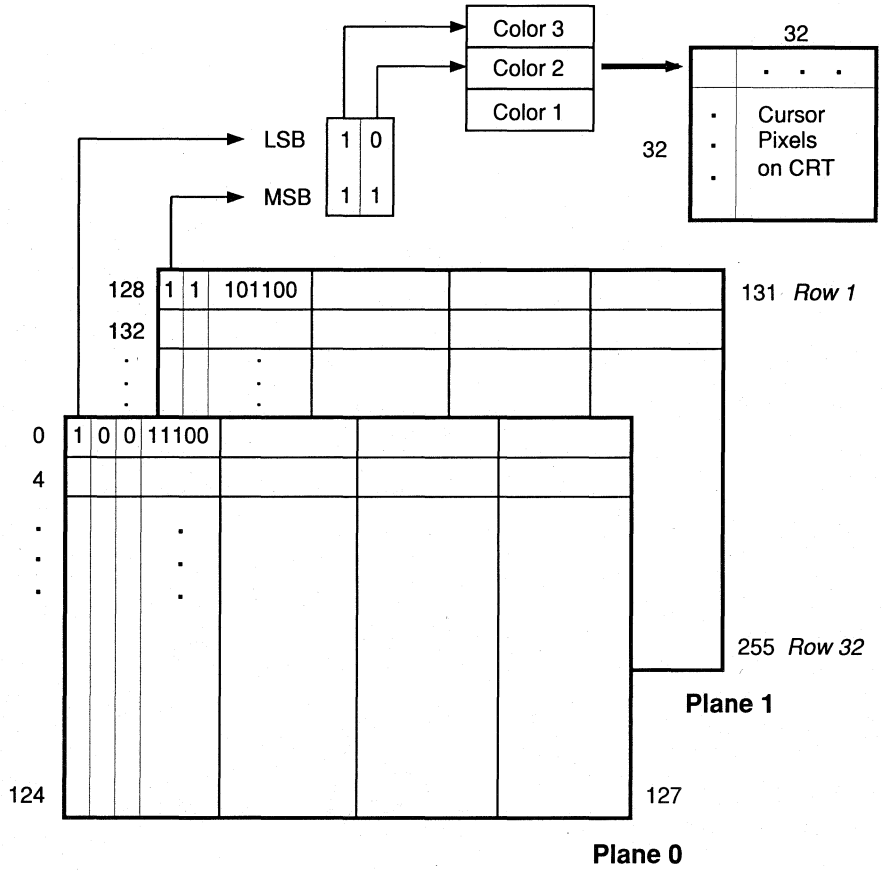
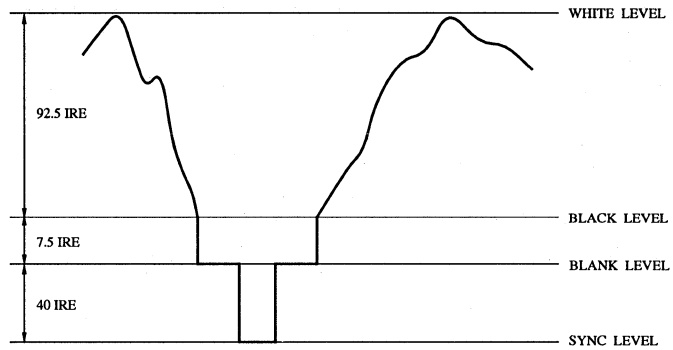


Figure 3. Planar Pixel Format and Cursor RAM Array Pixel Mapping.

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RSET ~ 143 Ω. RS-343A levels and tolerances are assumed on all levels.

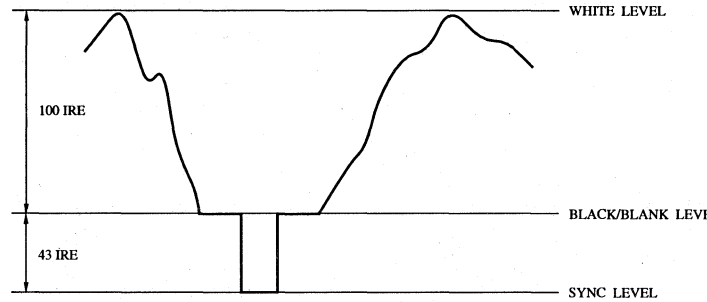
Figure 4. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RSET ~ 143 Ω.

Table 9. Video Output Truth Table (SETUP = 7.5 IRE).

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RSET ~ 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 5. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RSET~ 143 Ω.

Table 10. Video Output Truth Table (SETUP = 0 IRE).

Command Register 0 (RS value = 0110)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR00 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zeros when a low signal is asserted on the RESET* pin.

CR07	Reserved. (logical zero)	This bit is reserved for future expansion. A logical zero must be written to this bit to ensure proper operation.
CR06	Clock Disable ANDed with CR00 (0) Normal Operation (1) Disable Internal Clocking	When this bit *and* CR00 are a logical one, the internal clock and SCLK are disabled to further conserve power when in power-down mode. The RAM still retains the data, and MPU reads and writes can occur without loss of data. When this bit is a logical zero, internal clocking is enabled, and SCLK will be generated.
CR05	Setup Enable (0) Disable SETUP (0 IRE) (1) Enable SETUP (7.5 IRE)	This bit determines the video blanking pedestal. A logical zero sets a 0 IRE blanking pedestal, and a logical one sets 7.5 IRE.
CR04 CR03 CR02	Blue Sync Enable Green Sync Enable Red Sync Enable (0) Disable Sync (1) Enable Sync	These bits specify whether the respective IOB, IOG, or IOR output is to contain sync information.
CR01	DAC 6/8-Bit Resolution (0) 6-bit Operation (1) 8-bit Operation	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle.
CR00	Power-Down Enable (0) Normal Operation (1) Power-Down Operation	While this bit is a logical zero, the device operates normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data, and CPU reads and writes can occur with no loss of data. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used.

Command Register 1 (RS value = 1000)

This register may be written to or read by the MPU at any time. The bits in this register are not initialized. CR10 corresponds to data bus bit D0, the least significant data bit (see Table 4). All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR17	Reserved (logical zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR16, 15	Bit/Pixel Select (00) One 24-Bit Pixel (01) One or Two 16-Bit Pixels (10) Four 8-Bit Pixels (11) Eight 4-Bit Pixels	These bits select the pixel size depth and determine the multiplexing rates for 4-, 8-, and 24-bit/pixel operation. The 16-bit/pixel multiplexing rate is set by the state of CR12.
CR14	True-Color Bypass Enable (0) Pixel Addresses Palette (1) Pixel Bypasses Palette	When this bit is a logical zero, the pixel palette is addressed by the pixel data. When this bit is a logical one, the RGB pixel data bypasses the color palette and drives the DACs directly. True-color bypassing is available only for pixel sizes of 16 and 24 bits.
CR13	16-Bit RGB Color Format (0) 5:5:5 R:G:B Color Format (1) 5:6:5 R:G:B Color Format	This bit selects the RGB color format for 16-bit/pixel operation.
CR12	16-Bit Multiplexing Rate (0) 2:1 Multiplexing (1) 1:1 Multiplexing	When this bit is a logical zero, and CR16 and 15 are set to 01, two 16-bit values are latched in during every LCLK cycle. When this bit is a logical one, and CR16 and 15 are set to 01, one 16-bit value is output during every LCLK cycle. This bit is ignored if CR16/CR15 specify 4-, 8-, or 24-bit/pixel operation.
CR11	16-Bit Real-Time Switch Enable (0) CR10 Controls Selection (1) P7D Controls Selection	This bit is only valid when CR13 = 0 (5:5:5 format) and CR12 = 1 (1:1 multiplexing) are specified. When this bit is a logical zero, CR10 switches the ports multiplexed. When this bit is a logical one, pixel port bit P7D switches the ports multiplexed. This bit is ignored when 5:6:5 RGB color format is selected (when bit CR13 is a logical one).
CR10	16-Bit/Pixel Port Switch Control (0) Multiplex Port [B–A] (1) Multiplex Port [D–C]	This bit specifies which 16-bit port is selected for either 5:5:5 (CR13 = 0) or 5:6:5 (CR13 = 1) mode. In order for this bit to control which 16-bit port is selected, CR12 must be a logical one (16-bit 1:1 multiplexing). This bit is ignored when real-time port switching is enabled (CR11 = 1).

Internal Registers *(continued)*

Command Register 2 (RS value = 1001)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR20 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR27 SCLK Disabled
(0) SCLK Enabled
(1) SCLK Disabled

A logical zero must be written to this bit to enable SCLK to be output. A logical one written to this bit three-states the SCLK output.

CR26 Test Path Enable

(0) Normal Operation
(1) Test Path Enabled

When this bit is set to a logical zero, the device operates normally. A logical one enables certain test paths to be internally set up. This involves any input mode and any inputs that affect access to the color palette RAM. When this bit is set to a logical one, the pixel data is accessible on the MPU data bus. While this test mode is enabled, the device will not operate at speed.

CR25 PORTSEL Mask

(0) Masked
(1) Nonmasked

This bit determines the selection of the input port. It is logically ANDed with the PORTSEL pin. A logical zero selects the VGA port. When this bit is a logical one, the PORTSEL pin selects either the VGA or pixel port.

CR24 CLKSEL Enable

(0) PCLK0 Selected
(1) PCLK1 Selected

When this bit is a logical zero, PCLK0 is selected. When this bit is a logical one, PCLK1 is selected. To eliminate glitches on the SCLK output, switching between PCLKs should occur only when the multiplexing rate is 8:1 or 4:1. To ensure the integrity of the palette, the device should be put in sleep mode before switching clocks.

CR23 Display Mode Select

(0) Noninterlaced
(1) Interlaced

When this bit is a logical zero, the display format is noninterlaced. When the bit is a logical one, the display format is interlaced. The mode must be set properly to ensure proper operation of the internal cursor.

CR22 16-Bit/Pixel Palette Index Select

(0) Sparse Indexing
(1) Contiguous Indexing

When this bit is a logical zero, palette addressing is sparse. The RGB color component pixel data is mapped to the most significant bits of the RGB palette address. The least significant of the palette address bits are set to zero. When this bit is a logical one, palette addressing is contiguous. The RGB color component pixel data is mapped to the least significant bits of the palette address. The most significant bits of the address are set to zero.

CR21, 20 Cursor Mode Select

(00) Cursor Disabled
(01) Three-Color Cursor
(10) Two-Color/Highlight Cursor
(11) Two-Color/X-Windows Cursor

These bits determine the functionality of the onboard 32 x 32 x 2 cursor.

Pixel Read Mask Register (RS value = 0010)

The 8-bit pixel read mask register may be written to or read by the MPU at any time, and *is not* initialized at power-up. D0 is the least significant bit. The contents of this register are bit-wise ANDed with the pixel data prior to addressing the color palette RAM. The pixel read mask register must be initialized by the user to logical ones for proper operation.

Status Register (RS value = 1010)

The 8-bit status register monitors certain device states and identifies devices. It may be read by the MPU at any time; MPU write cycles to this register are ignored. D0 is the least significant bit corresponding to SR0. This register is not reset during power-up/reset.

SR7–SR6: These bits are identification values. SR7 = 0 and SR6 = 1.

SR5–SR4: These bits are revision values.

SR3: This is the SENSE* bit. If it is a logical zero, one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (370 mV). This bit is used to determine the presence of a CRT monitor, and with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned.

The SENSE reference has an additional ±10-percent tolerance when an internal voltage reference is used.

SR2: (0) Write Cycle
(1) Read Cycle

Read/write access status. This bit provides RD/WR status when address register $0, $3, $4, or $7 has been written to. When address register $0 or $4 has been written, the device is in the write mode and this bit is a logical zero. When address register $3 or $7 has been written, the device is in the read mode and this bit is a logical one.

SR1–SR0: These bits reflect the color component address for the next RD/WR cycle when the palette, cursor color registers, or overscan register are accessed.

Address [a,b] state: (00) Red Color Component
(01) Green Color Component
(10) Blue Color Component

Cursor (x,y) Registers (RS values: CXLR = 1100, CXHR = 1100, CXYL = 1110, and CXYH = 1111)

These registers are used to specify the (x,y) coordinate of the 32 x 32 x 2 hardware cursor. The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 32 (or $0020)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) register. If Xp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation in the Circuit Description section).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 32 (or $0020)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation).

Pin Descriptions

Pin Name	Pin #	Description
RESET*	47	Reset input (TTL compatible). When this signal is low, all the command register bits are set to zero. At reset, the device will be in VGA mode. The pixel read mask register is not initialized on reset and must be initialized by the user to logical ones for proper operation.
CBLANK*	65	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as illustrated in Tables 9 and 10. CBLANK* is latched on the rising edge of LCLK. When BLANK* is a logical zero, the pixel inputs are ignored. The falling edge of this signal determines the polarity of the CSYNC* input pin. The onboard cursor positioning counters are referenced to this signal.
CSYNC*	64	Composite sync control input (TTL compatible). The polarity of this pin is determined on the last rising LCLK edge before the falling edge of CBLANK*. CSYNC* does not override any other control or data input, as shown in Tables 9 and 10; therefore, it should be asserted only during the blanking interval. CSYNC* is latched on the rising edge of LCLK. Bits CR04, CR03, and CR02 in Command Register 0 can disable sync on IOB, IOG, or IOR outputs, respectively.
CDE	63	Composite display enable control input (TTL compatible). The state of this signal and CBLANK* determines whether the analog outputs are blanked or contain cursor color, pixel , or overscan data. This signal is latched on the rising edge of LCLK. If overscanning is not used, this pin must be tied to CBLANK*. The following is a list of combinations of CDE and CBLANK*: PORTSEL / CDE / CLBANK* / x / x / 0 / Video Blanking 0 / 0 / 1 / VGA Pixel Data 0 / 1 / 1 / Cursor Color, Pixel Data, or VGA Data 1 / 0 / 1 / Overscan Data 1 / 1 / 1 / Cursor Color or Pixel Data
ODD / EVEN*	62	Odd/even field input (TTL compatible). This signal should be changed only during vertical blank. This input is used to ensure proper operation of the onboard cursor when interlaced operation (command bit CR23=1) is selected. When this signal is a logical zero, an even field is specified. When this signal is a logical one, an odd field is specified. This input is ignored if noninterlaced operation (command bit CR23=0) is selected.
PCLK0	78	Pixel Clock 0 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical zero. The signal on this pin should be the VGA pixel clock. This clock should be specified when switching between the pixel and VGA ports on a pixel-by-pixel basis (in 1:1 mode, only). It is recommended that all clock inputs be driven by a dedicated buffer to avoid reflection-induced jitter. Refer to the PC Board Layout Considerations section for critical layout criteria.
PCLK1	76	Pixel Clock 1 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical one. The signal on this pin is typically the high-speed pixel clock used during multiplexed operation of the pixel port. Refer to the PC Board Layout Considerations section for critical layout criteria.
SCLK	83	VRAM shift clock output (TTL compatible). The signal on this pin is equal to the selected pixel clock divided by 8, 4, 2, or 1, depending on the operating mode selected.

Pin Descriptions *(continued)*

Pin Name	Pin #	Description
LCLK	81	Latch clock input (TTL compatible). The rising edge of this signal latches P7:0 (A–D) or VGA [7:0], and CBLANK*, CDE, CSYNC*, and PORTSEL. The information latched by this signal is synchronized internally with SCLK. Because of this synchronization process, there is a timing window on both sides of SCLK where LCLK must not rise (see AC Characteristics section). This timing window is necessary so that data latched by LCLK does not interfere with the setup and hold times required by the internal synchronizing latch. Data is synchronized with the selected pixel clock after being internally latched with SCLK. When the multiplexing rate is 8:1, 4:1, 2:1, or 1:1, this signal is equal to the selected pixel clock divided by 8, 4, 2, or 1, respectively.
P7:0 (A–D)	1–32	Pixel port inputs (TTL compatible). This port is selected if PORTSEL is a logical one. The appropriate pins on this port are multiplexed at rates of either 1:1, 2:1, 4:1, or 8:1, depending on the operating mode selected. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
VGA[7:0]	67–74	VGA port inputs (TTL compatible). This VGA port is selected if PORTSEL is a logical zero and only when in a 1:1 multiplexing mode. This port is always multiplexed 1:1. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
PORTSEL	66	VGA/pixel port select input (TTL compatible). This pin is ANDed with control register bit CR25 to determine whether the pixel port or VGA port is selected. A logical zero on this pin selects the VGA port only when in the 1:1 multiplexing mode regardless of the state of CR25. A logical one selects the pixel port if CR25=1. If a 1:1 multiplexing rate has been specified, this pin may be used to switch between the pixel and VGA ports on a pixel-by-pixel basis. Switching between the VGA and pixel ports cannot be done in 2:1, 4:1, or 8:1 MUX modes. This pin should not be left floating.
WR*	48	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS3 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. Refer to MPU Control Signal Interfacing in the PC Board Layout Considerations section for detailed layout suggestions.
RD*	49	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS3 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. Refer to MPU Control Signal Interfacing in the PC Board Layout Considerations section for detailed layout suggestions.
RS0–RS3	50–53	Register select inputs (TTL compatible). RS0–RS3 specify the type of read or write operation being performed, as shown in Tables 1 and 2. Refer to MPU Control Signal Interfacing in the PC Board Layout Considerations section for detailed layout suggestions.
D0–D7	54–61	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
SENSE*	46	Comparator sense output (CMOS compatible). This pin will be low if one or more of the IOR, IOG, and IOB analog output levels exceed the internal comparator reference level. The sense output can drive only one CMOS load.
IOR, IOG, IOB	35,37,39	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Description</th></tr>
<tr><td>FSADJUST</td><td>33</td><td>Full-scale adjust control. The IRE relationships in Figures 4 and 5 are maintained, regardless of the full-scale output current.

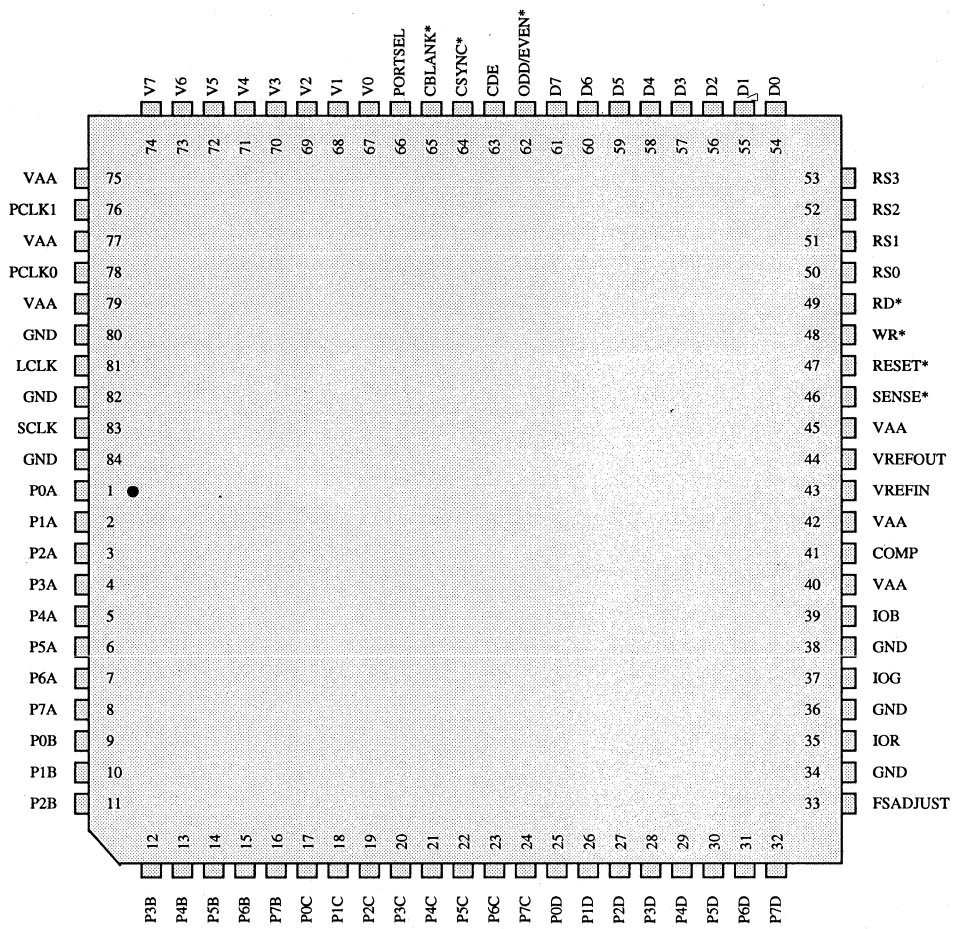
When an external or the internal voltage reference (Figures 6 and 7 in the PC Board Layout Considerations section) is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

K is defined in the table below. It is recommended that a 143 Ω RESET resistor be used for doubly- terminated 75 Ω loads (i.e., RS-343A applications).

<table>
<tr><th></th><th colspan="2">Sync Enabled</th><th colspan="2">Sync Disabled</th></tr>
<tr><th>Setup</th><td>0 IRE</td><td>7.5 IRE</td><td>0 IRE</td><td>7.5 IRE</td></tr>
<tr><th>K (8 bits)</th><td>2.888</td><td>3.055</td><td>2.045</td><td>2.207</td></tr>
<tr><th>K (6 bits)</th><td>2.867</td><td>3.029</td><td>2.021</td><td>2.183</td></tr>
</table>
</td></tr>
<tr><td>VREF OUT</td><td>44</td><td>Voltage reference output. This output provides a 1.2 V (typical) reference and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating. (See Figures 6 and 7.) Up to four Bt484s can be driven by this output.</td></tr>
<tr><td>VREF IN</td><td>43</td><td>Voltage reference input. If an external voltage reference is used (Figure 7), it must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figures 6 and 7. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor (Figure 6).</td></tr>
<tr><td>COMP</td><td>41</td><td>Compensation pin. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>VAA</td><td>40,42,45,75,77,79</td><td>Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>GND</td><td>34,36,38,80,82,84</td><td>Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
</table>

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt484, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook.*

The layout should be optimized for lowest noise on the Bt484 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt484 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt484 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 6 and 7. This bead should be located within 3 inches of the Bt484. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 6 and 7 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt484 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt484 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt484 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt484 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt484 to minimize reflections. Unused analog outputs should be connected to GND.

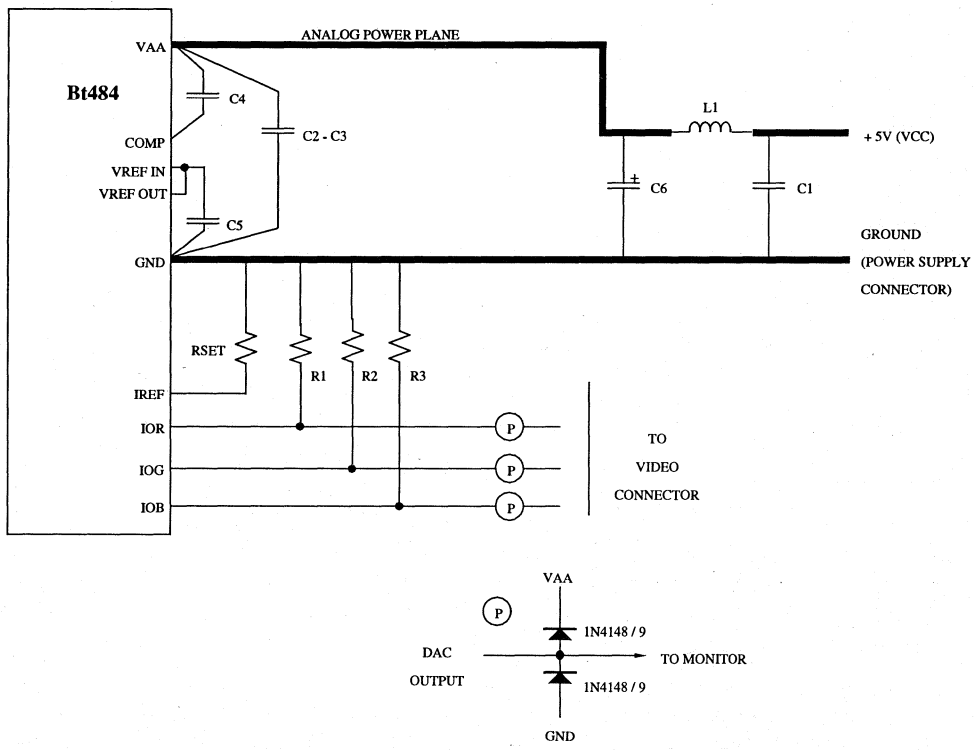
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt484 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 6 and 7 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



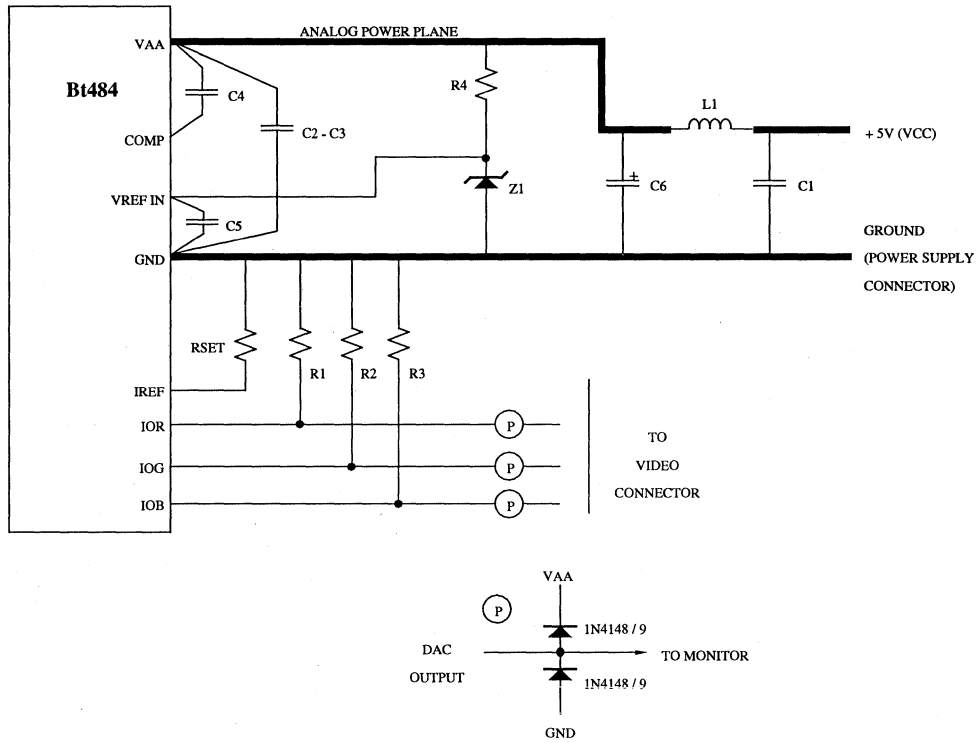
Note: For operation above 75 MHz, each group of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt484.

Figure 6. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: For operation above 75 MHz, each group of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	143 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt484.

Figure 7. Typical Connection Diagram and Parts List (External Voltage Reference).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration	VREF				V
Reference Voltage		1.112	1.235	1.359	

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or more than –0.5 V below ground can induce destructive latchup.

Application Information

Using Multiple Devices

When multiple Bt484s are used, each Bt484 should have its own power plane ferrite bead. If the internal reference is used, each Bt484 should use its own internal reference.

Although the multiple Bt484s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt484 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about ten times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Onboard VREF	VREFOUT	1.103	1.225	1.348	V
Voltage Reference Input Current	IVR IN		1.4	2.3	mA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, RSET = 143 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: When the Bt484 is in the 6-bit mode, the output levels are approximately 1.5-percent lower than these values.

AC Characteristics

		85 MHz Devices			75 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
PCLK 0, PCLK 1 All MUX Rates	Fmax			85			75	MHz
RS0–RS3 Setup Time (Figure 8)	1	10			10			ns
RS0–RS3 Hold Time	2	10			10			ns
RD* Asserted to D0–D7 Driven	3	2			2			ns
RD* Asserted to D0–D7 Valid	4			40			40	ns
RD* Negated to D0–D7 3-Stated	5			20			20	ns
Read D0–D7 Hold Time	6	2			2			ns
Write D0–D7 Setup Time	7	10			10			ns
Write D0–D7 Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*pclk			6*pclk			ns
LCLK Rates (Figures 9 and 10)	Lmax							
8:1 Multiplexing				10.63			9.38	MHz
4:1 Multiplexing				21.25			18.75	MHz
2:1 Multiplexing				42.50			37.50	MHz
1:1 Multiplexing or VGA				85			75	MHz
SCLK Rate	Smax							
8:1 Multiplexing				10.63			9.38	MHz
4:1 Multiplexing				21.25			18.75	MHz
2:1 Multiplexing				42.50			37.50	MHz
1:1 Multiplexing or VGA				50.35			50.35	MHz
PCLK 0, PCLK 1 Cycle Time All MUX Rates	11	11.77			13.33			ns
PCLK 0, PCLK 1 Pulse Width High All MUX Rates	12	5			5			ns
PCLK 0, PCLK 1 Pulse Width Low All MUX Rates	13	4			4			ns
LCLK Cycle Time	14							
8:1 Multiplexing		94.12			106.61			ns
4:1 Multiplexing		47.06			53.33			ns
2:1 Multiplexing		23.53			26.67			ns
1:1 Multiplexing or VGA		11.77			13.33			ns
LCLK Pulse Width High	15							
8:1 Multiplexing		5			5			ns
4:1 Multiplexing		5			5			ns
2:1 Multiplexing		5			5			ns
1:1 Multiplexing or VGA		5			5			ns
LCLK Pulse Width Low	16							
8:1 Multiplexing		4			4			ns
4:1 Multiplexing		4			4			ns
2:1 Multiplexing		4			4			ns
1:1 Multiplexing or VGA		4			4			ns

See test conditions at the end of this section.

AC Characteristics *(continued)*

Parameter	Symbol	85 MHz Devices Min	85 MHz Devices Typ	85 MHz Devices Max	75 MHz Devices Min	75 MHz Devices Typ	75 MHz Devices Max	Units
SCLK Cycle Time	17							
8:1 Multiplexing		94.12			106.67			ns
4:1 Multiplexing		47.06			53.33			ns
2:1 Multiplexing		23.53			26.67			ns
1:1 Multiplexing or VGA		19.86			19.86			ns
Data Setup to LCLK P7:0(A–D)	18	1			1			ns
Data Hold from LCLK P7:0(A–D)	19	5			5			ns
Data Setup and Hold ro LCLK VGA (7:0), CDE, CBLANK* CSYNC*, PORTSEL	20	3			3			ns
SCLK Output Delay (1:1 mode)	21		6	11		6	11	ns
SCLK Output Delay (MUX mode)			10	20		10	20	ns
Analog Output Delay				30			30	ns
Analog Output Rise/Fall Time	22		3			3		ns
Analog Output Settling Time (Note 1)	23		13			13		ns
Clock and Data Feedthrough (Note 1)	24		–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV – sec
SENSE* Output Delay	25		1			1		µs
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
VAA Supply Current (Note 2)	IAA							mA
Normal Operation			260	330		260	330	mA
Sleep Mode (Note 3)			TBD	TBD		TBD	TBD	mA

See test conditions and notes at the end of this section.
(@) T = SCLK Cycle Time

Pipeline Delay	MIN	MAX
1:1/VGA mode	8 LCLKS	8 LCLKS
2:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 8 PCLKS
4:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 10 PCLKS
8:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 14 PCLKS

Note: Pipeline Delay (MIN) is the minimum number of clocks required to output 1 pixel after all pixels have been latched. Pipeline delay (MAX) is the maximum number of clocks required to output all pixels after all pixels have been latched. In the 1:1/VGA mode, LCLK is the primary clock latching and pipelining for the pixels.

AC Characteristics *(continued)*

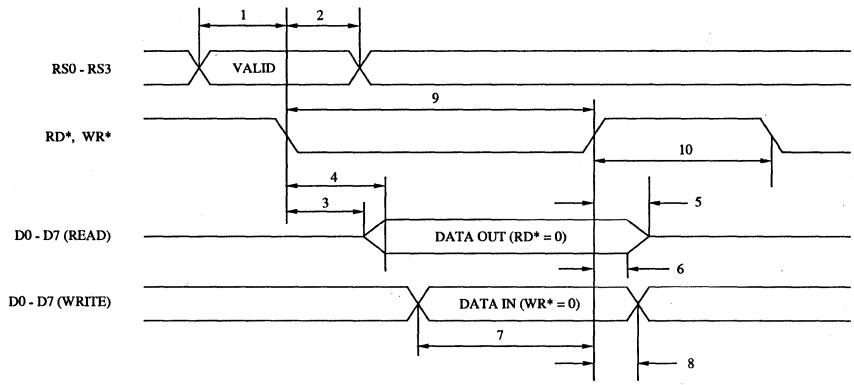
Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 147 Ω. TTL input values are 0–3 V with input rise/fall times ≤4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF; SENSE* and D0–D7 output load ≤50 pF. SCLK output load = 50 pF. See timing notes in Figures 8, 9, and 10. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: 75 MHz. IAA (typ) at VAA = 5.0 V, and 25°C. IAA (max) at VAA = 5.25 V, and 70°C. 4:1 MUX mode at 40-percent blanking. Temperature coefficient = 0.4 mA/°C for decreasing temperatures. The temperature coefficient will increase IAA by 30 mA at 0° C.

Note 3: External voltage reference is disabled during sleep mode, all inputs are low, and clock is running.

Timing Waveforms



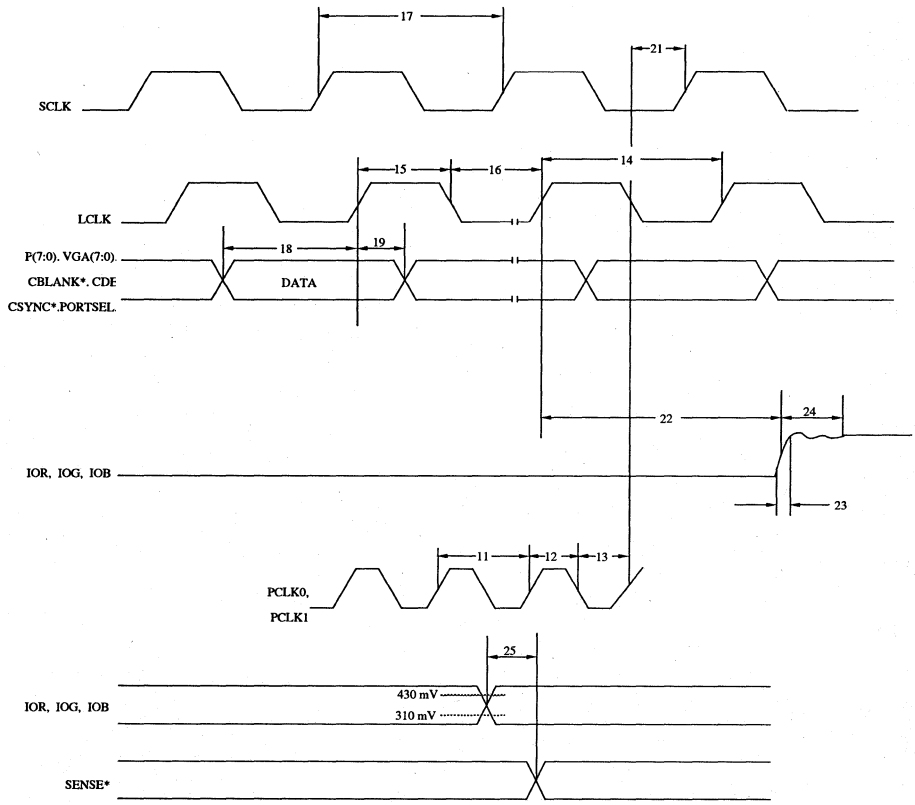
Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. MPU Read/Write Timing.

Timing Waveforms *(continued)*



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

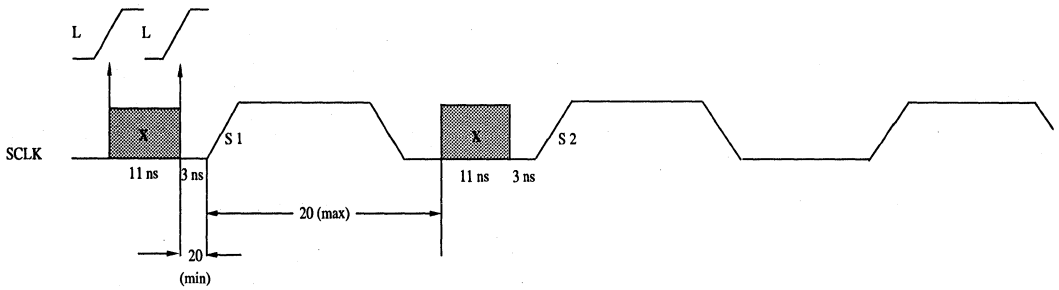
Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 9 . Video Input/Output Timing (Non-1:1).

4

Timing Waveforms *(continued)*



L = LCLK rising edges

S1 = First SCLK rising edge

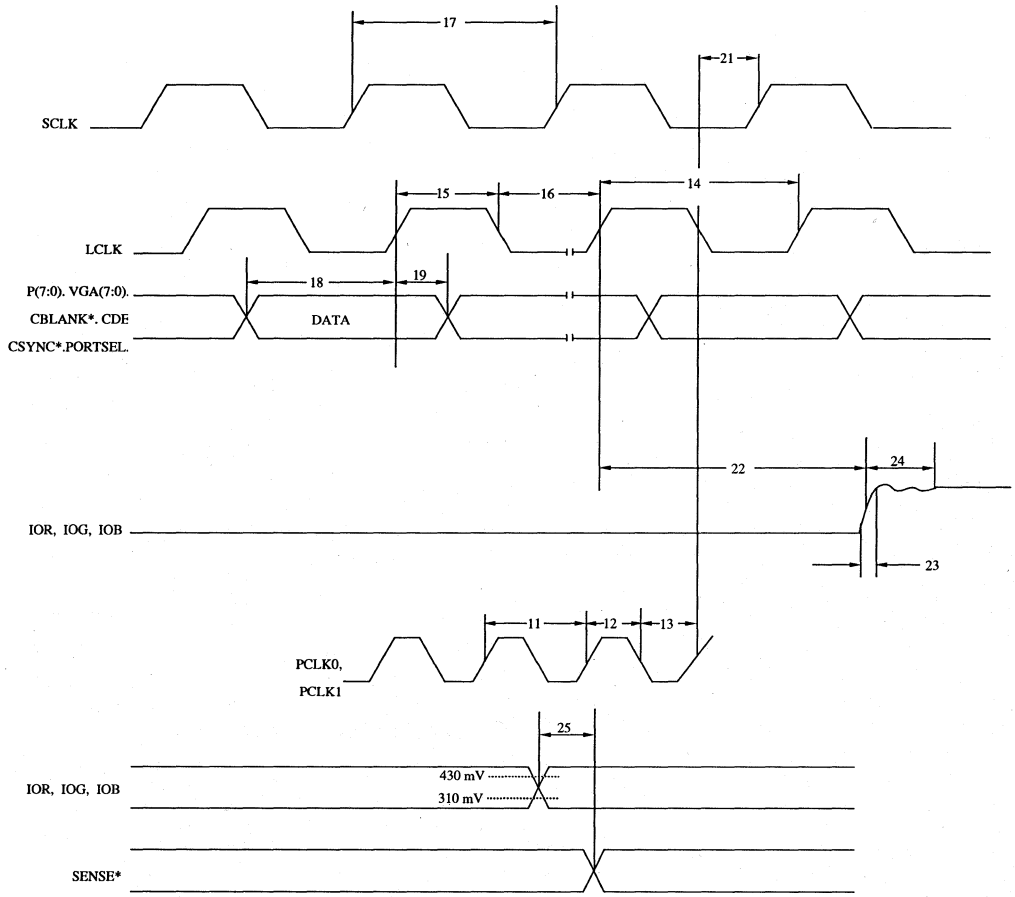
S2 = Second SCLK rising edge

If the pixel data latched by LCLK is to be synchronized correctly with the internal PCLK clock, an LCLK rising edge cannot occur in an invalid window as illustrated above.

If L occurs within the 11 ns invalid region (X), it is not guaranteed on which rising edge of SCLK (S1 or S2) the data will be synchronized. If L occurs before the 11 ns invalid region (X), then the data is guaranteed to be synchronized on S1. If L occurs after the 11 ns invalid region (X), then the data will not be synchronized on S1 and is guaranteed to be synchronized on S2.

Figure 9 (continued). Video Input/Output Timing (Non-1:1).

Timing Waveforms *(continued)*



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 10. Video Input/Output Timing (1:1 MUX Rates).

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt484KPJ85	85 MHz	84-pin Plastic J-Lead	0° to +70°C
Bt484KPJ75	75 MHz	84-pin Plastic J-Lead	0° to +70°C

Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt485

135 MHz Monolithic CMOS True-Color RAMDAC™

4

Distinguishing Features

- 135, 110, 85, 75 MHz Pipelined Operation
- 8:1, 4:1, 2:1, 1:1 Multiplexed Pixel Ports
- Separate 8-bit VGA Port
- 2-Times-Clock Multiplier
- 64 x 64 x 2 Programmable Cursor
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 3 x 8 Cursor Color Palettes
- Optional Sync on All Three Channels
- 0 or 7.5 IRE Blanking Pedestal
- Voltage Reference
- Analog Output Comparators
- Antisparkle Circuitry
- Power-Down Mode
- VRAM Shift Clock
- VGA Support in a True-Color Window
- 84-pin PLCC Package

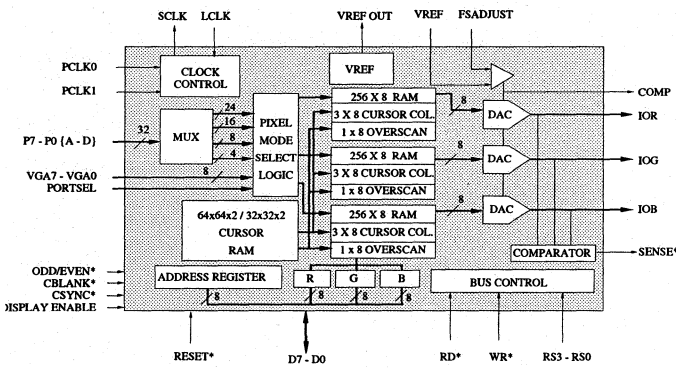
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt484

Functional Block Diagram



Product Description

The Bt485 RAMDAC is designed specifically for high-performance color graphics. The Bt485 is pin-compatible and functionally backwards- compatible to the Bt484.

Included are four byte-wide pixel input ports (multiplexed 4:1), three 256 x 8 color lookup tables with triple 8-bit video D/A converters (configurable for either 6-bit or 8-bit D/A converter operation), and a programmable 64 x 64 x 2 cursor with its own color palette.

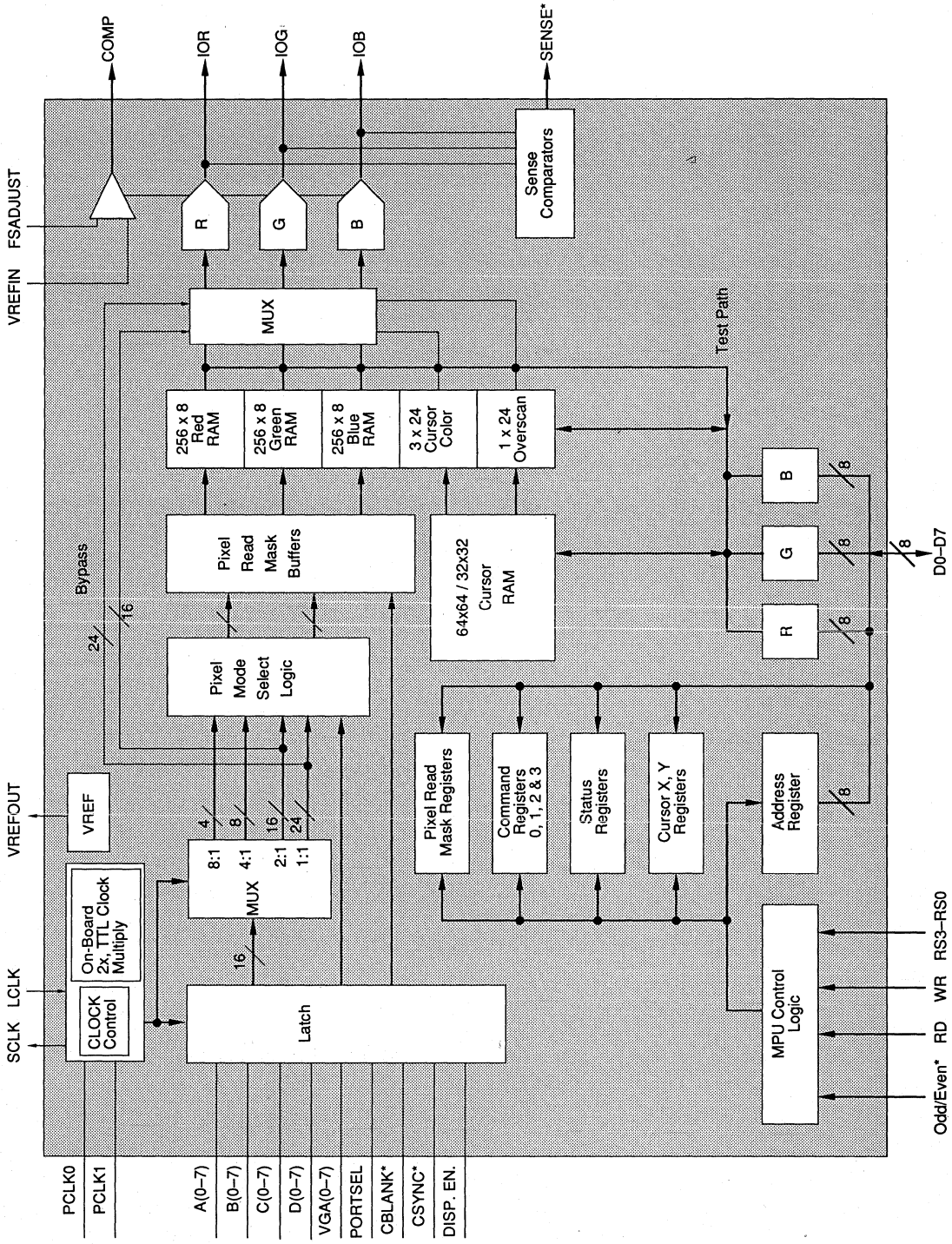
The Bt485 may alternately be configured for a lower performance VGA mode, where 8 bits of VGA pixel data (from a VGA controller) are input through a separate VGA pixel port.

Several operational modes are supported by the 32 pins allocated for the P7:P0 port including 8-bit pseudo color, 16- and 24-bit true color, and various packed and sparse pixel formats. The color palette may be bypassed in any of the true-color modes.

The Bt485 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load.

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L485001 Rev. A

Brooktree®



Bt485 Detailed Block Diagram.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, a standard MPU bus interface is supported, giving the MPU direct access to the color palette RAM. MPU data is transferred into and out of the RAMDAC with the D0–D7 data pins. The read/write timing is controlled by the RD* and WR* inputs.

The RS0–RS3 select inputs specify which control register the MPU is accessing, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers. D0 corresponds to ADDR0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written. The Timing Waveforms section contains further information.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Cursor and Overscan Color Data

To write cursor color data, the MPU writes the address register (cursor color write mode) with the address of the cursor color location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the cursor color registers. After the blue write cycle, the 3 bytes of red, green, and blue color information are concatenated into a 24-bit word and written to the cursor color location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

RS3–RS0	Access	Addressed by MPU
0000	R/W	address register; palette/cursor RAM write
0001	R/W	6/8-bit color palette data
0010	R/W	pixel mask register
0011	R/W	address register; palette/cursor RAM read
0100	R/W	address register; cursor/overscan color write
0101	R/W	cursor overscan and color data
0110	R/W	command register 0
0111	R/W	address register; cursor/overscan color read
1000	R/W	command register 1
1001	R/W	command register 2
1010	read only	status register
1011	R/W	cursor RAM array data
1100	R/W	cursor x-low register
1101	R/W	cursor x-high register
1110	R/W	cursor y-low register
1111	R/W	cursor y-high register

Table 1. Control Input Truth Table (RS3 = MSB and RS0 = LSB).

Circuit Description *(continued)*

CR31 (A9)	ADDR 0–7 (counts binary)	ADDRa,b (counts modulo 3)	RS3	RS2	RS1	RS0	Addressed by MPU
N/A	$00–$FF	00	0	0	0	1	color palette RAM (red component)
		01	0	0	0	1	color palette RAM (green component)
		10	0	0	0	1	color palette RAM (blue component)
N/A	xxxx xx00	00	0	1	0	1	overscan color (red component)
		01	0	1	0	1	overscan color (green component)
		10	0	1	0	1	overscan color (blue component)
N/A	xxxx xx01	00	0	1	0	1	cursor color 1 red component
		01	0	1	0	1	cursor color 1 green component
		10	0	1	0	1	cursor color 1 blue component
N/A	xxxx xx10	00	0	1	0	1	cursor color 2 red component
		01	0	1	0	1	cursor color 2 green component
		10	0	1	0	1	cursor color 2 blue component
N/A	xxxx xx11	00	0	1	0	1	cursor color 3 red component
		01	0	1	0	1	cursor color 3 green component
		10	0	1	0	1	cursor color 3 blue component
N/A	$00–$7F	N/A	1	0	1	1	cursor RAM array, plane 0 (32 x 32 x 2 cursor only)
N/A	$80–$FF	N/A	1	0	1	1	cursor RAM array, plane 1 (32 x 32 x 2 cursor only)
0	$000–$1FF	N/A					cursor RAM array, plane 0 (64 x 64 x 2 cursor only)
1	$200–$3FF	N/A					cursor RAM array, plane 1 (64 x 64 x 2 cursor only)

When the cursor color register or overscan register is addressed, the 6 MSBs of the address register are don't-care conditions. Therefore, when the address register is read and the previous access was to the cursor color registers or overscan register, address register bits [7–2] are returned as either ones or zeros.

Table 2. Address Register Operation and Auto-Incrementing.

Reading Cursor Color Data

To read cursor color data, the MPU loads the address register (cursor color read mode) with the address of the cursor color location to be read. The contents of the cursor color register at the specified address are copied into the RGB registers, and the address register is incremented to the next cursor color location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the cursor color registers. Following the blue read cycle, the contents of the cursor color location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB registers and lookup table RAMs occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three. They are reset to

zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Accessing the Cursor RAM Array

The 32 x 32 x 2 cursor RAM is accessed in a planar format. In the planar format only 7 address bits are used. The eighth bit determines which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 7.

After each access in the planar format, the address increments. The MPU uses ADDR, a binary address counter, to access the cursor RAM array (see Table 2). ADDR is the same binary counter used for RGB auto-incrementing. Any write to ADDR after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the ADDR does not reset the cursor, auto-incrementing logic. The color palette RAM and the cursor RAM share the same external address register, and MPU addressing for this and all other registers is determined by the external register select lines RS3–RS0 (see Table 1).

The 64 x 64 x 2 cursor RAM is accessed in a planar format. The larger cursor RAM can be accessed after bit CR32 in Command Register 3 has been set to a logical one. Bits CR30 and CR31 in Command Register 3 become the load inputs to the 2 MSBs of a 10-bit address counter; therefore, these bits must be written in Command Register 3 before the lower 8 bits are written to the address counter through the MPU port. In the planar format, only 9 address bits are used. The tenth bit is to determine which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 9.

After each access in the planar format, the address increments. The MPU uses ADDR, a 10-bit binary address counter, to access the cursor RAM array. The address counter is the same 8-bit binary counter used for RGB auto-incrementing with CR30 and CR31 as its extended MSBs. Any write to the address counter after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the address counter does not reset the cursor, auto-incrementing logic. The color palette RAM and the cursor RAM share the same external address register, and MPU addressing for this and all other registers is determined by the external register select lines RS3–RS0 (see Table 1).

6-Bit / 8-Bit Operation

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are logical zeros.

Accessing the cursor RAM array does not depend on the resolution of the DACs.

In the 6-bit mode, the Bt485's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Power-Down Mode

The Bt485 incorporates a power-down capability, controlled by command bit CR00. While command bit CR00 is a logical zero, the Bt485 functions normally.

While command bit CR00 is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the MPU may read or write to the RAM while the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. The DACs output no current, and the three command registers may still be written to or read by the MPU. The output DACs require about 1 second to turn off (sleep mode) or turn on (normal), depending on the compensation capacitor used (see Video Generation for further information).

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

Frame Buffer Clocking

The video DRAM shift clock (SCLK) is generated by the Bt485. SCLK is one eigth, one fourth, or one half the pixel clock rate, depending on whether multiplexing is 8:1, 4:1, or 2:1, respectively. In the 1:1/VGA mode, SCLK = LCLK.

P0–P7 (A–D) are pixel data, 8 bits per pixel (4:1 MUX) and 4 bits per pixel (8:1 MUX) for 4 and 8 horizontally consecutive output pixels. P0–P7 (A–D) are always latched on the rising edge of LCLK.

The pixel clock is specified to be either PCLK 0 or PCLK 1 by command bit CR24.

Onboard 2x TTL Clock Multiplier

The Bt485 provides an onboard 2x TTL clock multiplier for high-speed operations. The clock multiplier can be

enabled or disabled by programming bit CR33 in Command Register 3 (see Accessing Command Register 3 in the Internal Registers section). Upon applying a RESET signal, the clock multiplier is disabled until bit CR33 is written to a logical one. Either PCLOCK0 or PCLOCK1 can be doubled internally. For operations above 90 MHz, the clock doubler is recommended.

The clock multiplier can lower system costs by eliminating expensive ECL crystals and clock synthesizers. It can also improve system design by eliminating conversion logic.

Frame Buffer Pixel Port Interface

There are four 8-bit pixel ports, (A–D), used to interface to the frame buffer memory.

Video input data ports A through D are designated in this manner to represent the order of pixel data presentation: Port A always corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by B, then C, and finally D, repeating the pattern ABCD, ABCD, until the first scan line is completely displayed.

For the cursor display, the output sequence depends on the CR23 command bit and the ODD/EVEN* input. For example, when either interlaced or noninterlaced operation is selected, the current field is displayed.

Scan line 1 is always displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 2 immediately follows scan line 1. In the interlaced mode, scan line 2 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed and the ODD/EVEN pin has been toggled.

Only the ODD lines or only the EVEN lines will be displayed, if the ODD/EVEN does not change.

Figure 1 shows the interlaced and noninterlaced display scan. Noninterlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

Pixel Read Mask Register

Each pixel clock cycle, P0–P7 pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true color bypass is enabled. The pixel mask register is not initialized at the power-up/reset and should be initialized by the user to logical ones for proper operation.

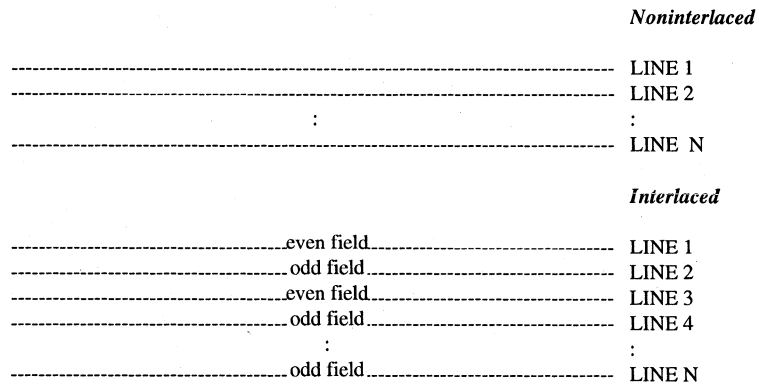


Figure 1. Interlaced/Noninterlaced Display Operation.

Circuit Description *(continued)*

Modes of Operation

4-Bits/Pixel Operation (8:1 MUX)

The 32 input bits are multiplexed 8:1 and are configured for 4 bits/pixel. There are eight independent 4-bit pixel ports, P7:4 (A–D) and P3:0 (A–D). The pixel bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every eight PCLK cycles. SCLK will equal the PCLK selected, divided by 8. The 4 bits from each port will select 1 of 16 locations (RAM address 0–15) in the palette in the order presented in Table 3.

8-Bits/Pixel Operation (4:1 MUX)

The 32 input bits are multiplexed 4:1 and are configured for 8 bits/pixel. There are four independent 8-bit pixel ports, (A–D). The pixel bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every four PCLK cycles. SCLK will be equal to the PCLK selected, divided by 4. The 8 bits from each port will select 1 of 256 locations in the palette as presented in Table 3.

16-Bits/Pixel Operation (2:1 MUX)

The 32 input bits are multiplexed 2:1 and are configured for 16 bits/pixel. Multiplexing of 2:1 is selected through bit CR12 in Command Register 1. There are two independent 16-bit pixel ports, (B–A) and (D–C). The bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every two PCLK cycles. SCLK will be equal to the PCLK selected, divided by 2. The pixel bits multiplexed in this mode are from the same ports of RGB color formats of 5:5:5 or 5:6:5. P7D and P7B are ignored internally when the 5:5:5 color format is selected (see Table 3).

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the most significant bits of the respective palette address; the least significant bits are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the least significant bits of the respective palette address; the most significant bits are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors. The DACs can be configured for 6 or 8 bits of resolution in this mode.

16-Bits/Pixel Operation (1:1 MUX)

The 1:1 multiplexing mode is selected through CR12 in Command Register 1. When this mode is selected, two independent 16-bit pixel ports, (B–A) and (D–C), are latched on the rising edge of LCLK and are multiplexed 1:1. Selection between the two ports is made by bit CR10 in Command Register 1. One rising edge of LCLK should occur every PCLK cycle. SCLK is equal to the PCLK selected.

Bit P7D switches between the two ports on a pixel-by-pixel basis when 5:5:5 RGB color format (bit CR13 in Command Register 1) and real-time pixel port switching is enabled (bit CR11 in Command Register 1). If PORTSEL is a logical zero, the VGA port is multiplexed regardless of the state of P7D. Bit P7B is ignored internally when in 5:5:5 mode. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

Bits P7B and P7D are ignored internally if 5:5:5 RGB color format is selected and real-time pixel port switching is disabled. Programming bit CR10 in Command Register 1 determines switching for both 5:5:5 and 5:6:5 RGB color formats.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the most significant bits of the respective palette address; the least significant bits are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the least significant bits of the respective palette address; the most significant bits are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors. The DACs can be configured for 6 or 8 bits of resolution in this mode.

24-Bits/Pixel Operation (1:1 MUX)

When 24 bits/pixel is selected, there is one 24-bit pixel port. The pixel bits, P7:0 (C–A), are latched on the rising edge of LCLK and are multiplexed 1:1. One rising edge of LCLK should occur every PCLK cycle. SCLK is equal to the PCLK selected. The RGB color format in this mode is 8:8:8.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as

Circuit Description *(continued)*

PORTSEL	CR11	CR10	P7D	CR12	CR13	CR16	CR15	Ports MUXed	MUX Rate	Operating Modes
0	x	x	x	x	x	x	x	VGA(7:0)	1:1	VGA
1	x	x	Data	x	x	1	1	P7:4(A) P3:0(A) P7:4(B) P3:0(B) P7:4(C) P3:0(C) P7:4(D) P3:0(D)	8:1	4 Bits/Pixel
1	x	x	Data	x	x	1	0	P7:0(A) P7:0(B) P7:0(C) P7:0(D)	4:1	8 Bits/Pixel
1	x	x	x	0	0	0	1	P7:0(B-A) P7:0(D-C)	2:1	16 Bits/Pixel (5:5:5) (see Table 4)
1	x	x	Data	0	1	0	1	P7:0(B-A) P7:0(D-C)	2:1	16 Bits/Pixel (5:6:5) (see Table 5)
1	0	0	x	1	0	0	1	P7:0(B-A)	1:1	16 Bits/Pixel (5:5:5)
1	0	1	x	1	0	0	1	P7:0(D-C)	1:1	16 Bits/Pixel (5:5:5)
1	1	x	0	1	0	0	1	P7:0(B-A)	1:1	16 Bits/Pixel (5:5:5) (see Table 4)
1	1	x	1	1	0	0	1	P7:0(D-C)	1:1	16 Bits/Pixel (5:5:5) (see Table 4)
1	x	0	x	1	1	0	1	P7:0(B-A)	1:1	16 Bits/Pixel (5:6:5) (see Table 5)
1	x	1	Data	1	1	0	1	P7:0(D-C)	1:1	16 Bits/Pixel (5:6:5) (see Table 5)
1	x	x	x	x	x	0	0	P7:0(C-A)	1:1	24 Bits/Pixel (see Table 6)

Table 3. Modes of Operation (Pixel Port Configuration).

Circuit Description *(continued)*

Bit	MSB															LSB
Format	S	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B
Port 1	S	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	S	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

If bit CR11 in Command Register 1 is a logical zero, then S=CR10 bit, 16-bit/pixel port switch control (1:1 multiplexing, CR12 = 1). If bit CR11 in Command Register 1 is a logical one, then S=P7D bit, real-time pixel port switch (1:1 multiplexing, CR12 = 1).

Table 4. 5:5:5 RGB Color Format for Both 2:1 and 1:1 Multiplexing Modes.

Bit	MSB															LSB
Format	R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B
Port 1	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	P7D	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

Table 5. 5:6:5 RGB Color Format for Both 2:1 and 1:1 Multiplexing Modes.

Bit	MSB																						LSB
Format	R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B
Port	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A

Note: P7:0(D) are ignored.

Table 6. 24-Bits/Pixel RGB Color Format.

well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When 8:8:8 color format is selected, the display can contain 16.8 million simultaneous colors. The DACs should be configured for 8 bits of resolution in this mode (CR14=1 and CR01=1).

VGA Port

An 8-bit pixel port is provided to support VGA pixel data. The data is latched on the rising edge of LCLK. One rising edge of LCLK should occur every PCLK cycle. SCLK will equal the PCLK selected. A logical zero on the PORTSEL pin ensures that the VGA port is selected. A logical one on the PORTSEL pin selects the pixel port. To use the VGA PORTSEL feature the RAMDAC *must* be configured in the 1:1 multiplexing mode through the RAM (CR14 = 0) or pallette bypass (CR14 = 1). After the RAMDAC has been properly configured, the VGA PORTSEL can then be used to select between the pixel port and the VGA port on a pixel-by-pixel basis. The PORTSEL pin can also be used to switch between VGA and the pixel ports in 2:1, 4:1, or 8:1 MUX modes on a frame-by-frame basis. The VGA pixels address the color palette when selected. Only PCLK0 should be used when switching between the VGA and pixel ports on a pixel-by-pixel basis. PCKL1 should be used when switching between the VGA and pixel ports on a frame-by-frame basis. The 8-bit VGA data forms a common index into the palette, selecting 1 of 256 colors. Valid data begins at address zero.

Pixel Read Mask Register

The pixel data has can be masked with the 8-bit pixel read mask register before being transferred to the color palette. The pixel data is bit-wise logically ANDed with the

	MSB							LSB	
Pixel Mask Register	7	6	5	4	3	2	1	0	Register Bits
VGA Data	7	6	5	4	3	2	1	0	Palette Index
4 Bits/Pixel	x	x	x	x	3	2	1	0	Palette Index
8 Bits/Pixel	7	6	5	4	3	2	1	0	Palette Index
16 Bits/Pixel	7	6	5	4	3	x	x	x	Red Palette Index
5:5:5 Format	7	6	5	4	3	x	x	x	Green Palette Index
SPARSE	7	6	5	4	3	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	4	3	2	1	0	Red Palette Index
5:5:5 Format	x	x	x	4	3	2	1	0	Green Palette Index
CONTIGUOUS	x	x	x	4	3	2	1	0	Blue Palette Index
16 Bits/Pixel	7	6	5	4	3	x	x	x	Red Palette Index
5:6:5 Format	7	6	5	4	3	2	x	x	Green Palette Index
SPARSE	7	6	5	4	3	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	4	3	2	1	0	Red Palette Index
5:6:5 Format	x	x	5	4	3	2	1	0	Green Palette Index
CONTIGUOUS	x	x	x	4	3	2	1	0	Blue Palette Index
24 Bits/Pixel	7	6	5	4	3	2	1	0	Red Palette Index
8:8:8 Format	7	6	5	4	3	2	1	0	Green Palette Index
	7	6	5	4	3	2	1	0	Blue Palette Index

Table 7. Pixel Index Masking.

contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true-color bypass is enabled. The pixel read mask register is not initialized at the power-up/reset and must be initialized by the user to logical ones for proper operation (see Table 7).

Cursor Operation

The Bt485 has an on-chip, three-color, 64 x 64 x 2 pixel user-definable cursor. A 32 x 32 x 2 pixel user-defineable cursor can also be selected by writing bit CR32 in Command Register 3. This cursor can be used with both interlaced and noninterlaced systems.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor position register (Xp,Yp) (see Figure 2). A (0,0) written to the cursor position registers will place the cursor off the screen. A (1,1) written to the cursor position registers will place the lower right pixel of the cursor on the upper left corner of the screen. Only one cursor pattern per frame is displayed at the location specified for both interlaced and noninterlaced display formats, regardless of the number of updates to (Xp,Yp). The cursor's vertical or horizontal location is not affected during any frame displayed. There are no restrictions on updating (Xp, Yp) other than both cursor position registers must be written when the cursor location is updated. Internal x-and y-position registers are loaded after the upper byte of Yp has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written.

Cursor positioning is relative to CDE. The cursor position is not dependent upon CBLANK* (see Figure 2). The reference point of the cursor (row 0, column 0) is in the lower right corner. The cursor Xp position is relative to the first rising edge of LCLK when CDE is sampled at logical one. The cursor Yp position is relative to the first rising edge of LCLK when CDE is sampled at logical one after the CDE vertical blanking interval has been determined (see Figure 2). If a CDE transition from logical zero to logical one (as determined by LCLK) does not occur within 2048 PCLKs (2048 LCLKs when in 1:1 MUX mode), CDE is in vertical blanking. In 8:1, 4:1, or 2:1 MUX modes, cursor timing is based on the PCLK selected. When the MUX rate is 1:1, cursor timing is based on LCLK.

The 64 x 64 x 2 cursor pattern can be displayed in an interlaced system if bit CR23 in Command Register 2 is a logical one. If Yp is greater than 64 ($0040), and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the ODD/EVEN* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field,

Circuit Description *(continued)*

and the data in row 63 of the cursor RAM will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, then the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 63 of the cursor RAM will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 64 ($0040), cursor display does not depend on whether Yp is odd or even. If the ODD/EVEN* pin is a logical zero, the first line of the cursor is displayed on scan line 1. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field will correspond to subsequent scan lines in the even field. If the ODD/EVEN* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line 2. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

The cursor pattern can be displayed in an interlaced system if bit CR23 in Command Register 2 is a logical one. If Yp is greater than 32 ($0020), and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the ODD/EVEN* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field, and the data in row 31 of the cursor RAM array will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, then the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 31 of the cursor RAM array will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 32 ($0020), cursor display does not depend on whether Yp is odd or even. If the ODD/EVEN* pin is a logical zero, the first line of the cursor is displayed on scan line 1. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field will correspond to subsequent scan lines in the even field. If the ODD/EVEN* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line 2. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

If bit CR23 is a logical zero, the cursor must be

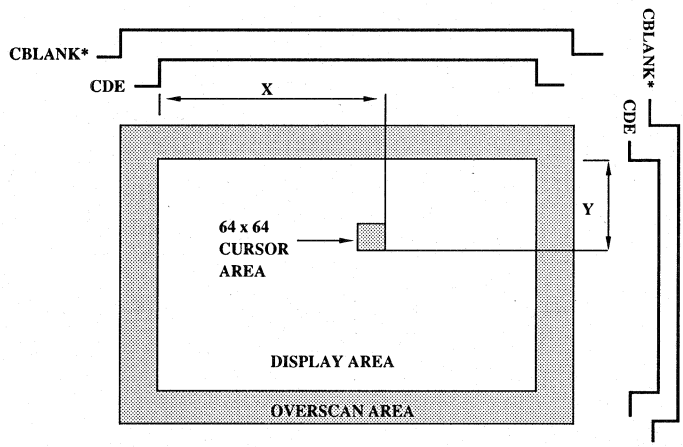


Figure 2. Cursor Positioning.

displayed in a noninterlaced system. Scan lines displayed in a frame correspond to sequential cursor lines in the cursor RAM relative to the first active cursor line in the frame.

Figure 3 is a visual explanation of planar pixel format and cursor RAM array pixel mapping.

Cursor Color Support

The cursor has three modes for color selection. Bits CR21 and CR20 in Command Register 2 determine which cursor mode is to be used. Mode 1 is a three-color cursor, mode 2 is referred to as a PM/Window cursor, and mode 3 is referred to as an X-Windows cursor (see Table 8).

Highlight Logic

The highlight logic is enabled in cursor mode 2 when both plane data (plane 1 and plane 0) are logical ones (see Table 8). When the highlight logic is enabled, it ensures that the pixel highlighted has a unique color. This is because the highlight logic bit-wise complements the 24- or 18-bit palette or bypass data supplied to the DACs.

Video Generation

The CSYNC* and CBLANK* inputs are latched on the rising edge of LCLK to maintain synchronization with the color data. They add appropriately weighted currents to the analog outputs and produce the specific output levels required for video applications, as illustrated in Figures 4 and 5. Tables 9 and 10 detail how the CSYNC* and BLANK* inputs modify the output levels.

The CR05 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command bits CR02, CR03, and CR04 specify whether the RGB outputs contain sync information.

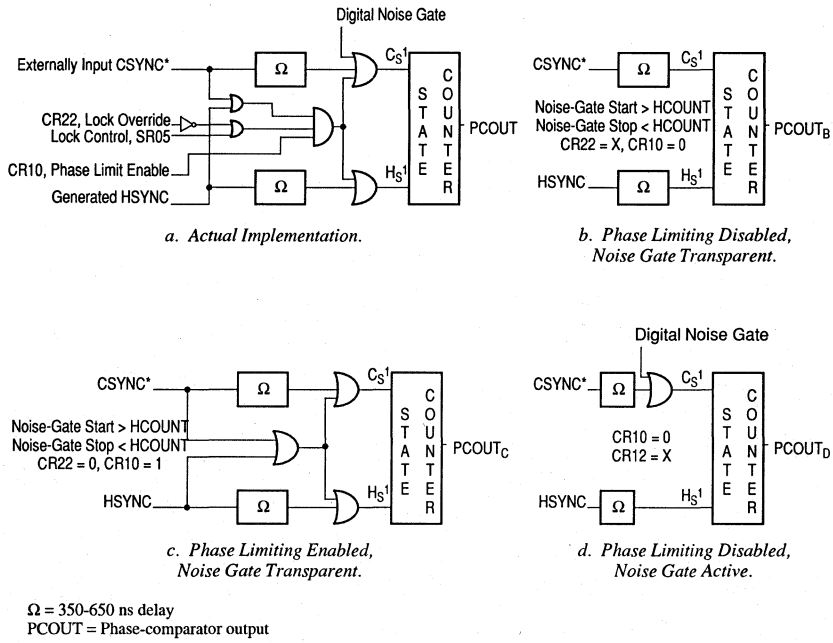
SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, or IOB outputs have exceeded the internal voltage reference level of the SENSE* comparator circuit. This output is used to determine the presence of a CRT monitor, and, with diagnostic code, the difference between a loaded or an unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For the proper operation of the SENSE circuit, the following levels should be applied to the comparator by the IOR, IOG, and IOG outputs:

DAC Low Voltage ≤ 260 mV (Note 1)
DAC High Voltage ≥ 410 mV (Note 1)

Note 1: SENSE values are subject to change upon completion of characterization.

There is an additional ±10-percent tolerance on the above levels when the internal voltage reference is used. If SYNC* is logical zero, SENSE* is stable. The SENSE* output can drive only one CMOS load.



a. Actual Implementation.

b. Phase Limiting Disabled, Noise Gate Transparent.

c. Phase Limiting Enabled, Noise Gate Transparent.

d. Phase Limiting Disabled, Noise Gate Active.

Ω = 350-650 ns delay
PCOUT = Phase-comparator output

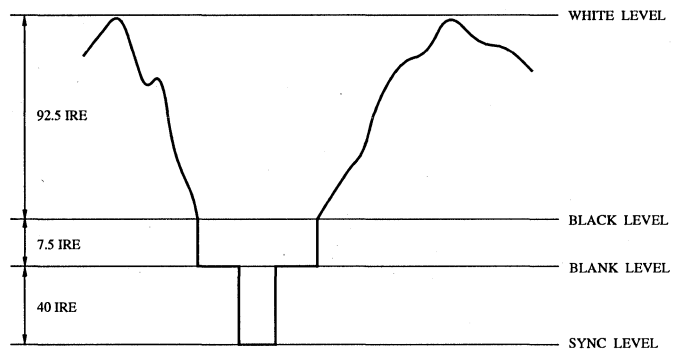
Figure 3. Planar Pixel Format and Cursor RAM Array Pixel Mapping for Both 32 x 32 and 64 x 64 Cursors.

Plane 1	Plane 0	MODE 1	MODE 2	MODE 3
0	0	Palette Data	Cursor Color 1	Palette Data
0	1	Cursor Color 1	Cursor Color 2	Palette Data
1	0	Cursor Color 2	Palette Data	Cursor Color 1
1	1	Cursor Color 3	Palette Data Complement	Cursor Color 2

Table 8. Overlay Color Modes.

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET ~ 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 7.5 IRE).

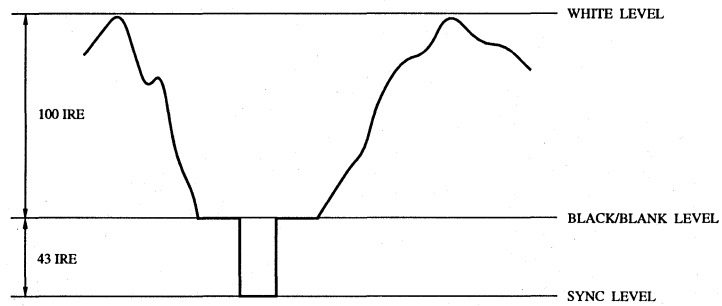
Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET ~ 147 Ω.

Table 9. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET ~ 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 5. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET~ 147 Ω.

Table 10. Video Output Truth Table (SETUP = 0 IRE).

Command Register 0 (RS value = 0110)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR00 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zeros when a low signal is asserted on the RESET* pin.

CR07	(0) Command Register 3 Cannot be Addressed (1) Command Register 3 Can be Addressed	A logical one written to this bit allows the user to indirectly access Command Register 3.
CR06	Clock Disable ANDed with CR00 (0) Normal Operation (1) Disable Internal Clocking	When this bit *and* CR00 are a logical one, the internal clock and SCLK are disabled to further conserve power when in power-down mode. The RAM still retains the data, and MPU reads and writes can occur without loss of data. When this bit is a logical zero, internal clocking is enabled and SCLK will be generated.
CR05	Setup Enable (0) Disable SETUP (0 IRE) (1) Enable SETUP (7.5 IRE)	This bit determines the video blanking pedestal. A logical zero sets a 0 IRE blanking pedestal, and a logical one sets 7.5 IRE.
CR04 CR03 CR02	Blue Sync Enable Green Sync Enable Red Sync Enable (0) Disable Sync (1) Enable Sync	These bits specify whether the respective IOB, IOG, or IOR outputs are to contain sync information.
CR01	DAC 6/8-Bit Resolution (0) 6-bit Operation (1) 8-bit Operation	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle.
CR00	Power-Down Enable (0) Normal Operation (1) Power-Down Operation	While this bit is a logical zero, the device operates normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data, and CPU reads and writes can occur with no loss of data. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used.

Internal Registers *(continued)*

Command Register 1 (RS value = 1000)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR10 corresponds to data bus bit D0, the least significant data bit (see Table 7). All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR17	Reserved (logical zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR16, 15	Bit/Pixel Select (00) One 24-Bit Pixel (01) One or Two 16-Bit Pixels (10) Four 8-Bit Pixels (11) Eight 4-Bit Pixels	These bits select the pixel size depth and determine the multiplexing rates for 4-, 8-, and 24-bit/pixel operation. The 16-bit/pixel multiplexing rate is set by the state of CR12.
CR14	True-Color Bypass Enable (0) Pixel Addresses Palette (1) Pixel Bypasses Palette	When this bit is a logical zero, the pixel palette is addressed by the pixel data. When this bit is a logical one, the RGB pixel data bypasses the color palette and drive the DACs directly. True-color bypassing is available only for pixel sizes of 16 and 24 bits.
CR13	16-Bit RGB Color Format (0) 5:5:5 R:G:B Color Format (1) 5:6:5 R:G:B Color Format	This bit selects the RGB color format for 16-bit/pixel operation.
CR12	16-Bit Multiplexing Rate (0) 2:1 Multiplexing (1) 1:1 Multiplexing	When this bit is a logical zero and CR16 and 15 are set to 01, two 16-bit values are latched in during every LCLK cycle. When this bit is a logical one and CR16 and 15 are set to 01, one 16-bit value is output during every LCLK cycle. This bit is ignored if CR16/CR15 specify 4-, 8-, or 24-bit/pixel operation.
CR11	16-Bit Real-Time Switch Enable (0) CR10 Controls Selection (1) P7D Controls Selection	This bit is only valid when CR13 = 0 (5:5:5 format) and CR12 = 1 (1:1 multiplexing) are specified. When this bit is a logical zero, CR10 switches the ports multiplexed. When this bit is a logical one, pixel port bit P7D switches the ports multiplexed. This bit is ignored when 5:6:5 RGB color format is selected (when bit CR13 is a logical one).
CR10	16-Bit/Pixel Port Switch Control (0) Multiplex Port [B–A] (1) Multiplex Port [D–C]	This bit specifies which 16-bit word is selected for either 5:5:5 (CR13 = 0) or 5:6:5 (CR13 = 1) modes. In order for this bit to control which 16-bit port is selected, CR12 must be a logical one (16-bit 1:1 multiplexing). This bit is ignored when real-time port switching is enabled (CR11 = 1).

Internal Registers *(continued)*

Command Register 2 (RS value = 1001)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR20 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR27	SCLK Disabled (0) SCLK Enabled (1) SCLK Disabled	A logical zero must be written to this bit to enable SCLK to be output. A logical one written to this bit three-states the SCLK output.
CR26	Test Path Enable (0) Normal Operation (1) Test Path Enabled	When this bit is set to a logical zero, the device operates normally. A logical one enables certain test paths to be internally set up. This involves any input mode and any inputs that affect access to the color palette RAM. When this bit is set to a logical one, the pixel data is accessible on the MPU data bus. While this test mode is enabled, the device will not operate at speed.
CR25	PORTSEL Mask (0) Masked (1) Nonmasked	This bit determines the selection of the input port. It is logically ANDed with the PORTSEL pin. A logical zero selects the VGA port. When this bit is a logical one, the PORTSEL pin selects either the VGA or pixel port.
CR24	CLKSEL Enable (0) PCLK0 Selected (1) PCLK1 Selected	When this bit is a logical zero, PCLK0 is selected. When this bit is a logical one, PCLK1 is selected. To eliminate glitches on the SCLK output, switching between PCLKs should occur only when the multiplexing rate is 8:1 or 4:1. To ensure the integrity of the palette, the device should be put in sleep mode before switching clocks.
CR23	Display Mode Select (0) Noninterlaced (1) Interlaced	When this bit is a logical zero, the display format is noninterlaced. When the bit is a logical one, the display format is interlaced. The mode must be set properly to ensure proper operation of the internal cursor.
CR22	16-Bit/Pixel Palette Index Select (0) Sparse Indexing (1) Contiguous Indexing	When this bit is a logical zero, palette addressing is sparse. The RGB color component pixel data is mapped to the most significant bits of the RGB palette address. The least significant of the palette address bits are set to zero. When this bit is a logical one, palette addressing is contiguous. The RGB color component pixel data is mapped to the least significant bits of the palette address. The most significant bits of the address are set to zero.
CR21, 20	Cursor Mode Select (00) Cursor Disabled (01) Three-Color Cursor (10) Two-Color/Highlight Cursor (11) Two-Color/X-Windows Cursor	These bits determine the functionality of the onboard 64 x 64 x 2 or the 32 x 32 x 2 hardware cursor.

Command Register 3 (RS value = 1010, when bit CR07 in Command Register 0 is set to logical one.)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR30 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR37	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR36	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR35	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR34	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR33	2x Clock Multiplier (0) 2x Clock Multiplier Disabled (1) 2x Clock Multiplier Enabled.	This bit enables or disables the 2x multiplier. A logical one written to this bit enables the 2x on-chip TTL clock multiplier for high-speed operation. A logical zero written to CR33 will disable the clock multiplier and will allow the external clock source to directly drive the logic.
CR32	Cursor Select (0) 32x32x2 Cursor (1) 64x64x2 Cursor	This bit selects either a 64 x 64 or a 32 x 32 hardware cursor. A logical zero written to this bit will select the 32 x 32 cursor size, and a logical one will select the 64 x 64 cursor size.
CR31, 30	MSBs for 10-bit Address Counter CR31 = A9 CR30 = A8	These bits are the load inputs to the 2 MSBs of the 10-bit address counter. The 10-bit address counter can be set to access any particular location in the 64 x 64 x 2 cursor RAM array.

Internal Registers *(continued)*

Pixel Read Mask Register (RS value = 0010)

The 8-bit pixel read mask register may be written to or read by the MPU at any time, and *is not* initialized at power-up. D0 is the least significant bit. The contents of this register are bit-wise ANDed with the pixel data prior to addressing the color palette RAM. The pixel read mask register must be initialized by the user to logical ones for proper operation.

Status Register (RS value = 1010)

The 8-bit status register monitors certain device states and identifies devices. It may be read by the MPU at any time; MPU write cycles to this register are ignored. D0 is the least significant bit corresponding to SR0. This register is not reset during power-up/reset.

SR7–SR6: These bits are identification values. SR7=0 and SR6=1.
SR5–SR4: These bits are revision values.

SR3: This is the SENSE* bit. If it is a logical zero, one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This bit is used to determine the presence of a CRT monitor, and, with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The SENSE reference has an additional ±10-percent tolerance when an internal voltage reference is used.

SR2: (0) Write Cycle
(1) Read Cycle

Read/write access status. This bit provides RD/WR status when the register select bits equal $0, $3, $4, or $7. When address register $0 or $4 has been written, the device is in the write mode and this bit is a logical zero. When address register $3 or $7 has been written, the device is in the read mode and this bit is a logical one.

SR1–SR0: When read, these bits reflect the color component address for the next RD/WR cycle when the palette, cursor color registers, or overscan register are accessed: Address [a,b] state (00) Red Color Component
(01) Green Color Component
(10) Blue Color Component

Accessing Command Register 3

A fourth Command Register, CR3, was added to address the extended functionality of the Bt485 and to remain backwards compatible to the Bt484. Since there are only 4 register select lines (and all 16 combinations have already been used), CR3 must be accessed indirectly.

Command Register 3 is accessed with the following sequence of operations:

1. Set RS3–RS0 = 0110, Command Register 0.
2. Write a logical one to CR07.
3. Set RS3–RS0 = 0000, address register.
4. Write address register to 0000 0001.
5. Set RS3–RS0 = 1010.
6. Read or write Command Register 3.

With this indirect addressing, the status register can be accessed by writing 0000 0000 to the address register, as in step 4. The status register cannot be written to; it can only be read.

When a 64 x 64 x 2 cursor is selected (CR32 = 1), CR31 and CR30 must be written to use a 10-bit counter to address the larger RAM array. CR31 and CR30 become the load inputs to the 2 MSBs of the 10-bit address counter. Therefore, to set this counter to access a particular location in the 64 x 64 x 2 cursor RAM array, these 2 bits must be written to Command Register 3 before the lower 8 bits are written to the address counter through the MPU port. As the 10-bit address counter auto-increments, the new values of this counter can be read back through CR31 and CR30. The contents of this register will be reset with the assertion of the external RESET* pin.

Internal Registers *(continued)*

Cursor (x,y) Registers (RS values: CXLR = 1100, CXHR = 1101, CYLR = 1110, and CYHR = 1111)

These registers are used to specify the (x, y) coordinate of the 64 x 64 x 2 hardware cursor. The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are ignored.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 64 (or $0040)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) register. If Xp is equal to 0, the cursor will be offscreen (see Cursor Operation in the Circuit Description section).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 64 (or $0040)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation).

Cursor (x, y) Registers (RS values: CXLR = 1100, CXHR = 1101, CYLR = 1110, and CYHR = 1111)

These registers are used to specify the (x, y) coordinate of the 32 x 32 x 2 hardware cursor. The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 32 (or $0020)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) register. If Xp is equal to 0, the cursor will be offscreen (see Cursor Operation).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 32 (or $0020)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation).

Pin Descriptions

Pin Name	Pin #	Description
RESET*	47	Reset input (TTL compatible). When this signal is low, all the command register bits are set to zero, and the device is in VGA mode. The pixel read mask register is not initialized on reset and must be initialized by the user to logical ones for proper operation (see Pixel Read Mask Register in the Circuit Description section).
CBLANK*	65	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 9 and 10. CBLANK* is latched on the rising edge of LCLK. When BLANK* is a logical zero, the pixel inputs are ignored. The falling edge of this signal determines the polarity of the CSYNC* input pin. The onboard cursor positioning counters are referenced to this signal.
CSYNC*	64	Composite sync control input (TTL compatible). The polarity of this pin is determined on the last rising LCLK edge before the falling edge of CBLANK*. CSYNC* does not override any other control or data input, as shown in Tables 9 and 10; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LCLK. Bits CR04–CR02 in Command Register 0 can permanently disable sync on the IOR, IOG, or IOB output.
CDE	63	Composite display enable control input (TTL compatible). The state of this signal and CBLANK* determines whether the analog outputs are blanked or contain cursor color, pixel , or overscan data. This signal is latched on the rising edge of LCLK. If overscanning is not used, this pin should be tied to CBLANK*. The following is a list of combinations of CDE and CBLANK*: PORTSEL CDE CLBANK* x x 0 Video Blanking 0 0 1 VGA Pixel Data 0 1 1 Cursor Color or VGA Data 1 0 1 Overscan Data 1 1 1 Cursor Color or Pixel Data
ODD / EVEN*	62	Odd/even field input (TTL compatible). This signal should be changed only during vertical blank. This input is used to ensure proper operation of the onboard cursor when interlaced operation (command bit CR23=1) is selected. When this signal is a logical zero, an even field is specified. When this signal is a logical one, an odd field is specified. This input is ignored if noninterlaced operation (command bit CR23=0) is selected.
PCLK0	78	Pixel Clock 0 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical zero. The signal on this pin should be the VGA pixel clock. This clock should be specified when switching between the pixel and VGA ports on a pixel-by-pixel basis (in 1:1 mode, only). It is recommended that all clock inputs be driven by a dedicated buffer to avoid reflection-induced jitter.
PCLK1	76	Pixel Clock 1 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical one. The signal on this pin is typically the high-speed pixel clock used during multiplexed operation of the pixel port.
SCLK	83	VRAM shift clock output (TTL compatible). The signal on this pin is equal to the selected pixel clock divided by 8, 4, 2, or 1, depending on the operating mode selected. If 2x clock multiplier is selected (CR33 = 1), then the SCLK output is equal to pixel clock divided by 4, 2, or 1, or pixel clock multiplied by 2, in 8:1, 4:1, 2:1, or 1:1 modes, respectively.

Pin Descriptions *(continued)*

Pin Name	Pin #	Description
LCLK	81	Latch Clock input (TTL compatible). The rising edge of this signal latches P7:0 (A–D) or VGA [7:0], and CBLANK*, CDE, CSYNC*, and PORTSEL. The information latched by this signal is synchronized internally with SCLK. Because of this synchronization process, there is a timing window on both sides of SCLK where LCLK must not rise (see AC Characteristics section). This timing window is necessary so that data latched by LCLK does not interfere with the setup and hold times required by the internal synchronizing latch. Data is synchronized with the selected pixel clock after being internally latched with SCLK. When the multiplexing rate is 8:1, 4:1, 2:1, or 1:1, this signal is equal to the selected pixel clock divided by 8, 4, 2, or 1, respectively.
P7:0 (A–D)	1–32	Pixel port inputs (TTL compatible). This port is selected if PORTSEL is a logical one and PORTSEL is not masked by CR25. The appropriate pins on this port are multiplexed at rates of either 1:1, 2:1, 4:1, or 8:1, depending on the operating mode selected. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
VGA[7:0]	67–74	VGA port inputs (TTL compatible). This port is selected if PORTSEL is a logical zero. This port is multiplexed 1:1. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
PORTSEL	66	VGA/pixel port select input (TTL compatible). This pin is ANDed with control register bit CR25 to determine whether the pixel port or VGA port is selected. A logical zero on this pin selects the VGA port regardless of the state of CR25. A logical one selects the pixel port if CR25 = 1. This pin may be used in 1:1 mode to switch between the pixel and VGA ports on a pixel-by-pixel basis. This pin may also be used to switch between the VGA and pixel ports in 2:1, 4:1, or 8:1 MUX modes on a frame-by-frame basis. This pin should not be left floating.
WR*	48	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS3 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	49	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS3 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0–RS3	50–53	Register select inputs (TTL compatible). RS0–RS3 specify the type of read or write operation being performed, as shown in Tables 1 and 2.
D0–D7	54–61	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
SENSE*	46	Comparator sense output (CMOS compatible). This pin will be low if one or more of the IOR, IOG, and IOB analog output levels exceed the internal comparator reference levels. The sense output can drive only one CMOS load.
IOR, IOG, IOB	35, 37, 39	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Description</th></tr>
<tr><td>FSADJUST</td><td>33</td><td>Full-scale adjust control. The IRE relationships in Figures 4 and 5 are maintained, regardless of the full-scale output current.

When an external or the internal voltage reference (Figures 6 and 7 in the PC Board Layout Considerations section) is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

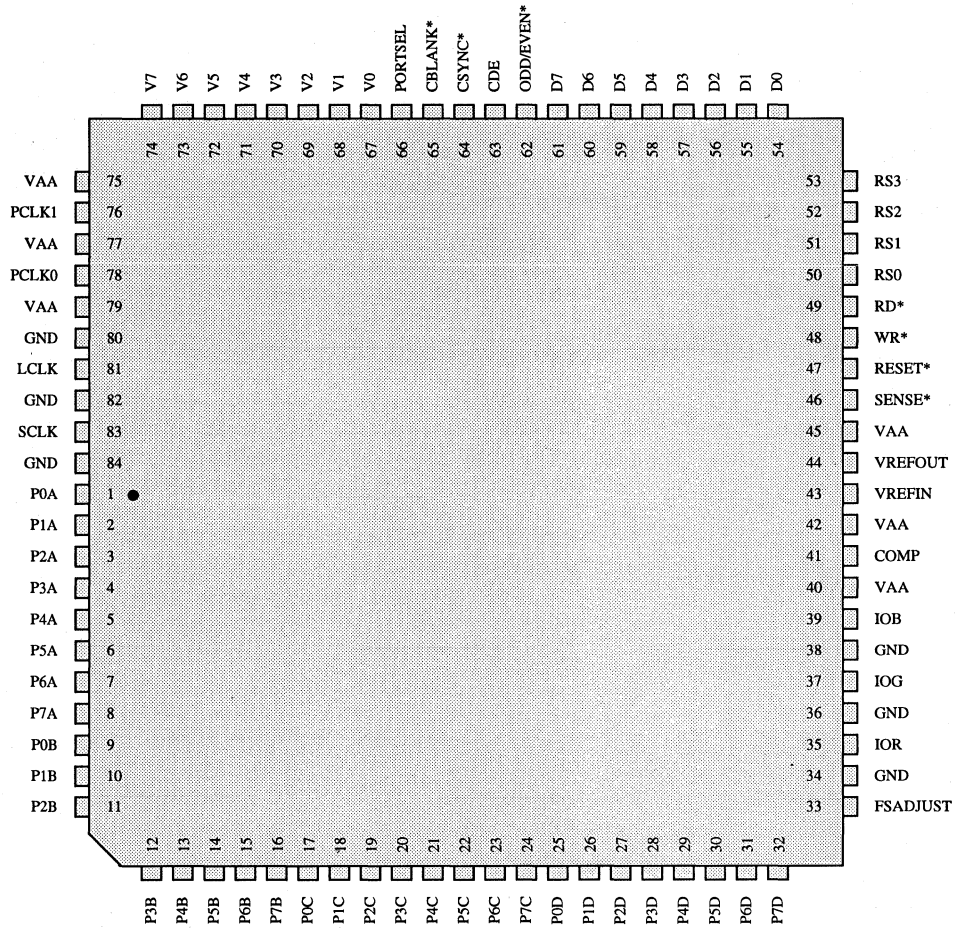
RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications).

<table>
<tr><th></th><th colspan="2">Sync Enabled</th><th colspan="2">Sync Disabled</th></tr>
<tr><th>Setup</th><td>0 IRE</td><td>7.5 IRE</td><td>0 IRE</td><td>7.5 IRE</td></tr>
<tr><th>K (8 bits)</th><td>3.025</td><td>3.195</td><td>2.120</td><td>2.280</td></tr>
<tr><th>K (6 bits)</th><td>3.000</td><td>3.170</td><td>2.100</td><td>2.260</td></tr>
</table>

K values are subject to change upon completion of characterization.</td></tr>
<tr><td>VREF OUT</td><td>44</td><td>Voltage reference output. This output provides a 1.235 V (typical) reference and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating. (See Figures 6 and 7.) Up to four Bt485s can be driven by this output.</td></tr>
<tr><td>VREF IN</td><td>43</td><td>Voltage reference input. If an external voltage reference is used (Figure 7), it must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figures 6 and 7. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor (Figure 6).</td></tr>
<tr><td>COMP</td><td>41</td><td>Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>VAA</td><td>40, 42, 45, 75, 77, 79</td><td>Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>GND</td><td>34, 36, 38, 80, 82, 84</td><td>Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
</table>

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt485, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt485 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt485 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt485 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 6 and 7. This bead should be located within 3 inches of the Bt485. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 6 and 7 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt485 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt485 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt485 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt485 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt485 to minimize reflections. Unused analog outputs should be connected to GND.

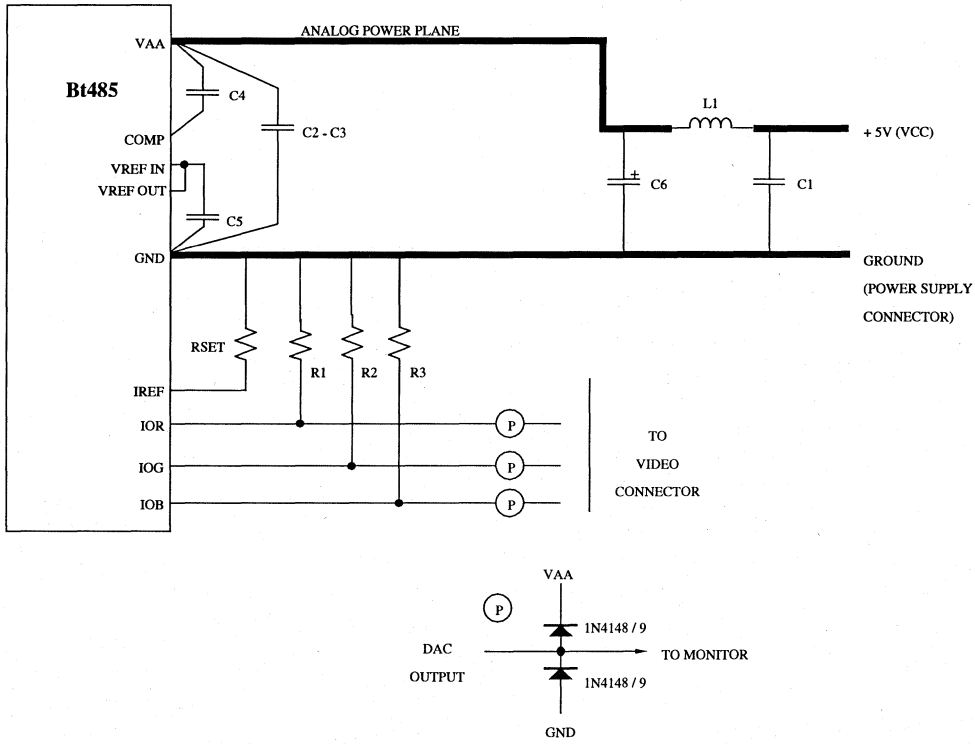
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt485 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 6 and 7 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



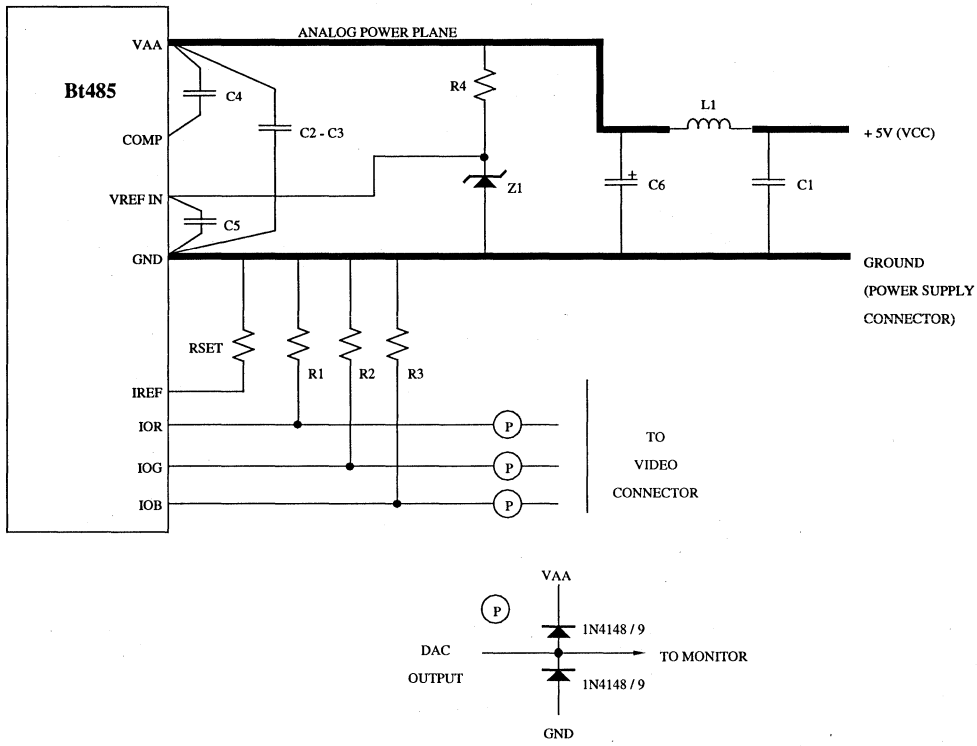
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt485.

Figure 6. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	147 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt485.

Figure 7. Typical Connection Diagram and Parts List (External Voltage Reference).

Application Information

Using Multiple Devices

When multiple Bt485s are used, each Bt485 should have its own power plane ferrite bead. If the internal reference is used, each Bt485 should use its own internal reference.

Although the multiple Bt485s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt485 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about ten times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

Recommended Operating Conditions

(All numbers are preliminary and will be finalized upon completion of characterization)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration	VREF				V
Reference Voltage		1.112	1.235	1.359	

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

(All numbers are preliminary and will be finalized upon completion of characterization)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

(All numbers are preliminary and will be finalized upon completion of characterization)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Onboard VREF	VREFOUT	TBD	TBD	TBD	V
Voltage Reference Input Current	IVR IN				mA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, RSET = 147 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: When the Bt485 is in the 6-bit mode, the output levels are approximately 1.5-percent lower than these values.

AC Characteristics

(All numbers are preliminary and will be finalized upon completion of characterization)

		135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
PCLK 0, PCLK 1 All MUX Rates	Fmax			135			110	MHz
RS0–RS3 Setup Time (Figure 8)	1	10			10			ns
RS0–RS3 Hold Time	2	10			10			ns
RD* Asserted to D0–D7 Driven	3	2			2			ns
RD* Asserted to D0–D7 Valid	4			40			40	ns
RD* Negated to D0–D7 3-Stated	5			20			20	ns
Read D0–D7 Hold Time	6	2			2			ns
Write D0–D7 Setup Time	7	10			10			ns
Write D0–D7 Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*pclk			6*pclk			ns
LCLK Rates (Figures 9 and 10)	Lmax							
8:1 Multiplexing				16.9			13.75	MHz
4:1 Multiplexing				33.8			27.5	MHz
2:1 Multiplexing				67.5			55	MHz
1:1 Multiplexing or VGA				90			90	MHz
SCLK Rate	Smax							
8:1 Multiplexing				16.9			13.75	MHz
4:1 Multiplexing				33.8			27.5	MHz
2:1 Multiplexing				42.50			37.50	MHz
1:1 Multiplexing or VGA				50.35			50.35	MHz
PCLK 0, PCLK 1 Cycle Time (Note 1) All MUX Rates	11	14.81			18.18			ns
PCLK 0, PCLK 1 Pulse Width High All MUX Rates	12	tbd			tbd			ns
PCLK 0, PCLK 1 Pulse Width Low All MUX Rates	13	tbd			tbd			ns
Duty Cycle 2xPCLK		tbd	tbd	tbd	tbd	tbd	tbd	%
LCLK Cycle Time	14							
8:1 Multiplexing		59.17			72.72			ns
4:1 Multiplexing		29.58			36.36			ns
2:1 Multiplexing		14.81			18.18			ns
1:1 Multiplexing or VGA		11.11			11.11			ns
LCLK Pulse Width High	15							
8:1 Multiplexing		4			4			ns
4:1 Multiplexing		4			4			ns
2:1 Multiplexing		4			4			ns
1:1 Multiplexing or VGA		4			4			ns
LCLK Pulse Width Low	16							
8:1 Multiplexing		4			4			ns
4:1 Multiplexing		4			4			ns
2:1 Multiplexing		4			4			ns
1:1 Multiplexing or VGA		4			4			ns

See test conditions at end of this section.

AC Characteristics *(continued)*

(All numbers are preliminary and will be finalized upon completion of characterization)

		135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
SCLK Cycle Time	17							
8:1 Multiplexing		59.17			72.72			ns
4:1 Multiplexing		29.58			36.36			ns
2:1 Multiplexing		23.53			26.67			ns
1:1 Multiplexing or VGA		19.86			19.86			ns
Data Setup to LCLK P7:0(A-D)	18	1			1			ns
Data Hold from LCLK P7:0(A-D)	19	5			5			ns
Data Setup and Hold to LCLK VGA(7:0), CDE, CBLANK*	20	3			3			ns
CSYNC*, PORTSEL								ns
LCLK valid skew with respect to SCLK (Note 2)	21	–3		T–14	–3		T–14	ns
SCLK Output Delay (1:1 mode) (Note 3)								
SCLK Output Delay (MUX mode) (Note 3)	22		6	11			11	ns
Analog Output Delay			10	20			20	ns
Analog Output Rise/Fall Time				30			30	ns
Analog Output Settling Time (Note 4)	23		3					ns
Clock and Data Feedthrough (Note 4)	24		13					ns
Glitch Impulse (Note 4)	25		–30					dB
SENSE* Output Delay			75					pV - sec
DAC-to-DAC Crosstalk	26		1					µs
Analog Output Skew			–23					dB
				2			2	ns
VAA Supply Current (Note 5)								
Normal Operation	IAA							mA
Sleep Mode (Note 6)			TBD	TBD			TBD	mA
			TBD	TBD			TBD	mA

See test conditions at end of this section.

Pipeline Delay	MIN	MAX
1:1/VGA mode	8 LCLKS	8 LCLKS
2:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 8 PCLKS
4:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 10 PCLKS
8:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 14 PCLKS

Pipeline delay (MIN) is the minimum number of clocks required to output 1 pixel after all pixels have been latched. Pipeline delay (MAX) is the maximum number of clocks required to output all pixels after all pixels have been latched. In the 1:1/VGA mode, LCLK is the primary clock latching and pipelining for the pixels.

AC Characteristics *(continued)*

(All numbers are preliminary and will be finalized upon completion of characterization)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 147 Ω. TTL input values are 0–3 V with input rise/fall times ≤3 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF; SENSE* and D0–D7 output load ≤50 pF. SCLK output load = 50 pF. See timing notes in Figures 8 and 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Note 1: To pipeline data at 110 or 135 MHz, the 2 x clock multiplier must be activated. Duty cycle range TBD.

Note 2: T = SCLK cycle time. Approximate numbers based on Bt484. Actual specifications will be determined upon characterization of the Bt485.

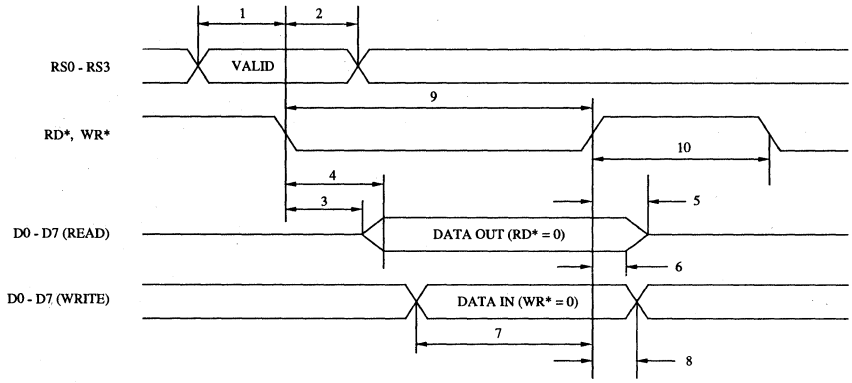
Note 3: Approximate numbers based on Bt484. Actual specifications will be determined upon characterization of the Bt485.

Note 4: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 5: At 135 MHz. IAA (typ) at VAA = 5.0 V, 25°C. IAA (max) at VAA = 5.25 V, 70°C. 4:1 MUX mode at 40-percent blanking.

Note 6: External voltage reference is disabled during sleep mode, all inputs are low, and clock is running.

Timing Waveforms



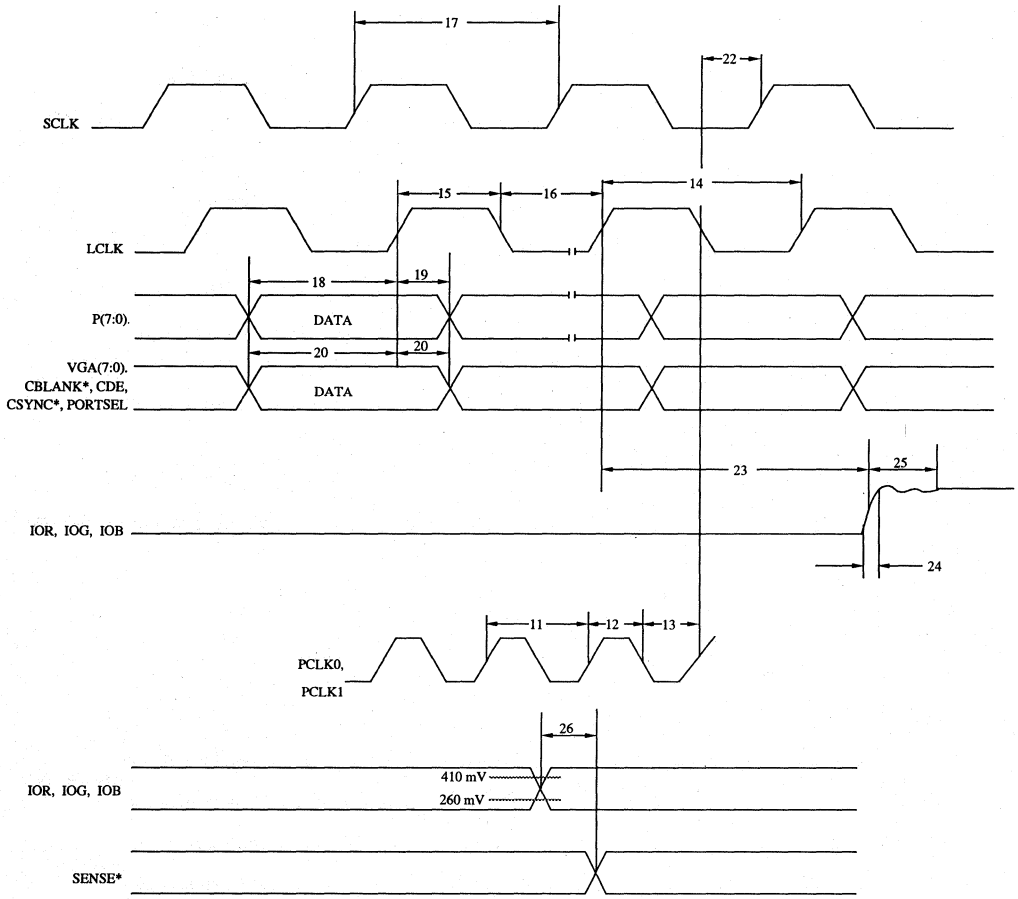
Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. MPU Read/Write Timing.

Timing Waveforms *(continued)*



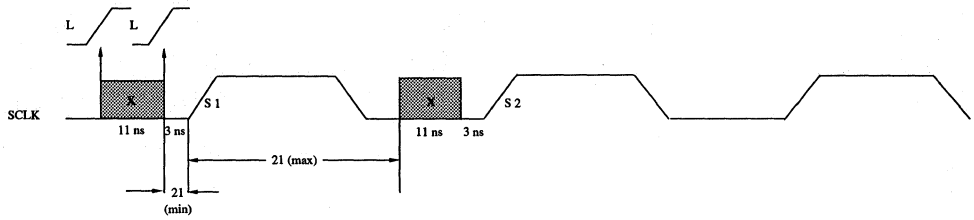
Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of

Figure 9. Video Input/Output Timing (Non-1:1).

Timing Waveforms *(continued)*



L = LCLK rising edges

S1 = First SCLK rising edge

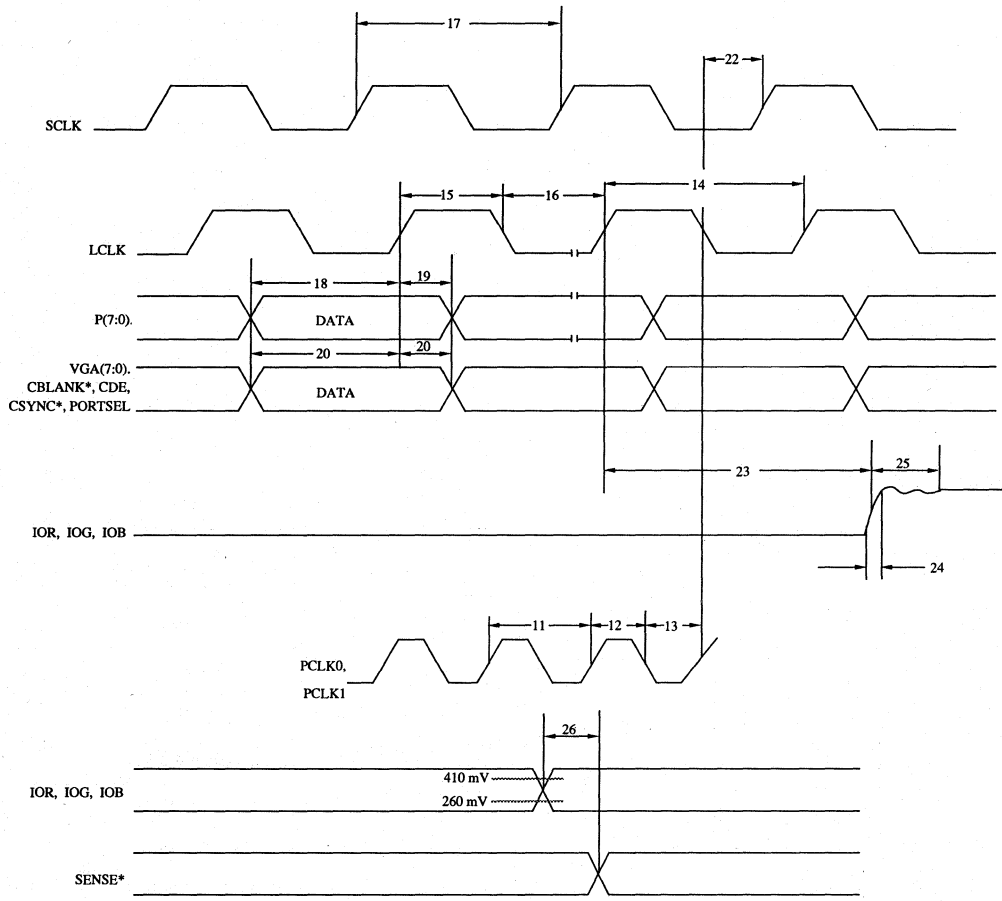
S2 = Second SCLK rising edge

In order for the pixel data latched by LCLK to be synchronized correctly with the internal PCLK clock, an LCLK rising edge cannot occur in an invalid window, as illustrated above.

If L occurs within the 11 ns invalid region (X), it is not guaranteed on which rising edge of SCLK (S1 or S2) the data will be synchronized. If L occurs before the 11 ns invalid region (X), then the data is guaranteed to be synchronized on S1. If L occurs after the 11 ns invalid region (X), then the data will not be synchronized on S1 and is guaranteed to be synchronized on S2.

Figure 9 (continued). Video Input/Output Timing (Non-1:1).

Timing Waveforms *(continued)*



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 10. Video Input/Output Timing (1:1 MUX Rates).

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Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt485KPJ135	135 MHz	84-pin Plastic J-Lead	0° to +70°C
Bt485KPJ110	110 MHz	84-pin Plastic J-Lead	0° to +70°C

Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice.

Bt885

135 MHz
Monolithic CMOS
Video CacheDAC™

Distinguishing Features

- 135 MHz Pipelined Operation
- VGA Compatible
- Mixed Video and Graphics
- 64-bit Graphics/Video Pixel Ports
- YCrCb-to-RGB Conversion
- YCrCb 4:2:2 and 2:1:1 Interpolation
- Uses Brooktree's VideoCache™ Technology
- Horizontal Video Upscaling
- 64 x 64 x 2 Cursor
- VRAM Shift Clock Support
- Enables DRAM Based Motion Video Systems
- Programmable Video Extents
- Programmable Color Keying
- Three 256 x 8 Color Palette RAMs
- Simplifies Integration of Video into Microsoft Windows™
- 3 x 24 Cursor Color Palette
- Standard MPU Interface
- Power-Down Mode
- Directly Implements Brooktree's VideoCache™ Connector
- 160 PQFP

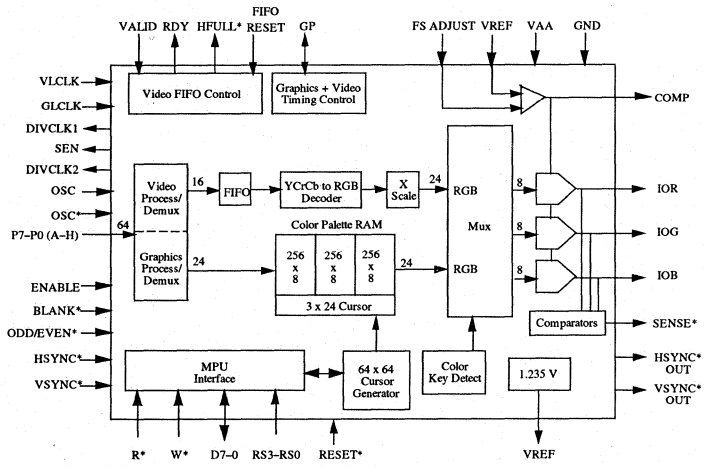
Applications

- Video Decompression Acceleration
- Multimedia Workstations
- High-Resolution Graphics
- Desktop Video

Related Products

- Bt812 Video Decoder
- Bt858 Video Encoder
- BtVLD Video Loader Device

Functional Block Diagram



Product Description

The Bt885 is designed specifically for dual or unified frame buffer multimedia subsystems. A dedicated video port accepts either an 8- or 16-bit CCIR601 YCrCb data stream and allows onscreen switching on a pixel-by-pixel basis. Mixing occurs within programmable video extents based on a flexible color key mechanism. Bt885 is intended to replace multiple RAMDAC™-based multimedia subsystems. The Bt885 register set is VGA compatible.

The Bt885 can operate with video decompression and Bt812 processor chips using programmable interpolation for CCIR601 4:2:2, 2:1:1, and 1:0.5:0.5 formats so that video data mixes with the graphics data at the same rate.

Using Brooktree's 800-byte VideoCache™ FIFO enables asynchronous delivery of graphics and video, easing system bandwidth requirements for video transfer, and allows for efficient use of system memory. Non-integer scaling permits arbitrary video window sizing.

The 64 x 64 x 2 bit cursor has its own palette and has priority over the video or graphics. The cursor operates in three modes: Microsoft Windows™, three color, and X Windows.

The Bt885 supports independent 32-bit graphics and 32-bit video pixel ports and is compatible with both VRAM and DRAM based video subsystems.

The Bt885 generates RS-343A compatible video signals into a doubly-terminated 75 Ω load, or RS-170 compatible video signals into a singly-terminated 75 Ω load. No external buffering is required.

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L885001 Rev.A

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Section 5

WORKSTATION GRAPHICS RAMDACs

5

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Contents

Advance

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Bt445

150 MHz Monolithic CMOS Triple 256 x 8 RAMDAC™

Distinguishing Features

- PLL Pixel Clock Generation (M/N)
- Up to 64-Bit Input Pixel Port Width
- 150, 135, and 110 MHz Operation
- High-Resolution True-Color Support
- 1:1 to 64:1 Multiplexed Pixel Port
- Bt458 Software Compatible
- Programmable Pixel Format
- Three 256 x 8 Color Palette RAMs
- 16 x 24 Overlay Palette
- 4 x 24 Cursor Palette
- Digital Pixel Output Port
- 0 or 7.5 IRE Blanking
- VRAM Shift Clock Generation
- System Clock Generation
- JTAG Support
- 160-pin PQFP Package

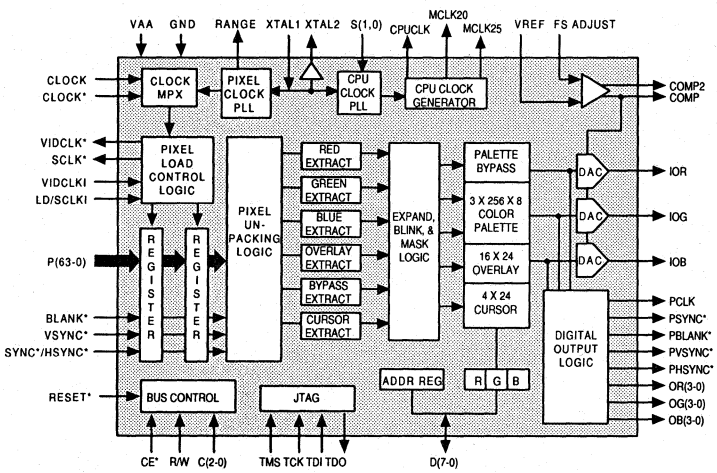
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Color Flat Panel Displays

Related Products

- Bt431
- Bt458
- Bt858

Functional Block Diagram



Product Description

The Bt445 is designed specifically for high-performance, high-resolution color graphics applications. The wide input pixel port and internal multiplexing modes enable TTL-compatible interfacing to the frame buffer, while maintaining PLL-generated 135 MHz, or externally provided 150 MHz video data rates required for high refresh rate, high-resolution color graphics.

The Bt445 supports PLL pixel clock generation, supporting a variety of frequencies using an M/N divisor scheme. This decreases system cost due to the elimination of multiple crystal oscillators that are used to support a variety of monitor and refresh rates. In addition, the Bt445 provides the serial VRAM clock, video clock, and various multi-purpose system clocks.

Using a patented pixel port architecture, Flexport™, the input pixel port can be configured in an almost unlimited variety of pixel depths, multiplex modes, and input port widths. For example, these modes include 1-, 2-, 4-, 8-, 12-, 16-, and 24-bit/pixel pseudo color and true color with overlay and cursor palette support. The Bt445 runs 24-bit true color, with cursor, overlay, and palette bypass support, at pixel rates for 1280 x 1024 monitors. The Bt445 is also Bt458 software compatible.

Other features include programmable setup and digital pixel outputs, as required for active matrix TFT support or NTSC encoding.

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Circuit Description

Introduction

The Bt445 is a flexible 150-MHz RAMDAC, which provides multiple multiplex operating modes with multiple plane depth resolutions, while still maintaining Bt458 register compatibility.

Two phase lock loops are provided to eliminate high-speed signals on the PCB and expensive ECL crystal oscillators. One is programmable ((M/N)/L), where M is 6 bits, N is 4 bits, and L can be 1, 2, 4, or 8) and is used to generate the pixel clock frequency. The second PLL operates from the same crystal or oscillator input as the pixel PLL, and is not programmable. It may be used to provide additional clock outputs that may be used for the CPU system clocks, and/or SCSI or Ethernet clocks, for example.

The Bt445's input pixel port can be software-configured to be any width from 1–64 pins. This allows maximum versatility for frame buffer configuration. For example, the Bt445 can support a frame buffer architecture having a 6:1 multiplexed 8-bit pseudo-color frame buffer (48 signals) with 2-bit overlay (12 signals). The input port width in this case may be set to 60 pins. A pixel display order can be selected to start from the lower-numbered bits of the input pixel port (LSB unpacking) or from the higher-numbered bits (i.e., the pixel port width, MSB unpacking).

The Bt445 also provides fully programmable multiplex rates (1:1 to 64:1, any integer value) and fully programmable pixel widths (1 to 32 bits per pixel, any integer value). The only restrictions are that the pixel port start position, multiplex rate, and pixel width be consistent. This means that the number of bits per pixel multiplied by the multiplex rate must be less than or equal to the number of input port bits configured. Also, when configured for 1:1 multiplexed, the maximum pixel rate is limited by the input pixel port rate, as indicated in the AC Characteristics section.

After pixel serialization has occurred, the Bt445 allows full configurability for source and width selection of the red, green, blue, overlay, cursor, and palette bypass fields of the source pixel. For example, in a 16-bit wide pixel, the red field may come from bits 4–0, green may come from bits 9–5, blue may come from bits 14–10, and palette bypass control may come from bit 15 of the pixel.

Pseudo-color modes are supported by sourcing the red, green, and blue fields from the same bits in the source pixel. In fact, any fields of an input pixel may appear in any order or be coincident or overlapped with other fields.

The color palette bypass bit controls the selection between color palette usage or bypass. Users can use the lookup table for gamma correction or they can bypass the LUT on a pixel-by-pixel basis. This allows users to customize features with ASICs, while providing capabilities for cost-efficient high-resolution 1280 x 1024 true-color graphics. Color palette bypass is available in all pixel modes, allowing numerous monochrome/gray-scale options on the Bt445.

The Bt445 also provides a digital pixel output port from the DAC inputs to support driving an active matrix TFT LCD or an NTSC encoder such as the Bt858. The Bt445 provides a clock, and the red, green, and blue pixel data prior to the decoder of the DACs. In addition, the pipelined sync and blank outputs are provided so that users can synchronize their timing to valid pixel data. Two modes of operation are provided: 4-4-4 true color where the high-order nibble of red, green, and blue are provided, and an 8-8-8 true-color mode where all bits of red, green, and blue are provided at a reduced pixel rate. When using the digital output port (i.e., output bits OR3–OR0, OG3–OG0, or OB3–OB0), the DAC output quality is not guaranteed.

For battery-powered applications, various power-down modes are available. In one mode, the RAM and DACs are turned off. The RAM retains data and may be accessed for read or write operations by the MPU. Another mode powers down the pixel clock, RAM, and DACs. A video RAM shift clock (SCLK*) is provided by the Bt445, changing the cycle frequency in correspondence with the multiplex factor. This simplifies timing requirements to develop external logic for VRAM timing generation. In addition, the Bt445 provides another output clock (VIDCLK*) which should be used for the generation of the CRT timing signals.

Circuit Description *(continued)*

MPU Interface

As illustrated in the functional block diagram, the Bt445 supports a standard MPU bus interface, allowing the MPU to access the internal control registers and color palettes. The dual-port color palette RAM, overlay palette, and cursor color registers allow color updating without contention with the display refresh process.

Table 1 illustrates how the C(2–0) control inputs work in conjunction with the internal address register to specify which control register, color palette RAM entry, overlay register, or cursor color register will be accessed by the MPU.

The reset pin presets the internal registers, defaulting all internal registers to be compatible with the 4:1 multiplex configuration of the Bt458. Features such as alternate pixel depth modes and multiplex factors are available through the use of the C(2) control pin, which provides access to the extra features.

The 8-bit address register (ADDR(7–0)) is used to address the internal color and control registers, eliminating the requirement for external address multiplexers. ADDR(0) corresponds to D(0) and is the least significant bit.

Reading/Writing Color Data

To write color data the MPU loads the address register with the address of the color palette RAM location, overlay palette, or cursor color register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C(2–0) to select the color register. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C(2–0) to select either the color palette RAM, overlay palette, or cursor color registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR(7–0)) are accessible to the MPU.

Additional Information

Although the color and overlay palette RAMs and cursor color registers are dual ported, if the pixel data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers can also be accessed through the address register in conjunction with the C(2–0) inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

To prevent pixels from being disturbed during writes to the control registers, the MPU data must be valid during the entire chip enable time, or the accesses should be limited to blanking time. The setup time shown in the AC Characteristics section are the minimum required to internally capture the data.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU. This is not recommended, as this may cause problems in Bt445 code-compatible products.

Circuit Description *(continued)*

C(2-0)			ADDR(7-0)	Reset Value [Hex]	Addressed by MPU
0	0	0	$xx		Address Register
0	0	1	$00–$FF		Primary Color Palette RAM*
0	1	0	$00	3A	ID Register ($3A)
			$01	A0	Revision Register ($A0)
			$02		Reserved
			$03		Reserved
			$04	FF	Read Enable Register
			$05	0	Blink Enable Register
			$06	43	Command Register 0
			$07	0	Test Register 0
			$08–$FF		Reserved
0	1	1	$00–$0F		Overlay Color Palette RAM (Note 1)
			$10–$FF		Reserved
1	0	0	$xx		Reserved
1	0	1	$00	07	Red MSB Position
			$01	08	Red Width Control
			$02	FF	Red Display Enable Control
			$03	0	Red Register Blink Enable
			$04–$07		Reserved ($00)
			$08	07	Green MSB Position
			$09	08	Green Width Control
			$0A	FF	Green Display Enable Control
			$0B	0	Green Blink Enable Register
			$0C–$0F		Reserved ($00)
			$10	07	Blue MSB Position
			$11	08	Blue Width Control
			$12	FF	Blue Display Enable Control
			$13	0	Blue Blink Enable Register
			$14–$17		Reserved ($00)
			$18	09	Overlay MSB Position
			$19	02	Overlay Width Control
			$1A	03	Overlay Display Enable Control
			$1B	0	Overlay Blink Enable Register
			$1C–1F		Reserved ($00)
			$20	0	Cursor MSB Position
			$21	02	Cursor Width Control
			$22	03	Cursor Display Enable Control
			$23	0	Cursor Blink Register
			$24–$FF		Reserved ($00)

Table 1. Address Register (ADDR) Operation.

Circuit Description *(continued)*

C(2–0)			ADDR (7–0)	Reset Value [Hex}	Addressed by MPU
1	1	0	$00	0X	Test Register 1
			$01	40	Command Register 1
			$02	0	Digital Output Control Register
			$03	03	VIDCLK* Cycle Control Register
			$04		Reserved
			$05	19	Pixel PLL Rate Register 0
			$06	04	Pixel PLL Rate Register 1
			$07	XX	PLL Control Register
			$08	04	Pixel Load Control Register
			$09	28	Pixel Port Start Position Register
			$0A	08	Pixel Format Control Register
			$0B	03	MPX Rate Register
			$0C	XX	Signature Analysis Registers (Note 1)
			$0D	0A	Pixel Depth Control Register
			$0E	0	Palette Bypass Position
			$0F	01	Palette Bypass Width Control
			$10–$FF		Reserved ($00)
1	1	1	$00		Cursor Color 0 (Note 1)
			$01		Cursor Color 1 (Note 1)
			$02		Cursor Color 2 (Note 1)
			$03		Cursor Color 3 (Note 1)
			$04–$FF		Reserved

Note 1: Requires modulo 3 loading/reading.

Table 1. (continued). Address Register (ADDR) Operation.

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Circuit Description *(continued)*

Clock Generation

The Bt445 has two phase lock loops for generating the pixel clock and three system clocks. (See the Functional Block Diagram and Figure 1). The pixel clock is fully programmable, able to generate over 500 unique pixel clock frequencies using a single crystal.

The advanced phase lock loops (PLLs) contain an internal loop filter to provide maximum noise immunity and reduce jitter. Except for the reference crystal or oscillator, no external components or adjustments are necessary.

The pixel clock generator uses an M over (L x N) scheme to provide precise frequencies. The M, N, and L values can be programmed through the command registers with a variety of values, which generally provide frequency granularity that averages less than 1 MHz. M is a binary 6-bit value, N is a binary 4-bit value, and L is selectable to be 1, 2, 4, or 8. Serial clock and video clocks are generated from the derived pixel clock.

A second PLL generates a number of various clocks (MCLK20, MCLK25, CPUCLK), which may be used for the CPU clock and other system clocks. Using a 20 MHz crystal, a constant 20 MHz and 25 MHz clock is available for Ethernet and SCSI clock generation, while the CPU clock output is selectable between 25, 33, 40, or 50 MHz. The reference crystal used must be an AT cut, with series configuration, and operated in the fundamental mode. An oscillator reference can also be used by capacitively coupling the oscillator's output to the XTAL1 input, as shown in Figure 2. For this configuration, leave the XTAL2 pin disconnected as shown.

Both PLLs can be disabled separately to provide maximum flexibility in configuring the Bt445 to match the system requirements. In order to minimize noise, all unused outputs should be disabled via the command registers. Additionally, in order to provide minimal noise effects to the RAMDAC, all of the clock generated outputs are low drive and must be redriven by a buffer before distribution.

With the assertion of RESET*, the video clock defaults into a mode whereby a one-fourth pixel rate video clock is automatically generated. This rate is consistent with the LD rate needed to use a Bt458 in 4:1 multiplex mode. The PLLs are also initiated with RESET* to generate the system clocks.

As an alternative to using the PLL for pixel clock generation, the Bt445 is also designed to accept differential clock signals (CLOCK and CLOCK* in Figure 2). These clock inputs can be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close to the driving source as possible. A 150-Ω chip resistor near the RAMDAC pins is also needed to ensure proper termination. (See Figure 3).

Circuit Description *(continued)*

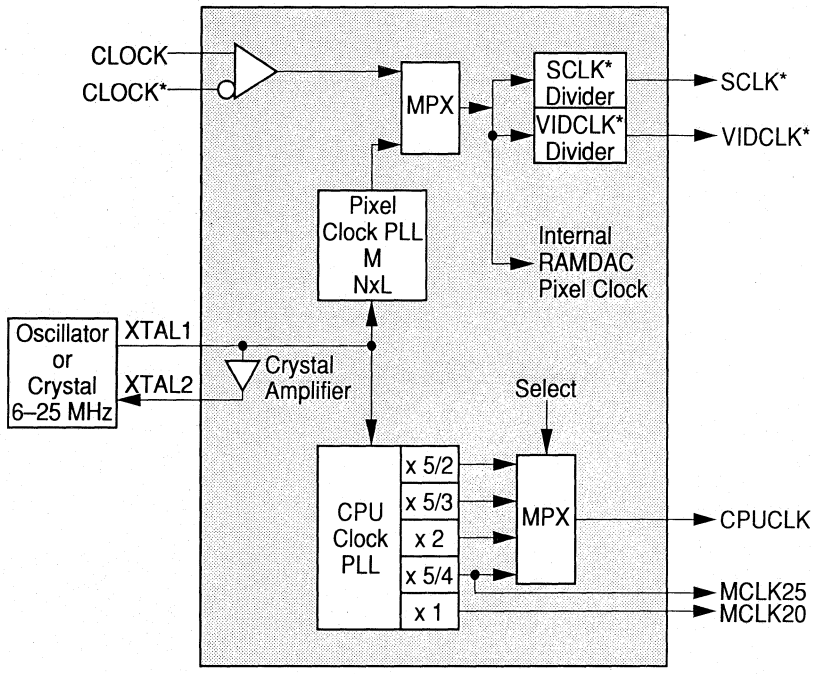

Figure 1. PLL Clock Generation Block Diagram.

Circuit Description *(continued)*

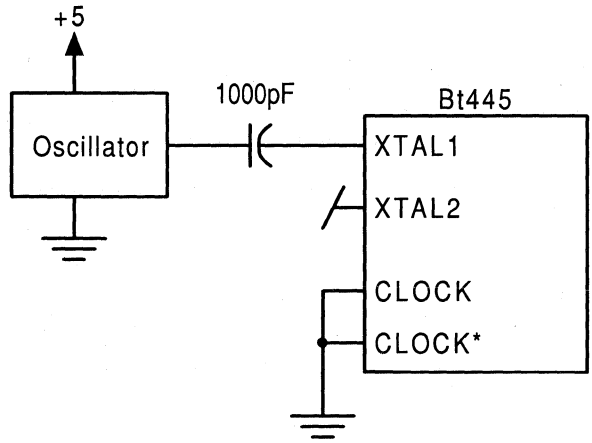

Figure 2. Oscillator Clock Interface.

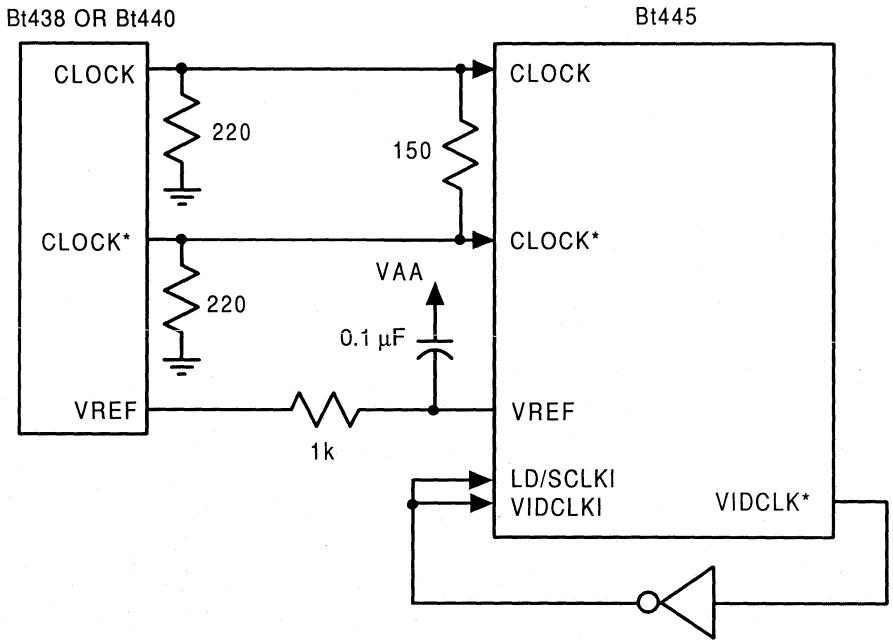

Figure 3. Differential ECL CLock Interface.

Circuit Description *(continued)*

Frame Buffer Clocking

Pixel data may be clocked into the Bt445 in one of two modes: with VIDCLK input and output signals, or with the SCLK input and output signals.

Pixel Loading Using SCLK

System designs that interface VRAM frame buffer serial data directly to the Bt445 can use the SCLK* and LD/SCLKI signal pairs to load pixel data. In this mode, the Bt445 facilitates the generation of the VRAM shift clock by providing VRAM serial shift clock, SCLK*. SCLK* should be used to clock the VRAM shift registers that provide pixel data to the Bt445. The ratio of SCLK* to the pixel clock equals the value set into the MPX rate register.

SCLK* is stopped (in a logical "1" state) during blanking to allow the system to reload the VRAM serial shift registers. System implementations using "midline" transfer may necessitate inserting a VRAM shift clock pulse during blanking time to load the shift register tap address. The system may insert this additional clock without incurring additional gate delays by using a NAND driver for generating SCLK to the VRAMs. The unused input on the NAND driver may be used to insert the additional SCLK to load the tap address. The SCLK* (active low time) pulse width is nominally two pixel clock cycles; as a result, architectures using less than 4:1 multiplexing will not normally use the SCLK*/SCLKI signals for pixel loading. Also refer to the AC timing specifications for the maximum rates at which the SCLK* may be operated.

The buffered version of SCLK*, referred to in this specification as SCLK, is returned to the Bt445 to be used to load the input pixel data. This allows for faster serial path operation, as the buffer delay does not add to the serial port delay in determining the minimum SCLK cycle time at which the system may operate (refer to Figures 4 and 5).

The VIDCLKI signal is still used to load the VSYNC*, HSYNC*, SYNC*, and BLANK* signals. The VIDCLK rate is independent of the pixel depth; the VIDCLK rate is selected by the VIDCLK rate select register.

Pixel Loading Using VIDCLK

System architectures that preclude using the SCLK signals for loading pixel data may instead use the VIDCLK* signal to load pixel data. In this mode of operation, the LD/SCLKI and VIDCLKI should be connected together.

In this mode, the VIDCLK rate select field should be written as the same value as the MPX Rate Register. The SCLK* output is disabled (high-z) when the Bt445 is configured in this mode.

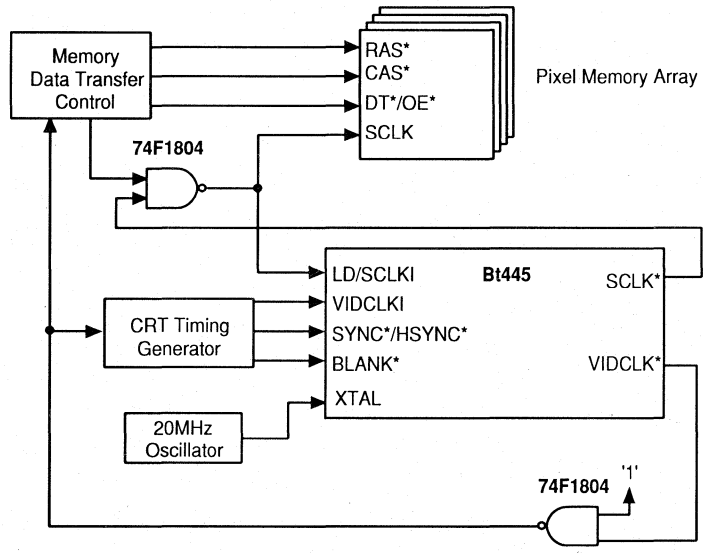

Figure 4. Frame Buffer Clocking Interface, Using SCLK.

Circuit Description *(continued)*

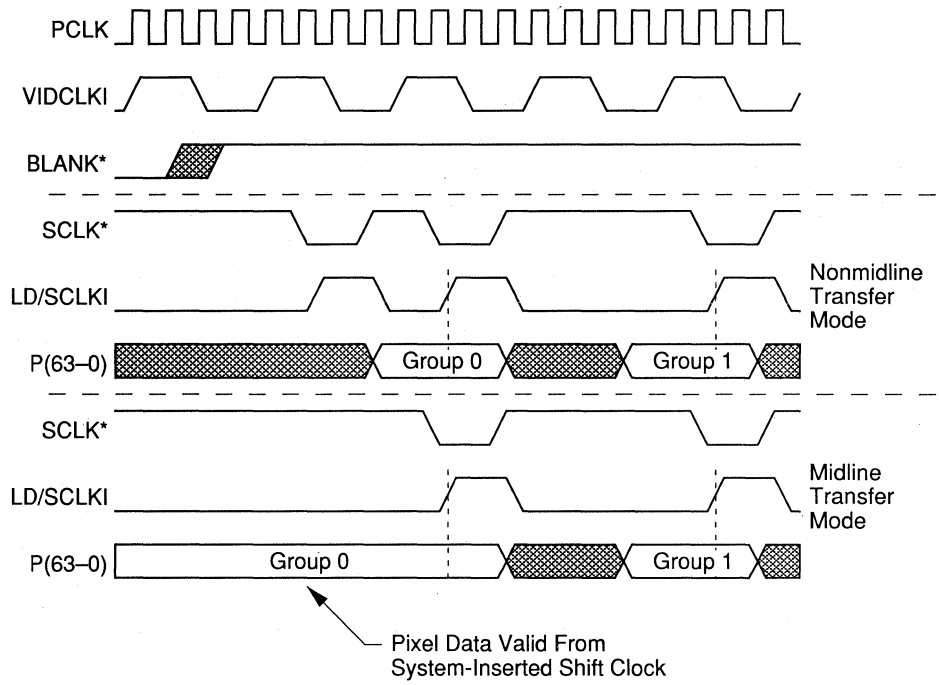

Figure 5. Frame Buffer Interface Timing Diagram Using SCLKI.

Circuit Description *(continued)*

VIDCLK Generation

At reset time, the Bt445 is configured to load pixels using VIDCLK. The multiplex rate is set to 4:1 (Bt458 compatible). When changing the VIDCLK rate, the VIDCLK* output is guaranteed not to glitch when changing from one rate to another. During the transition, the minimum low or high pulse width will be at least the low or high width of the faster of the old or new VIDCLK rate. For 1:1 and 2:1 VIDCLK* rates, the VIDCLK* output will have a 50/50 duty cycle; for 3:1 to 64:1 VIDCLK* rates, the VIDCLK* active (low) pulse width is 2 pixel clocks.

Video Generation

The VIDCLK* output is a free-running clock typically used for clocking the display timing generator. The period of VIDCLK* is independent of SCLK* and is controlled by the MPU by the VIDCLK* rate register. VIDCLK may be the pixel clock divided by any integer from 1–64. SYNC* and BLANK* information are registered with each rising edge of VIDCLKI and inserted into the pipelined pixel stream at the appropriate time.

When using SCLK* to clock pixels, SYNC* and BLANK* are registered by a different clock from the pixel data; therefore, they do not correspond to the pixel inputs that are present at the same time. The SYNC* and BLANK* inputs are used to provide the RAMDAC with timing information.

When the Bt445 is configured for using VIDCLK for loading pixel data, SYNC* and BLANK* correspond to the pixel data being loaded on the same clock edge.

Every clock cycle, the selected color information from the color palette RAMs or overlay registers are presented to the D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 6 and 7.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) may contain sync information. Tables 2 and 3 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the the Bt445 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

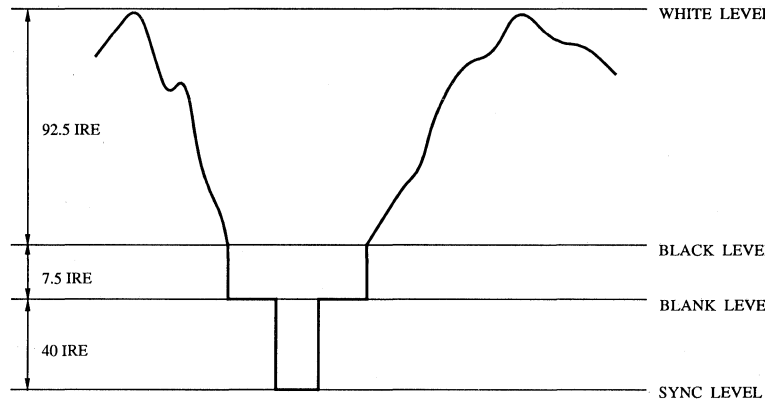

Figure 6. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 2. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
18.6	0.698	26.67	1.00
0.00	0.000	8.05	0.302
0.00	0.000	0.00	0.000

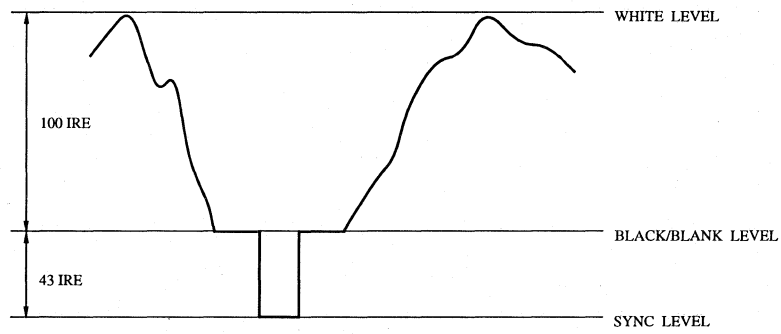

Figure 7. Composite Video Output Waveform SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.5	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 3. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

Frame Buffer Interface

Systems Using VIDCLK* for Loading Pixel Data

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt445 incorporates internal registers and multiplexers. As illustrated in Figure 8, on the rising edge of LD/SCLKI and VIDCLKI, sync and blank information, color, overlay, cursor, and palette bypass information are all registered. The number of pixels supplied for each input cycle depends on the multiplex rate as determined by the current mode. Note that with this configuration, the sync and blank timing will be recognized only with load pixel rate resolution, set by the multiplex mode. Typically, the LD/SCLKI signal is generated from the inverted signal of the VIDCLK* output of the Bt445.

Pixel port bits used as overlay inputs have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

LD/SCLKI may be phase shifted in any amount relative to CLOCK or VIDCLK*. As a result, the pixel and overlay data are registered on the rising edge of LD/SCLKI, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD/SCLKI signal by at least one, but not more than TBD, clock cycles. This LOAD signal transfers the registered pixel and overlay data into a second set of registers, which are then internally multiplexed at the pixel clock rate.

Color Selection

At each pixel port load cycle, one or more pixels consisting of color, overlay, cursor, and/or palette bypass information are processed by the multiplexing and unpacking logic, read masks, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

The color selection process may be broken down into the following steps:

1. Multiplex the input pixels from the pixel port load cycle to the pixel clock rate using the appropriate pixel port start position, pixel unpacking mode, and pixel multiplex mode.
2. Expand the resulting 1:1 pixel data to 8 bits each of red, green, and blue; 4 bits of overlay; 2 bits of

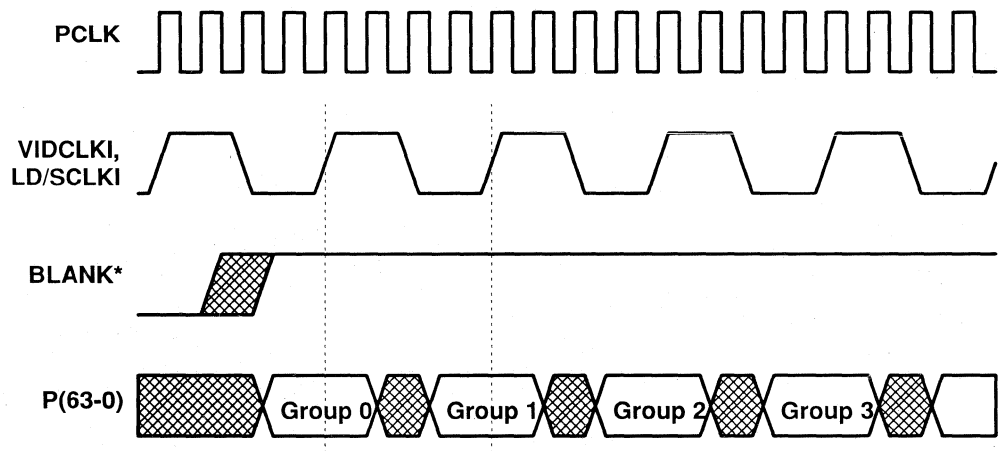

Figure 8. Frame Buffer and Pixel Port Timing Diagram, Using VIDCLK*Output.

cursor; and 1 bit of palette bypass control. Pseudo-color modes will supply the same 8-bit result to each of the red, green, and blue colors at this point.

3. Apply the appropriate read masks to the pixel data.
4. Apply the appropriate blink masks to the pixel data.
5. If the palette is bypassed apply the resulting pixel data directly to the DAC inputs; otherwise, apply the pixel data to the addresses of each of the respectively red, green, and blue color palettes. Use the results to drive the DACs inputs.

Pixel Port Start Position Selection

The Bt445's pixel path architecture allows the configurability of the starting position for pixel unpacking. This provides the system designer with greater options to tailor the Bt445 to the desired frame buffer organization. The starting position is configured via the Pixel Port Start Position Register and may be specified to be any position from P(63) to P(0).

One use could be in systems utilizing double frame buffer designs. For example, in an MSB unpacking, 8-bit pixel, 4:1 multiplex configuration, frame buffer A could be attached to input pixel port bits P(31–0) and frame buffer B could be attached to input pixel port bits P(63–32). Assuming the other registers have been appropriately programmed, the Bt445 would allow switching between the frame buffers by simply programming a $20 (for frame buffer A) or a $40 (for frame buffer B) into the Pixel Port Start Position Register.

Pixel Unpacking Selection

The Bt445 supports pixel unpacking starting from either the low-order side of the input pixel port (LSB unpacking) or the high-order side of the input pixel port (MSB unpacking). The starting bit for either unpacking direction is specified by using the Pixel Port Start Position Register. For further information, see the Pixel Port Start Position Register in the Internal Register section. Within each pixel, the MSB is the highest numbered bit.

Pixel Depth Selection

The Bt445 provides extremely flexible options for various pixel depths on a frame-by-frame basis. The selection of the pixel depth is set via the Pixel Depth Register. The pixel depth may be specified to be any size from 1–32 bits per pixel. Not all bits of a pixel will necessarily be used. The pixel depth must be consistent with the pixel port start position and multiplex rate.

Multiplex Rate Selection

The Multiplex Rate is selectable independent from the pixel depth and pixel port start position. Valid multiplex rates are 1:1 to 64:1 (any integer amount). Again, the only restriction is that the multiplex rate must be consistent with the pixel depth and pixel port start position. When using VIDCLK to load pixels, the multiplex rate should be programmed at the same rate as the VIDCLK* rate to select the cycle time of VIDCLK*.

Start Position/Pixel Depth/Multiplex Rate Restrictions

The Bt445 is specified to operate at the pixel depths, pixel port start positions, and multiplex rates that satisfy the following relationship:

For MSB unpacking:
$$\text{Start Position} - (\text{Pixel Depth} \times \text{Multiplex Rate}) \geq 0$$

For LSB unpacking:
$$(\text{Pixel Depth} \times \text{Multiplex Rate}) - \text{Start Position} \leq 64$$

Programming the Bt445 to configurations not consistent with this relationship will yield unspecified results that will not be tested or guaranteed.

Pixel Processing

The pixel unpacking process, which uses the pixel port start position, pixel depth, and multiplex rate, internally yields a serialized pixel stream. Each pixel in this serial stream may be up to 32 bits wide, as specified by the Pixel Depth Register. At this point, the individual fields are extracted from each pixel. The fields extracted are: Red, Green, Blue, Overlay, Cursor, and Palette Bypass Control. The red, green, and blue fields may each be up to 8 bits wide, the overlay field may be up to 4 bits wide, and the palette bypass control may be 1 bit wide. The MSB position and width of each of these fields within the pixel is independently specified by the corresponding source and width registers. The fields may overlap or be noncontiguous. For example, for 8-bit pseudo color mode, the red, green, and blue position and width registers would specify the same field of the pixel.

Circuit Description *(continued)*

5-Bit Input Pixel Field		High-order Bits of Input Pixel to be Low-Order Appended	Resulting 8-bit Expanded Field
Hex	Binary		
$00	0 0000	000	$00
$01	0 0001	000	$08
$02	0 0010	000	$10
$03	0 0011	000	$18
$04	0 0100	001	$21
$05	0 0101	001	$29
$06	0 0110	001	$31
$07	0 0111	001	$39
$08	0 1000	010	$42
$09	0 1001	010	$4A
$0A	0 1010	010	$52
$0B	0 1011	010	$5A
$0C	0 1100	011	$63
$0D	0 1101	011	$6B
$0E	0 1110	011	$73
$0F	0 1111	011	$7B
$10	1 0000	100	$84
$11	1 0001	100	$8C
$12	1 0010	100	$94
$13	1 0011	100	$9C
$14	1 0100	101	$A5
$15	1 0101	101	$AD
$16	1 0110	101	$B5
$17	1 0111	101	$BD
$18	1 1000	110	$C6
$19	1 1001	110	$CE
$1A	1 1010	110	$D6
$1B	1 1011	110	$DE
$1C	1 1100	111	$E7
$1D	1 1101	111	$EF
$1E	1 1110	111	$F7
$1F	1 1111	111	$FF

If this effect is not desired, the read mask registers may be used to force the appended LSBs to zero.

Table 4. Expansion of Pixel Color Fields Less Than 8 Bits to an 8-bit Field. Five-bit Pixel Color Field Example.

Generation of Unspecified Pixel Data LSBs

When true-color source pixel data contains less than 8 bits per color channel, it is expanded to 8 bits by left justifying and adding the appropriate LSBs to allow for full-scale and best-fit linearity over the DAC output range. This allows the use of the same gamma correction table for the various pixel modes. Table 4 illustrates this effect by indicating the actual values applied to the red DAC input when in the 16-bit-per-pixel 5-5-5 mode, with palette bypass.

Circuit Description *(continued)*

Color Palette Bypass Mode

The color palette bypass control is used to control the access to the color palette RAM by the pixel data. The overlay and cursor color palette are not affected; they are always used if overlay or cursor data is present. Bypassing the color palette delivers what would have been the palette address directly to the DAC inputs.

Blinking

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt445 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining the number of syncs per blanking time. The Bt445 assumes that a vertical retrace occurs whenever more than one sync occurs during a blank interval.

Systems that do not require separate sync for the digital output section may provide a composite sync input on the SYNC*/HSYNC* input pin; the VSYNC* input should be a logical one. The Bt445 generates composite SYNC* by logically ORing the SYNC*/HSYNC* input with the VSYNC* input.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM.

Pixel Output Interface

The digital pixel output interface can be operated in either of two true-color modes: 4-4-4 or 8-8-8. This interface also provides the pixel output clock (PCLK), pipelined sync (PSYNC*) and pipelined blank (PBLANK*) outputs, and 12 bits of data. The pixel output interface signals OR(3–0), OG(3–0), OB(3–0), and PCLK are specified to run at a maximum pixel rate of 55 MHz when in 4-4-4 mode, or 27.5 MHz when in 8-8-8 mode (see Figure 9).

4-4-4 True-Color Mode

When operated in 4-4-4 true-color mode, the pixel output interface provides 12 bits of pixel data, (one pixel) on each rising or falling edge of the pixel clock output, where each group of 4 bits corresponds to the most significant nibble of the 3 bytes being provided at the red, green, and blue DAC inputs. OR(3–0) carries the R(7–4), OG(3–0) carries G(7–4), and OB(3–0) carries B(7–4).

8-8-8 True-Color Mode

When operated in 8-8-8 true-color mode, the pixel output interface provides 24 bits of pixel data each PCLK cycle. Each edge of the pixel data carries 12 bits of the pixel data, first the high order nibbles of red,

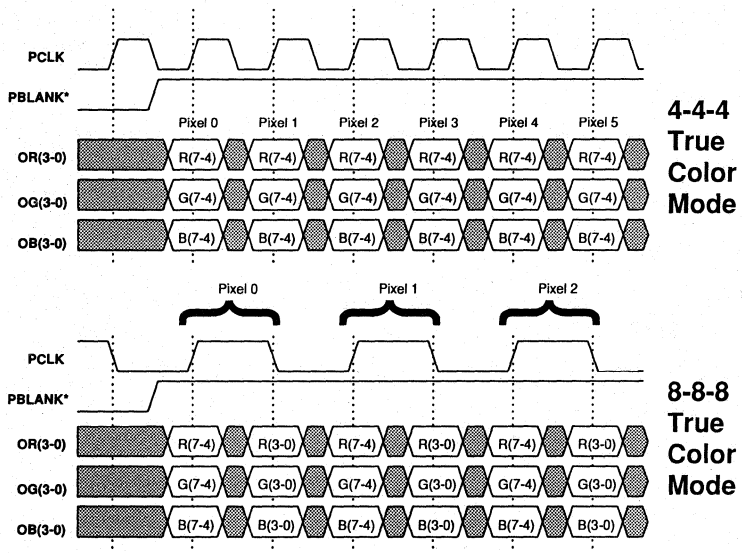

Figure 9. Pixel Output Interface Modes Representative Timing Diagram.

Circuit Description *(continued)*

green, and blue are presented on the rising edge of the pixel clock, then the low-order nibbles are presented on the falling edge of the clock. Note that decreased horizontal spacial resolution is traded for increased color resolution.

Reset Initialization

The S0 and S1 inputs are used at reset time to load the PLL Control Register with the proper CPU output clock multiplex rate. This allows for immediate proper selection of the CPU clock rate. While RESET* is a logical zero, the S0 and S1 inputs flow through and are latched as RESET* rises. The CPU output clocks are also glitchless during transitions as defined for VID-CLK rate transitions.

Power-Down Mode

The Bt445 incorporates a power-down capability, controlled by command bits CR13 and CR14. While both command bits are a logical zero, the Bt445 functions in the normal operating mode.

The command bits can be set so that the DACs and power to the RAM are turned off. Note that the RAM still retains the data. The RAM may be read by or written through the MPU. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. The DACs output no current, and the command registers may still be written to or read by the MPU. Note that the output DACs require about 1 second to turn off (sleep mode) or turn on depending on the compensation capacitor.

In order to conserve power during TFT-only operation, the DACs can be turned off, shunting valid pixel data to the TTL outputs. During this operation, the RAM is still active, indexing pixel data to RGB values.

Boundary Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt445 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to IEEE P1149.1, *Standard Test Access Port and Boundary Scan Architecture*, the Bt445 has dedicated pins which are used for test purposes only.

JTAG uses boundary-scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a Boundary-Scan Register (BSR), which applies or captures test data used for functional verification of the RAMDAC. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select) TCK (Test Clock), TDI (Test Data Input) and TDO (Test Data Out). Complete verification of the RAMDAC can be achieved through these four TAP pins. With boundary-scan cells at each digital pin, the Bt445 is able to apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt445 from the other components on the board, the user has easy access to all Bt445 digital pins through the TAP and can perform complete functionality testing without using expensive bed-of-nails testers.

The bidirectional MPU port and all digital outputs require extra attention with respect to JTAG. Because JTAG requires full control over each digital pin, additional output enable (OE) cells are included in the BSR for the MPU I/O port and various digital outputs. When loaded by the JTAG instructions, these OE cells control the driving strength of their respective pins.

With the JTAG bus, users also have access to a vital portion of the Bt445, the Signature Analysis Register (see Figure 10). With access to this register, users can easily verify expected video data serially through the JTAG port. The SAR is located between the lookup table and the inputs to the DACs.

With the power-on reset (POR) circuitry, the Bt445 will initialize each pin to operate in a RAMDAC mode instead of a JTAG test mode during power-up sequence.

Circuit Description *(continued)*

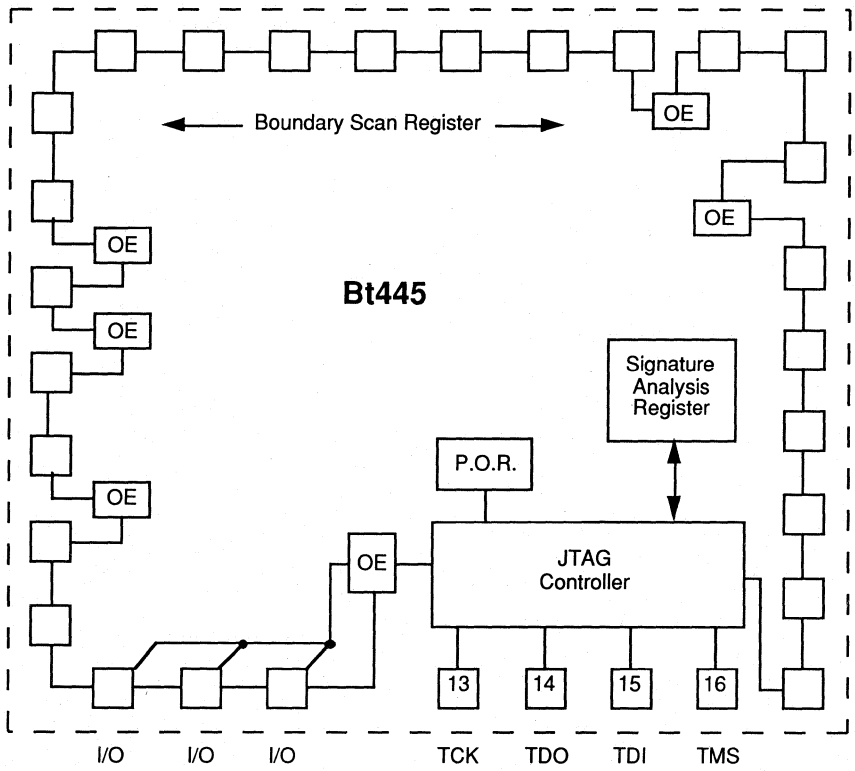

Figure 10. JTAG Block Diagram.

Internal Registers

The following are important programming notes regarding future code compatibility:

- Internal reserved address locations should not be accessed.
- To ensure compatibility with future Bt445 code-compatible devices, reserved values for fields should never be written.
- To ensure compatibility with future Bt445 code-compatible devices, reserved bits should be maintained with read-modify-writes, which only update the unreserved bits. Furthermore, when testing the contents of internal registers, reserved fields should be ANDed off prior to making comparisons. Although it should not be assumed that these reserved bits will always return zeros when read, the reset values will always be as shown.
- It is recommended that the lower 2 bits of overlay blink-and-read mask values be read and/or written from the extended register space (i.e., C(2)=1). Although functionally equivalent to accesses from the Bt458-compatible address space, new code will be easier to modify for future Bt445 code-compatible devices if these accesses are made in the extended register space.

Internal Registers *(continued)*

Command Register 0

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Reserved (logical zero)	0	In the Bt458, this bit specifies 4:1 multiplex mode. In the Bt445, this bit is ignored. To configure the Bt445 for Bt458-compatible 5:1, the extended Bt445 register set must be used.
6	Overlay color 0 disable (0) Use overlay color 0 (1) Use color palette RAM	1	When the overlay select bits are 0000, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
5,4	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	00	These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).
3	Overlay Plane 1 blink enable (0) Disable blinking (1) Enable blinking	0	If a logical one, this bit forces the overlay bit 1 inputs, if any, to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the overlay bit 1 inputs. This bit is also mapped into the Overlay Blink Enable Register bit 1.
2	Overlay Plane 0 blink enable (0) Disable blinking (1) Enable blinking	0	If a logical one, this bit forces the overlay bit 0 inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the overlay bit 0 inputs. This bit is also mapped into the Overlay Blink Enable Register bit 0.
1	Overlay plane 1 display enable (0) Disable (1) Enable	1	If a logical zero, this bit forces the overlay plane 1 inputs, if any, to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the overlay plane 1 input. This bit is also mapped into the Overlay Display Enable Register bit 1.
0	Overlay plane 0 display enable (0) Disable (1) Enable	1	If a logical zero, this bit forces the overlay plane 0 inputs, if any, to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the overlay plane 0 input. This bit is also mapped into the Overlay Display Enable Register bit 0.

Internal Registers *(continued)*

Command Register 1

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Green sync enable (0) Disable sync on IOG (1) Enable sync on IOG	0	This bit enables or disables sync information from being generated on the IOG output.
6	Pedestal Enable (0) 0 IRE (1) 7.5 IRE	1	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. A 0 IRE specifies that the black and blank levels are the same.
5	Reserved	0	Reserved for future expansion.
4,3	Power Down Enable (00) Normal Operation (01) DACs off (10) DACs and RAM off (11) Disable Internal Clocking	00	While these bits are 00, the device operates normally. With the DACs off standard operation occurs, but the output of the LUT is routed directly to the TTL outputs. If these register bits are set for the DACs and power to the RAM is turned off, functional operation is discontinued. In both power-down modes, the RAM still retains the data, and CPU reads and writes can occur with no loss of data. While the device is in the disable internal clocking mode, the internal clock and other output clock modes are completely disabled to further conserve power when in power-down mode. The RAM still retains the data and MPU reads and writes can occur with no loss of data.
2	Palette Addressing Mode (0) Sparse (1) Contiguous	0	This bit controls the field expansion mode. When this bit is a logical zero, pixel fields containing fewer than the normal width of the field will be expanded by left justifying the specified bits and using group replication onto the unspecified lower bits. When this bit is a logical one, the specified bits will be right justified with zeros placed onto the unspecified MSBs.
1	Signature Analysis Enable (0) Disable SAR (1) Enable SAR	0	This bit enables operation of all signature analysis register (SAR) clocking. A logical zero is the normal mode, the SAR disabled. Writing a logical one enables the SAR for operation on every pixel. As slightly more power is consumed when the SAR is enabled, it is recommended that the SAR be disabled when not actually being used.
0	Reset Pipelined Depth	0	Transitioning this bit from a logical zero to a logical one causes the pixel pipeline depth to be initialized. For further information, see "Pipeline Delay Initialization" in the Applications section.

Internal Registers *(continued)*

Red MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$07	Position of the MSB of the red field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the red color palette or red DAC output. The value specified should be less than the pixel size.

Red Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits : ($08)–8 Bits ($09)–Reserved : ($FF)–Reserved	$08	Number of bits to be used for the red field in a pixel. The size and position of the red field must lie within the defined pixel size.

Red Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–0	Blink Enable	$00	Bits 7–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) pixel planes 7–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. The register is also written with MPU data whenever the Bt458-compatible blink register is written.

Internal Registers *(continued)*

Red Display Enable Control

This register is also written when the Bt458-compatible read mask register is written.

Bit(s)	Field Name	Reset Value	Field Description
7	Enable Bit Plane 7 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 7. A logical zero causes bit 7 of the red field of the pixel to be forced to zero. A logical one causes bit 7 of the red field to pass to the color palette or DAC.
6	Enable Bit Plane 6 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 6. A logical zero causes bit 6 of the red field of the pixel to be forced to zero. A logical one causes bit 6 of the red field to pass to the color palette or DAC.
5	Enable Bit Plane 5 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 5. A logical zero causes bit 5 of the red field of the pixel to be forced to zero. A logical one causes bit 5 of the red field to pass to the color palette or DAC.
4	Enable Bit Plane 4 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 4. A logical zero causes bit 4 of the red field of the pixel to be forced to zero. A logical one causes bit 4 of the red field to pass to the color palette or DAC.
3	Enable Bit Plane 3 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 3. A logical zero causes bit 3 of the red field of the pixel to be forced to zero. A logical one causes bit 3 of the red field to pass to the color palette or DAC.
2	Enable Bit Plane 2 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 2. A logical zero causes bit 2 of the red field of the pixel to be forced to zero. A logical one causes bit 2 of the red field to pass to the color palette or DAC.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 1. A logical zero causes bit 1 of the red field of the pixel to be forced to zero. A logical one causes bit 1 of the red field to pass to the color palette or DAC.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 0. A logical zero causes bit 0 of the red field of the pixel to be forced to zero. A logical one causes bit 0 of the red field to pass to the color palette or DAC.

Internal Registers *(continued)*

Green MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$07	Position of the MSB of the green field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the green color palette or green DAC output. The value specified should be less than the pixel size.

Green Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits : ($08)–8 Bits ($09)–Reserved : ($FF)–Reserved	$08	Number of bits to be used for the green field in a pixel. The size and position of the green field must lie within the defined pixel size.

Green Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–0	Green Blink Enable	$00	Bits 7–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) green pixel planes 7–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. The register is also written with MPU data whenever the Bt458-compatible blink register is written.

Internal Registers *(continued)*

Green Display Enable Control

This register is also written mapped to the Bt458-compatible read mask.

Bit(s)	Field Name	Reset Value	Field Description
7	Enable Bit Plane 7 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 7. A logical zero causes bit 7 of the green field of the pixel to be forced to zero. A logical one causes bit 7 of the green field to pass to the color palette or DAC.
6	Enable Bit Plane 6 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 6. A logical zero causes bit 6 of the green field of the pixel to be forced to zero. A logical one causes bit 6 of the green field to pass to the color palette or DAC.
5	Enable Bit Plane 5 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 5. A logical zero causes bit 5 of the green field of the pixel to be forced to zero. A logical one causes bit 5 of the green field to pass to the color palette or DAC.
4	Enable Bit Plane 4 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 4. A logical zero causes bit 4 of the green field of the pixel to be forced to zero. A logical one causes bit 4 of the green field to pass to the color palette or DAC.
3	Enable Bit Plane 3 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 3. A logical zero causes bit 3 of the green field of the pixel to be forced to zero. A logical one causes bit 3 of the green field to pass to the color palette or DAC.
2	Enable Bit Plane 2 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 2. A logical zero causes bit 2 of the green field of the pixel to be forced to zero. A logical one causes bit 2 of the green field to pass to the color palette or DAC.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 1. A logical zero causes bit 1 of the green field of the pixel to be forced to zero. A logical one causes bit 1 of the green field to pass to the color palette or DAC.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 0. A logical zero causes bit 0 of the green field of the pixel to be forced to zero. A logical one causes bit 0 of the green field to pass to the color palette or DAC.

Internal Registers *(continued)*

Blue MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$07	Position of the MSB of the blue field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the blue color palette or blue DAC output. The value specified should be less than the pixel size.

Blue Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits : ($08)–8 Bits ($09)–Reserved : ($FF)–Reserved	$08	Number of bits to be used for the blue field in a pixel. The size and position of the blue field must lie within the defined pixel size.

Blue Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–0	Blue Blink Enable	$00	Bits 7–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) blue pixel planes 7–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. The register is also written with MPU data whenever the Bt458-compatible blink register is written.

Internal Registers *(continued)*

Blue Display Enable Control

This register is also written when the Bt458-compatible read mask register is written.

Bit(s)	Field Name	Reset Value	Field Description
7	Enable Bit Plane 7 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 7. A logical zero causes bit 7 of the blue field of the pixel to be forced to zero. A logical one causes bit 7 of the blue field to pass to the color palette or DAC.
6	Enable Bit Plane 6 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 6. A logical zero causes bit 6 of the blue field of the pixel to be forced to zero. A logical one causes bit 6 of the blue field to pass to the color palette or DAC.
5	Enable Bit Plane 5 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 5. A logical zero causes bit 5 of the blue field of the pixel to be forced to zero. A logical one causes bit 5 of the blue field to pass to the color palette or DAC.
4	Enable Bit Plane 4 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 4. A logical zero causes bit 4 of the blue field of the pixel to be forced to zero. A logical one causes bit 4 of the blue field to pass to the color palette or DAC.
3	Enable Bit Plane 3 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 3. A logical zero causes bit 3 of the blue field of the pixel to be forced to zero. A logical one causes bit 3 of the blue field to pass to the color palette or DAC.
2	Enable Bit Plane 2 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 2. A logical zero causes bit 2 of the blue field of the pixel to be forced to zero. A logical one causes bit 2 of the blue field to pass to the color palette or DAC.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 1. A logical zero causes bit 1 of the blue field of the pixel to be forced to zero. A logical one causes bit 1 of the blue field to pass to the color palette or DAC.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 0. A logical zero causes bit 0 of the blue field of the pixel to be forced to zero. A logical one causes bit 0 of the blue field to pass to the color palette or DAC.

Internal Registers *(continued)*

Overlay MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$09	Position of the MSB of the overlay field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the overlay palette or all DAC outputs. The value specified should be less than the pixel size.

Overlay Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits ($03)–3 Bits ($04)–4 Bits ($05)–Reserved : ($FF)–Reserved	$02	Number of bits to be used for the overlay field in a pixel. The size and position of the overlay field must lie within the defined pixel size.

Overlay Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–4	Reserved	$0	Reserved for future expansion.
3–0	Overlay Blink Enable	$0	Bits 3–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) overlay pixel planes 3–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. Bits 0 and 1 of this field are also read and written by accessing the Bt458-compatible overlay blink controls in Command Register 0.

Internal Registers *(continued)*

Overlay Display Enable Control

Bits 1 and 0 of this register are also mapped to the Bt458-compatible command register 0 bits 1 and 0.

Bit(s)	Field Name	Reset Value	Field Description
7–4	Reserved	0	Reserved for future expansion.
3	Enable Bit Plane 3 (0) Disable (1) Enable	0	This bit controls the enabling of overlay bit plane 3. A logical zero causes bit 3 of the overlay field of the pixel to be forced to zero. A logical one causes bit 3 of the overlay field to pass to the overlay palette.
2	Enable Bit Plane 2 (0) Disable (1) Enable	0	This bit controls the enabling of overlay bit plane 2. A logical zero causes bit 2 of the overlay field of the pixel to be forced to zero. A logical one causes bit 2 of the overlay field to pass to the overlay palette.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of overlay bit plane 1. A logical zero causes bit 1 of the overlay field of the pixel to be forced to zero. A logical one causes bit 1 of the overlay field to pass to the overlay palette.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of overlay bit plane 0. A logical zero causes bit 0 of the overlay field of the pixel to be forced to zero. A logical one causes bit 0 of the overlay field to pass to the overlay palette.

Internal Registers *(continued)*

Cursor MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$00	Position of the MSB of the cursor field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the cursor palette or all DAC inputs. The value specified should be less than the pixel size.

Cursor Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits ($03)–Reserved : ($FF)–Reserved	$02	Number of bits to be used for the cursor field in a pixel. The size and position of the cursor field must lie within the defined pixel size.

Cursor Blink Register

Bit(s)	Field Name	Reset Value	Field Description
7–2	Reserved	000000	Reserved for future expansion.
1, 0	Cursor Blink Enable	00	Bits 1 and 0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) cursor pixel planes 1 and 0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic.

Internal Registers *(continued)*

Cursor Display Enable Control

Bit(s)	Field Name	Reset Value	Field Description
7–2	Reserved	0000000	Reserved for future expansion.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of cursor bit plane 1. A logical zero causes bit 1 of the cursor field of the pixel to be forced to zero. A logical one causes bit 1 of the cursor field to pass to the cursor palette.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of cursor bit plane 0. A logical zero causes bit 0 of the cursor field of the pixel to be forced to zero. A logical one causes bit 0 of the cursor field to pass to the cursor palette.

Palette Bypass Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	LSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$00	Position of the LSB of the palette bypass field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to control palette bypass. The value specified should be less than the pixel size.

Palette Bypass Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–Reserved : ($FF)–Reserved	$01	Number of bits to be used for the palette bypass field in a pixel. The size and position of the palette bypass field must lie within the defined pixel size.

Internal Registers *(continued)*

Pixel Port Start Position Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Definition	Reset Value	Description
7–0	Pixel Port Start Position ($00) Bit 0 ($01) Bit 1 : ($3F) Bit 63 ($40) Bit 64 ($41) Reserved : ($FF) Reserved	$28	When MSB unpacked, this register should be loaded with the MSB + 1 of the pixel input bits to be used. When LSB unpacked, This register contains the LSB number of the pixel bits to be used. For example, if MSB unpacking is desired using bits 31–0 of the input pixel port, then this register should be loaded with $20. This register selects the starting bit position for the pixel unpacking logic.

Internal Registers *(continued)*

Pixel Format Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Definition	Reset Value	Description
7	Pixel Unpacking Order (0) MSB Unpacking (1) LSB Unpacking	0	This bit selects the pixel unpacking ordering. When pixels are MSB unpacked, the first pixel output will come from the higher-order bits of the input pixel port. When LSB is unpacked, the first pixel output will come from the lower-order bits of the input pixel port.
6	Reserved	0	Reserved for future expansion.
5	Cursor Enable (0) Disable (1) Enable	0	This bit enables the input pixel cursor field to select the cursor palette. When this bit is a logical zero, the input pixel cursor field is ignored.
4	Cursor Color 0 Enable (0) Disable (1) Enable	0	This bit enables the use of cursor color 0. When this bit is a logical zero, a cursor field value of zero causes the cursor to be transparent. When this bit is a logical one, a cursor field value of zero causes cursor color 0 to be used.
3	Overlay Enable (0) Disable (1) Enable	1	This bit enables the input pixel overlay field to select the overlay palette. When this bit is a logical zero, the input pixel overlay field is ignored.
2	Reserved	0	Reserved for future expansion.
1, 0	Palette Bypass Control (00) Always use Color Palette (01) Always bypass Color Palette (10) Use input pixel field (11) Reserved	00	This field specifies how the pixel data should address the color palette, or bypass it. If the color palette is used, a pixel will address the color palettes, and its contents would then be used as the inputs to the DACs or to drive the pixel output port. Cursor and overlays always use the color palette.

Internal Registers *(continued)*

Pixel Depth Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7–0	Pixel Depth Select ($00) Reserved ($01) 1 Bit/Pixel ($02) 2 Bits/Pixel ($03) 3 Bits/Pixel : ($1E) 30 Bits/Pixel ($1F) 31 Bits/Pixel ($20) 32 Bits/Pixel ($21) Reserved : ($FF) Reserved	$0A	These bits select the pixel depth. The total number of bits per pixel, including overlay, cursor, and unused bits in each pixel, must be specified. The reset value is consistent with the Bt458 (10 bits per pixel, 8 pseudo color plus 2 overlay).

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Pixel PLL Rate Register 0

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Reserved (logical zero)	00	Reserved.
5–0	Multiplier Selection (M) ($00) Reserved : ($17) Reserved ($18) Multiply by 24 ($19) Multiply by 25 : ($3E) Multiply by 62 ($3F) Multiply by 63	011001	Determines the multiplier factor for the input oscillator frequency (M) used in determining the final pixel clock frequency.

Internal Registers *(continued)*

Pixel PLL Rate Register 1

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Pixel Clock Divider (L) (00) Divide by 1 (01) Divide by 2 (10) Divide by 4 (11) Divide by 8	00	This bit controls the Pixel PLL divider L.
5,4	Reserved	00	Reserved.
3–0	Pixel Clock Divisor Selection (N) (0000) Reserved (0001) Reserved : (0011) Divide by 4 (0100) Divide by 5 : (1110) Divide by 15 (1111) Reserved	0100	Determines the divisor factor for the input oscillator frequency (N) used in determining the final pixel clock frequency.

Internal Registers *(continued)*

PLL Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Pixel Clock PLL Enable (0) PLL Disable (1) PLL Enable	1	This bit determines whether the PLL used to generate the pixel clock should be enabled or disabled. Should the PLL be disabled, the pixel clock must be input via the CLOCK and CLOCK*.
6	MCLK Enable (0) MCLKs Disabled (1) MCLKs Enabled	1	This bit disables the PLL used to synthesize the master clock which eventually generates the CPU clock, 20 MHz and 25 MHz clock. A logical zero written to this bit disables (i.e., three-states) PLL operation for these clocks only.
5,4	CPU Clock Selection (00) 50 MHz (01) 40 MHz (10) 33 MHz (11) 25 MHz	S(1,0)	These bits select the CPU frequency for CPUCLK output. When RESET* is active, S1 and S0 select the initial values of these two bits; when RESET* rises, these bits are latched.
3–0	VCO Gain Control (0000)–Range 0 (0001)–Range 1 (0010)–Range 2 : (0111)–Range 7 (1000)–Range 8 : (1111)–Range 15	1000	PLL VCO Gain Control.

Internal Registers *(continued)*

VIDCLK Cycle Control Register*

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Reserved	00	Reserved for future expansion.
5–0	VIDCLK Cycle Time Select	000011	These bits select the VIDCLK* cycle time in pixel clock units.
	(000000) CLOCK (000001) CLOCK/2 (000010) CLOCK/3 (000011) CLOCK/4 : (111101) CLOCK/62 (111110) CLOCK/63 (111111) CLOCK/64		

Internal Registers *(continued)*

Pixel Load Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7–5	Reserved	000	Reserved
4	SCLK* Control (0) Extra pulse not needed (1) Extra pulse needed	0	This bit specifies whether the first SCLK* pulse after a blanked time is needed (logical one) to read the first pixel item. A logical zero indicates that the system has externally provided the first VRAM shift clock, and the Bt445 may register valid pixel data with the first SCLK*.
3	SCLK* Enable (0) SCLK* Disabled (1) SCLK* Enabled	0	A logical one must be written to this bit to enable SCLK* to be output. A logical zero written to this bit three-states the SCLK* output and the system should use VIDCLK* to generate LD/SCLKI.
2	VIDCLK* Enable (0) VIDCLK* Disabled (1) VIDCLK* Enabled	1	A logical one must be written to this bit to enable VIDCLK to be output. A logical zero written to this bit three-states the VIDCLK* output.
1, 0	Reserved (logical zero)	00	Reserved.

Internal Registers *(continued)*

Digital Output Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Operating Mode (0) 4-4-4 True Color (1) 8-8-8 True Color	0	This bit selects the 4-4-4 or 8-8-8 true-color mode. When this bit is a logical zero, the 4-4-4 mode of operation is selected. In this mode the appropriate PCLK edge delivers the high-order nibble of the data being delivered to the DAC inputs. When this bit is a logical one, the 8-8-8 mode of operation is selected. In this mode the high-order nibble of each pixel is delivered on each PCLK rising edge, and the low-order nibble of each pixel is delivered on the falling edge of PCLK. In 8-8-8 mode, the PCLK edge select control is not used.
6	Reserved	0	Reserved.
5	OR, OG, OB(3–0) Output Enable (0) Disable (1) Enable	0	This bit enables the red, green, and blue digital outputs. This output should not be enabled when the pixel rate exceeds that specified by the AC timing parameters for this output. A logical zero in this bit disables (i.e., three-states) the red, green, and blue digital outputs. When three-stated, these outputs will float to valid TTL levels since internal pullup resistors are provided.
4	PVSYNC*, PHSYNC* Output Enable (0) Disable (1) Enable	0	This bit enables the separate pipelined sync outputs. A logical one enables the outputs; a logical zero causes these outputs to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.
3	PSYNC* Output Enable (0) Disable (1) Enable	0	This bit enables the pixel-synchronized, pipelined sync output signal. It may be used to generate the TTL sync signal required by monitors having separate sync. A logical one enables the output; a logical zero causes this output to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.
2	PBLANK* Output Enable (0) Disable (1) Enable	0	This bit enables the pixel-synchronized, pipelined blank output signal. A logical one enables the output; a logical zero causes this output to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.
1	PCLK Edge Select (0) Rising edge (1) Falling edge	0	This bit selects the edge of PCLK to which the digital output changes will be synchronized. A logical zero causes the AC timing parameters for the digital pixel outputs to be referenced to the rising edge of PCLK. A logical one causes the AC timing parameters for the digital pixel outputs to be referenced to the falling edge of PCLK. This bit is not used when the 8-8-8 mode of operation is selected.
0	PCLK Output Enable (0) Disable (1) Enable	0	This bit enables the PCLK output of the digital pixel output port. This output should not be enabled when the pixel rate exceeds that specified by the AC timing parameters for this output. A logical one enables the outputs; a logical zero causes this output to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.

Internal Registers *(continued)*

MPX Rate Register

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Reserved	00	Reserved for future expansion
5–0	MPX Rate ($00) 1:1 ($01) 2:1 ($02) 3:1 ($03) 4:1 : ($3E) 63:1 ($3F) 64:1	$03	Number of pixels loaded per input pixel load cycle. The value specified should be consistent with the pixel depth; i.e. the number of pixels multiplied by the pixel depth less than or equal to the number of bits for which the input port is configured.

Internal Registers *(continued)*

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt445, the value read by the MPU will be $3A. Data written to this register is ignored.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt445. The 4 most significant bits signify the revision letter, A, in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored.

Read Enable Register

Writing this Bt458-compatible register location causes the red, green, and blue read enable registers to be simultaneously written with the MPU data. Each read enable register is used to enable (logical one) or disable (logical zero) red, green, and blue planes from addressing the color palette RAM. D(7–0) correspond to bits 7–0 of the red, green, and blue fields of each pixel, respectively. Each register bit is logically ANDed with the corresponding field bit input. These registers may be written to or read by the MPU at any time and are initialized to $FF. An MPU read of this register reads the contents of the green read enable register.

Blink Enable Register

Writing this Bt458-compatible register location causes the red, green, and blue read blink registers to be simultaneously written with the MPU data. The blink enable register is used to enable (logical one) or disable (logical zero) individual bits in the red, green, and blue color fields from blinking at the blink rate and duty cycle specified by the command register. D(7–0) correspond to field bits 7–0, respectively. In order for a bit plane to blink, the corresponding bit in the read enable register must be a logical one. This register may be written to or read by the MPU at any time and is initialized to $00. An MPU read of this register reads the contents of the Green Blink Enable Register.

Signature Analysis Registers (SAR)

Signature Analysis Operation

These three 8-bit SARs may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the output SARs while BLANK* is a logical zero to load the seed value. The output SARs use data being loaded into the output DACs to calculate the signatures. JTAG logic can access the output SAR independently of the MPU operation. MPU accesses to the SARs require one address register load followed by three reads or writes to the red, green, and blue signature registers, respectively. D0 corresponds to R0, G0, and B0.

By loading a test display into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

It is imperative that the MPU adhere to conditions required to prevent the disruption of pixel data during signature acquisition to ensure consistent results. See the AC Characteristics section for further information.

Test Register 0

The test register provides Bt458-compatible diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is initialized to DAC-select equals none. When writing to the register, the upper 4 bits (D4–D7) are ignored. The contents of the test register are defined in Table 5.

To use test register 0, the host MPU writes to it, selecting the nibble and the DAC input to be read. This specifies which 4 bits of color information the MPU wishes to read (R(3–0), G(3–0), B(3–0), R(7–4), G(7–4), or B(7–4)). When the MPU reads test register 0, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits of the MPU data bus, and the lower 4 bits contain the red, green, blue, low, or high nibble selection information previously written. Note that either the pixel clock must be as slow as the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to test register 0, setting the DAC select field to 001 and the low nibble select to 0. The MPU then reads test register 0, keeping the pixel data stable, which results in D(7–4) containing the R(7–4) DAC input bits, and D(3–0) containing the red, green, blue, low, or high nibble enable information, as illustrated in Table 6.

Data Bit(s)	Field Name	Reset Value	Description
7–4	DAC Input Data	N/A	Color information at DAC input (4 bits of red, green, or blue). Data written to this field is ignored.
3	Low Nibble Select (0) High Nibble (1) Low Nibble	0	Writing a logical one to this field enables the low nibble (i.e., bits 3–0) of the selected DAC input to be read from bits 7–4 of this test register. Writing a logical zero to this field enables the high nibble (i.e., bits 7–4) of the selected DAC inputs to be read from bits 7–4 of this test register.
2–0	DAC Select (000) None (001) Red (010) Green (100) Blue All other decodes are reserved.	000	Blue enable Green enable Red enable

Table 5. Test Register 0.

MPU Bus Bits	Value Read
7–4	R(7–4)
3–0	0001

Table 6. Test Register 0 Example.

Internal Registers *(continued)*

The comparator, which may be accessed in Test Register 1 (see Table 7), enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional. When the monitor is not connected or one of the analog cables connecting the monitor is open (i.e., broken), the voltage present at the corresponding DAC output would be higher than predicted, as one of the termination resistors would not be present.

Bit(s)	Field Name	Reset Value	Description
7, 6	Operand 1 Select (00) Normal Operation (01) Select Green DAC Output (10) Select Red DAC Output (11) Reserved	00	This field selects Operand 1 of the comparator. For normal operation, the operand 1 and 2 fields should both contain 00.
5, 4	Operand 2 Select (00) Normal Operation (01) Select 145 mV Reference (10) Select Blue DAC Output (11) Reserved	00	This field selects Operand 2 of the comparator. For normal operation, the operand 1 and 2 fields should both contain 00.
3	Comparison Result (0) Operand 1 < Operand 2 (1) Operand 1 > Operand 2	N/A	This field yields the result of the comparison of the DAC and/or reference output. Comparing operands whose values lie within a few LSBs will yield unpredictable results. Data written to this bit is ignored, as this field is read only. This result is valid only after the required comparison settling time is reached (i.e., 5 µs after the operand becomes constant).
2–0	Reserved	000	Reserved.

Table 7. Test Register 1.

Pin Descriptions

Pin Count	Pin Name	Description
1	BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as illustrated in Tables 2 and 3. It is registered on the rising edge of LD. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
1	SYNC*/ HSYNC*	Composite sync/Hsync control input (TTL compatible). A logical zero on this input switches off an IRE current source on the IOG output (see Figures 6 and 7). SYNC*/ HSYNC* does not override any other control or data input, as shown in Tables 2 and 3; therefore, it should be asserted only during the blanking interval. It is registered on the rising edge of VIDCLKI. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
1	VSYNC*	Separate sync control inputs (TTL compatible). This signal is registered with each rising edge of VIDCLKI and is pipelined to the pixel data rate, then output with pixel timing to the PVSYNC* outputs. This signal is not internally used by the Bt445.
1	VIDCLKI	Video Clock input (TTL-compatible Schmitt Trigger). The rising edge of this input is used to load the SYNC* and BLANK* control inputs. Also, if SCLK* is not used to control the VRAM frame buffer, pixel inputs (P0–P47) are also loaded with the rising edge of this signal. This input is usually driven with a system-buffered/skewed version of the VIDCLK* output.
1	LD/SCLKI	Load Serial Clock Input (TTL-compatible Schmitt Trigger). This signal is used only when the Bt445 is configured to provide the VRAM serial clock (SCLK*) output. Pixel data is loaded on the rising edge of this signal, except for the first rising edge, which occurs during blanking. This input is usually driven with a system-buffered/skewed version of either the SCLK* output or VIDCLK*.
64	P(63–0)	Pixel Inputs Port (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM, 16 entries of the overlay palette, or 4 entries of cursor palette is to be used to provide color information. Depending on the pixel configuration, up to 64 consecutive pixels per load cycle are input through this port. They are registered on the rising edge of VIDCLKI or LD/SCLKI. These inputs have internal pullup resistors; therefore, unused pins do not require connection. However, if the system configuration allows, the unused pins should be connected to GND.
2	S(1, 0)	CPU Clock Rate Select Switch (TTL compatible). These inputs are used to set the initial CPU clock rate at reset time.
3	IOR, IOG, IOB	Red, green, and blue video current outputs. These high-impedance current sources are capable of directly driving a doubly-terminated 75-Ω coaxial cable (Figure 12).
1	SCLK*	VRAM shift clock output (TTL-voltage-level compatible, low drive). The signal on this pin is equal to the selected pixel clock divided by 1, 2, 4, 8, or 32 depending on the pixel depth selected. This clock must be redriven through an inverting buffer prior to the connection to the serial clock of the VRAMs.
1	VIDCLK*	Video Clock Output (TTL-voltage-level compatible, low drive). This output is a divided pixel as programmed in the VIDCLK* Cycle Control register. This clock must be redriven through an inverting buffer prior to the connection to the CRT timing generation logic.

Pin Descriptions *(continued)*

Pin Count	Pin Name	Description
1	PCLK	Pixel Clock (TTL-voltage-level compatible, low drive). This clock is used to synchronize the next stage with the digital outputs. It must be redriven through a noninverting buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 55 MHz driving a 20 pF load.
1	PSYNC*	Composite SYNC control output (TTL-voltage-level compatible, low drive). This signal is synchronized with the pixel outputs.
2	PHSYNC*, PVSYNC*	Separate SYNC control outputs (TTL-voltage-level compatible, low drive). These signals are synchronized with the pixel outputs.
1	PBLANK*	Composite BLANK control output (TTL-voltage-level compatible, low drive). This signal is synchronized with the pixel outputs.
12	OR (3–0) OG (3–0) OB (3–0)	Digital Outputs (TTL-voltage-level compatible, low drive). These low-drive outputs represent the 4 MSBs of the red, green, and blue DAC decoder and can be used to drive an active matrix TFT directly. These outputs must be redriven through a noninverting buffer prior to the connection to the next stage.
1	CPUCLK	CPU Clock (TTL-voltage-level compatible, low drive). This clock is used to derive the CPU clock and is selectable between 50, 40, 33, and 25 MHz (when using a 20 MHz crystal). This clock must be redriven through a buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 50 MHz driving a 20 pF load.
1	MCLK20	20 MHz Master Clock (TTL-voltage-level compatible, low drive). This master clock generates a constant 20 MHz clock. This clock must be redriven through a buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 50 MHz driving a 20 pF load.
1	MCLK25	25 MHz Master Clock (TTL-voltage-level compatible, low drive). This master clock generates a constant 25 MHz clock. This clock must be redriven through a buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 50 MHz driving a 20 pF load.
1	TMS	Test Mode Select (TTL compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When not performing JTAG operations, this pin should be driven to a logic high.
1	TCK	Test Clock (TTL compatible). Used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When not performing JTAG operations, this pin should be driven to a logic high.
1	TDI	Test Data In (TTL compatible). JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When not performing JTAG operations, this pin should be driven to a logic high.
1	TDO	Test Data Out (TTL compatible). JTAG output used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences, and will be three-stated at all other times. When not performing JTAG operations, this pin should be left floating.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Count</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>2</td><td>COMP, COMP2</td><td>Compensation pins. These pins provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between these two pins (Figure 13).</td></tr>
<tr><td>1</td><td>FS ADJUST</td><td>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 13). Note that the IRE relationships in Figures 6 and 7 are maintained, regardless of the full-scale output current.
The relationship between RSET and the full-scale output current on IOG is:
RSET (Ω) = K1 * VREF (V) / IOG (mA)
The full-scale output current on IOR and IOB for a given RSET is:
IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)
where K1 and K2 are defined as:
<table>
<tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr>
<tr><td>7.5 IRE</td><td>K1 = 11,294</td><td>K2 = 8,067</td></tr>
<tr><td>0 IRE</td><td>K1 = 10,684</td><td>K2 = 7,457</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>VREF</td><td>Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 13. The decoupling capacitor must be as close as possible to the device to keep lead lengths to an absolute minimum.</td></tr>
<tr><td>2</td><td>CLOCK, CLOCK*</td><td>Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.</td></tr>
<tr><td>1</td><td>XTAL1</td><td>Crystal input. This input is either connected to a crystal or driven by a CMOS oscillator. The internal phase lock loops generate the pixel and CPU clocks using this input.</td></tr>
<tr><td>1</td><td>XTAL2</td><td>Crystal amplifier output. This output is connected to the second terminal of the crystal when used.</td></tr>
<tr><td>1</td><td>CE*</td><td>Chip enable control input (TTL-compatible Schmitt Trigger). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally registered on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.</td></tr>
<tr><td>1</td><td>R/W</td><td>Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is registered on the falling edge of CE*.</td></tr>
<tr><td>3</td><td>C(2–0)</td><td>Command control inputs (TTL compatible). C2, C1, and C0 specify the type of read or write operation being performed, as illustrated in Table 1. They are registered with the falling edge of CE*.</td></tr>
</table>

Pin Descriptions *(continued)*

8	D(7–0)	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
1	RANGE	Compensation for VCO. A 0.01 µF ceramic chip capacitor must be connected between this pin and VAA (Figure 13).
1	RESET*	Reset input (TTL compatible). When this signal is asserted, all the Command Register Bits are set to be in a Bt458-compatible mode.
7	NC	No Connect. Reserved for future expansion. These pins should be left open.
19	VAA	Analog power. All VAA pins must be connected.
11	GND	Analog ground. All GND pins must be connected.

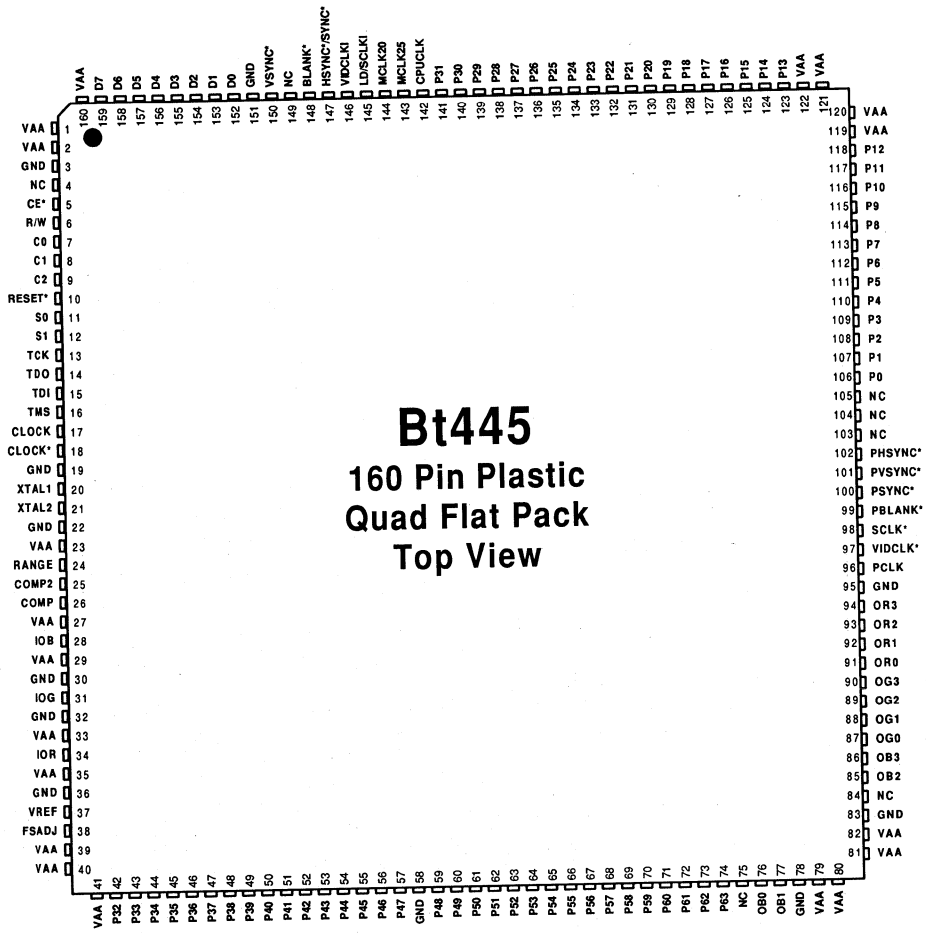


Figure 11. 160-pin PQFP Pin Assignments.

Pin Descriptions *(continued)*

Signal	Pin Number
BLANK*	148
SYNC*/HSYNC*	147
VSYNC*	150
NC	149
CLOCK*	18
CLOCK	17
XTAL1	20
XTAL2	21
RANGE	24
S0	11
S1	12
RESET*	10
CPUCLK	142
MCLK20	144
MCLK25	143
SCLK*	98
VIDCLK*	97
VIDCLKI	146
LD/SCLKI	145
P0	106
P1	107
P2	108
P3	109
P4	110
P5	111
P6	112
P7	113
P8	114
P9	115
P10	116
P11	117
P12	118
P13	123
P14	124
P15	125
P16	126
P17	127
P18	128
P19	129
P20	130
P21	131
P22	132
P23	133
P24	134

Signal	Pin Number
P25	135
P26	136
P27	137
P28	138
P29	139
P30	140
P31	141
P32	42
P33	43
P34	44
P35	45
P36	46
P37	47
P38	48
P39	49
P40	50
P41	51
P42	52
P43	53
P44	54
P45	55
P46	56
P47	57
P48	59
P49	60
P50	61
P5	62
P52	63
P53	64
P54	65
P55	66
P56	67
P57	68
P58	69
P59	70
P60	71
P61	72
P62	73
P63	74
VAA	1
VAA	2
VAA	23
VAA	27
VAA	29
VAA	33
VAA	35

Signal	Pin Number
VAA	39
VAA	40
VAA	41
VAA	79
VAA	80
VAA	81
VAA	82
VAA	119
VAA	120
VAA	121
VAA	122
VAA	160
GND	3
GND	19
GND	22
GND	30
GND	32
GND	36
GND	58
GND	78
GND	83
GND	95
GND	151
NC	4
NC	75
NC	84
NC	103
NC	104
NC	105
PCLK	96
PBLANK*	99
PSYNC*	100
PVSYNC*	101
PHSYNC*	102
OR0	91
OR1	92
OR2	93
OR3	94
OG0	87
OG1	88
OG2	89
OG3	90

Signal	Pin Number
OB0	76
OB1	77
OB2	85
OB3	86
IOR	34
IOG	31
IOB	28
COMP	26
COMP2	25
FS ADJUST	38
VREF	37
CE*	5
R/W	6
C2	9
C1	8
C0	7
D7	159
D6	158
D5	157
D4	156
D3	155
D2	154
D1	153
D0	152
TMS	16
TCK	13
TDI	15
TDO	14

5

PC Board Layout Considerations

PC Board Considerations

The Bt445 layout should be optimized for lowest noise on the Bt445 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground planes must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferable analog ground plane), layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt445 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8" wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 12.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 13 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is less than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt445 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

PC Board Layout Considerations *(continued)*

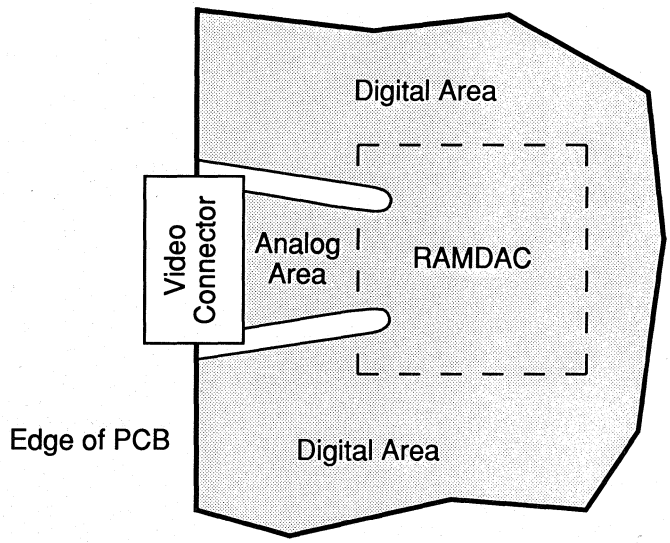


Figure 12. Representative Power/Ground Analog Area Layout

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must have adequate decoupling to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt445 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

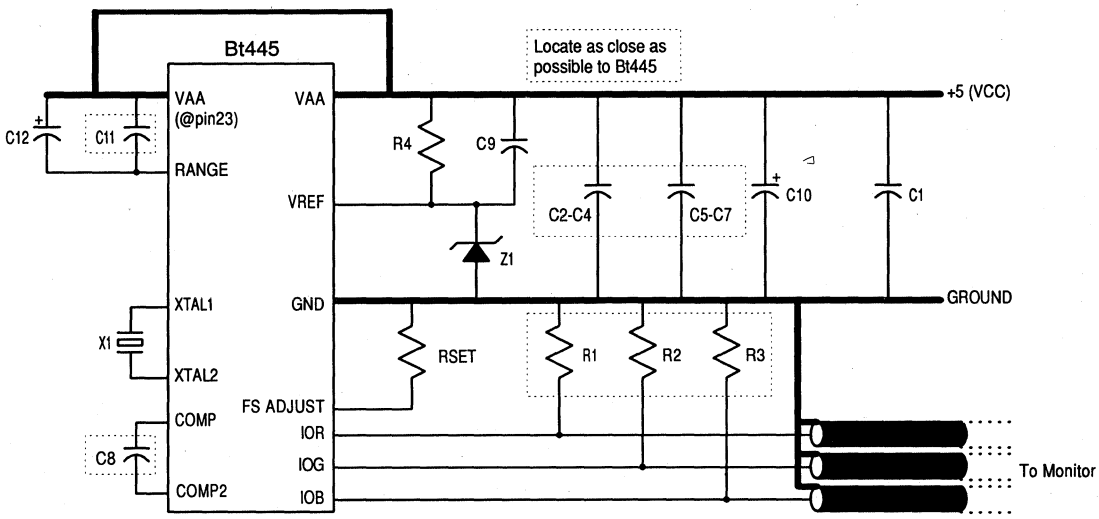
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

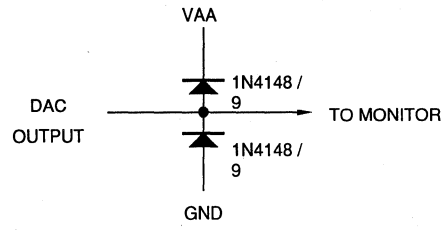
Analog Output Protection

The Bt445 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*





Diode Protection Circuit

Location	Description	Vendor Part Number
C1–C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7, C11	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
C12	4.7 µF tantalum capacitor	tbd
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
X1	20 MHz crystal	tbd
Z1	1.2 Vvoltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt445.

Figure 13. Typical Connection Diagram and Parts List.

Applications Information

Test Features of the Bt445

The Bt445 contains a dedicated test register and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Register

When enabled, the output signature registers operate with the 24 bits of data that are presented to the DAC inputs. These 24-bit vectors represent a single pixel-color, and are presented as inputs simultaneously to the red, green, and blue SARs, as well as the three on-chip DACs.

The SARs act as a wide linear feedback shift register on each succeeding DAC input. It is important to note that in all the multiplexed modes the SARs register every pixel.

The Bt445 will only generate signatures while in active-display (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt445 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 24 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream will be input to the chip, for example, one scan-line or one frame buffer of pixels. Then, at the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay, cursor, and palette bypass data validity is also tested using the signature registers.

It is not simple to describe algorithmically the specific linear feedback shift operation used in the Bt445. The linear feedback configuration are shown in Figure 14.

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel streamfed to the SARs.

When performing system tests that use the signature analysis registers, it is recommended that the pipeline delay be reset prior to the test to provide optimal allowance for input clock drift. This prevents the disruption of pixel data because of pipeline auto-reset, which may occur as the phase relation of the input clock drifts, with respect to the output clocks. Excessive input clock drift may require that signatures be acquired over shorter periods when the maximum drift may be more tightly controlled. This is especially recommended during environmental and power supply variation testing.

Analog Comparator

The other dedicated test structure in the Bt445 is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register. The capture occurs over one LD/SCLKI period set by a logical one at pin P31.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Applications Information *(continued)*

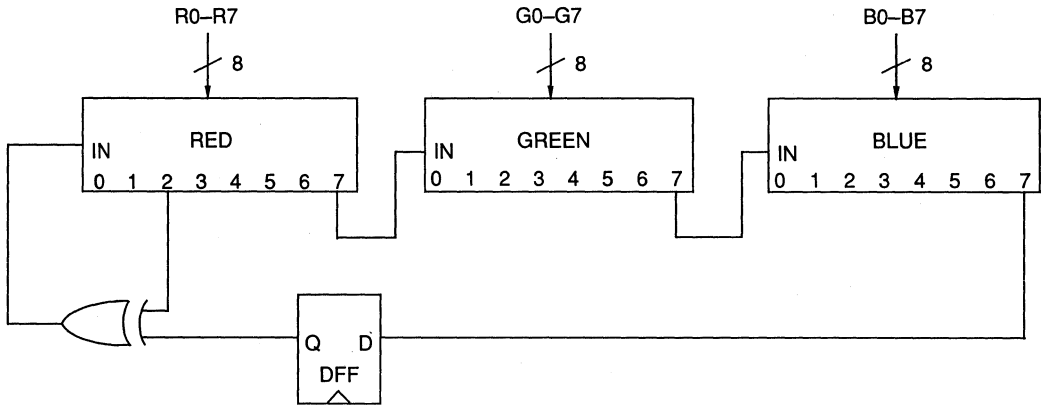


Figure 14. Signature Analysis Register Circuit.

Applications Information *(continued)*

Initializing the Bt445

Following the assertion of the reset signal, the Bt445 pixel unpacking logic and pixel formatting logic are initialized to the Bt458 4:1 MPX mode of operation. See Table 8.

Control Register	Value	Description
Pixel Port Start Position	40	4 pixels, each with 8-bit pseudo color and 2-bit overlay.
Pixel Depth	10	8-bit pseudo color and 2-bit overlay.
Pixel Multiplex Rate	4	4:1 Multiplexed.
Red, Green, Blue Shift	$00	8-bit pseudo-color sources Red, Green, and Blue from same field starting from low-order bit of pixel.
Red, Green, Blue Width	$08	
Red, Green, Blue Enable	$FF	All planes used.
Red, Green, Blue Blink	$00	Pixel blinking disabled.
Overlay Shift	$08	Overlay comes in on next high-order pixels above 8-bit pseudo-color bits.
Overlay Width	2	2-bit overlay supported in Bt458.
Overlay Enable	$03	Bit planes 0 and 1 enabled.
Overlay Blink	$00	Overlay blinking disabled.

Table 8. Reset Initialization.

Applications Information *(continued)*

Color Palette Initialization

Table 9 shows the sequence of MPU writes required to load the color palette entries:

Operation	Description	C(2–0)	Internal Address Register	MPU Data
Color Palette RAM Initialization	Write $00 to address register	000	–	$00
	Write red data to RAM (location $00)	001	$00	$rr
	Write green data to RAM (location $00)	001	$00	$gg
	Write blue data to RAM (location $00)	001	$00	$bb
	Write red data to RAM (location $01)	001	$01	$rr
	Write green data to RAM (location $01)	001	$01	$gg
	Write blue data to RAM (location $01)	010	$01	$bb
	:	:	:	:
	Write red data to RAM (location $FF)	001	$FF	$rr
	Write green data to RAM (location $FF)	001	$FF	$gg
	Write blue data to RAM (location $FF)	001	$FF	$bb
Overlay Color Palette Initialization	Write $00 to address register	000	–	$00
	Write red data to overlay (location $0)	011	$00	$rr
	Write green data to overlay (location $0)	011	$00	$gg
	Write blue data to overlay (location $0)	011	$00	$bb
	Write red data to overlay (location $1)	011	$01	$rr
	Write green data to overlay (location $1)	011	$01	$gg
	Write blue data to overlay (location $1)	011	$01	$bb
	:	:	:	:
	Write red data to overlay (location $F)	011	$0F	$rr
	Write green data to overlay (location $F)	011	$0F	$gg
	Write blue data to overlay (location $F)	011	$0F	$bb
Cursor Palette Initialization	Write $00 to address register	000	–	$00
	Write red data to cursor (location $0)	111	$00	$rr
	Write green data to cursor (location $0)	111	$00	$gg
	Write blue data to cursor (location $0)	111	$00	$bb
	Write red data to cursor (location $1)	111	$01	$rr
	Write green data to cursor (location $1)	111	$01	$gg
	Write blue data to cursor (location $1)	111	$01	$bb
	:	:	:	:
	Write red data to cursor (location $3)	111	$03	$rr
	Write green data to cursor (location $3)	111	$03	$gg
	Write blue data to cursor (location $3)	111	$03	$bb

Table 9. Color Palette Initialization.

Applications Information *(continued)*

Pipeline Delay Initialization

The Bt445 employs a variable pipeline delay to allow for easier system implementation. This scheme allows the LD/SCLKI and VIDCLKI signals to drift relative to the pixel clock (as would occur with varying environmental conditions such as warm-up and power supply fluctuations) without corrupting the output pixel data stream. The amount of allowable drift depends on the MPX Rate; for example, in a 4:1 MPX mode, the drift window is slightly less than 4 pixel clock cycles. This compares favorably with fixed-pipeline delay devices where the drift is necessarily less than one pixel clock to the point of pixel loss or duplication.

For optimum performance, the pipeline depth should be initialized away from the extremes of the drift window to allow for subsequent drift. This is accomplished by the transition of the RESET* signal from 0 to 1 or under the MPU's control by the transition of the RESET PIPELINE field in the Pixel Format Control Register from 0 to 1. The MPU should reset the pipeline whenever any of the following registers or fields are changed: the Pixel Port Start Position Register, the Pixel Unpacking Order Field, the MPX Rate Register, the Pixel Depth Control Register, the PLL Rate Registers, the Pixel Clock PLL Enable Field, The VCO Gain Control Field, or the SCLK* Enable field.

Additionally, when changing any controls affecting the pixel PLL rate or VCO gain, sufficient time should be allowed for the PLL to stabilize to the new rate prior to the MPU issuing the pipeline delay initialization.

Table 10 illustrates the allowable drift windows for LD/SCLKI relative to the pipeline depth initialization time for the various MPX modes.

PLL Initialization

Crystal Frequency Selection

The crystal frequency should be selected based on the required pixel rate(s), the display pixel rate tolerance, and the required system clock outputs. When using the Bt445-generated system clocks, because the system clock ratios are fixed, the crystal reference frequency is usually dictated by required system clock rates. The desired ratio for the PLL can then be computed by dividing required the pixel rate by the crystal frequency, looking up the M and N values in the ratio table for the closest ratio, and ensuring that the display can still satisfactorily operate within the best-fit pixel rate and associated CRT timings.

Ratio Selection

The PLL clock ratio is set by programming the M and N values through the MPU port. Reset M and N values are $18 and $04, respectively, yielding a pixel rate of 5 times the crystal reference.

Table 11 shows the complete range of M/N ratios for M ranges from 25–64 and N ranges from 4–15 and L = 1, for 20.0 and 14.318 MHz crystals.

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MPX Rate(s)	Minimum	Maximum	Units
1:1	0	0	Pixel Clocks
2:1	–1	+1	
3:1	–1	+2	
4:1	–2	+2	
5:1	–2	+3	
:	:	:	
63:1	–2	+61	
64:1	–2	+62	

External stopping of the CLOCK and CLOCK* signals is not required for pipeline delay initialization.

Table 10. Allowable LD/SCLKI Drift.

Applications Information *(continued)*

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
3.250	26	8	65.00	N/A	tbd
3.267	49	15	65.33	N/A	tbd
3.273	36	11	65.45	N/A	tbd
3.286	46	14	65.71	N/A	tbd
3.300	33	10	66.00	N/A	tbd
3.308	43	13	66.15	N/A	tbd
3.333	30	9	66.67	N/A	tbd
3.357	47	14	67.14	N/A	tbd
3.364	37	11	67.27	N/A	tbd
3.375	27	8	67.50	N/A	tbd
3.385	44	13	67.69	N/A	tbd
3.400	34	10	68.00	N/A	tbd
3.417	41	12	68.33	N/A	tbd
3.429	48	14	68.57	N/A	tbd
3.444	31	9	68.89	N/A	tbd
3.455	38	11	69.09	N/A	tbd
3.462	45	13	69.23	N/A	tbd
3.467	52	15	69.33	N/A	tbd
3.500	28	8	70.00	N/A	tbd
3.533	53	15	70.67	N/A	tbd
3.538	46	13	70.77	N/A	tbd
3.545	39	11	70.91	N/A	tbd
3.556	32	9	71.11	N/A	tbd
3.571	25	7	71.43	N/A	tbd
3.583	43	12	71.67	N/A	tbd
3.600	36	10	72.00	N/A	tbd
3.615	47	13	72.31	N/A	tbd
3.625	29	8	72.50	N/A	tbd
3.636	40	11	72.73	N/A	tbd
3.643	51	14	72.86	N/A	tbd
3.667	33	9	73.33	N/A	tbd
3.692	48	13	73.85	N/A	tbd
3.700	37	10	74.00	N/A	tbd
3.714	26	7	74.29	N/A	tbd
3.727	41	11	74.55	N/A	tbd
3.733	56	15	74.67	N/A	tbd
3.750	30	8	75.00	N/A	tbd
3.769	49	13	75.38	N/A	tbd
3.778	34	9	75.56	N/A	tbd
3.786	53	14	75.71	N/A	tbd
3.800	38	10	76.00	N/A	tbd
3.818	42	11	76.36	N/A	tbd
3.833	46	12	76.67	N/A	tbd
3.846	50	13	76.92	N/A	tbd
3.857	27	7	77.14	N/A	tbd
3.867	58	15	77.33	N/A	tbd
3.875	31	8	77.50	N/A	tbd
3.889	35	9	77.78	N/A	tbd
3.900	39	10	78.00	N/A	tbd

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
3.909	43	11	78.18	N/A	tbd
3.917	47	12	78.33	N/A	tbd
3.923	51	13	78.46	N/A	tbd
3.929	55	14	78.57	N/A	tbd
3.933	59	15	78.67	N/A	tbd
4.000	28	7	80.00	N/A	tbd
4.067	61	15	81.33	N/A	tbd
4.071	57	14	81.43	N/A	tbd
4.077	53	13	81.54	N/A	tbd
4.083	49	12	81.67	N/A	tbd
4.091	45	11	81.82	N/A	tbd
4.100	41	10	82.00	N/A	tbd
4.111	37	9	82.22	N/A	tbd
4.125	33	8	82.50	N/A	tbd
4.133	62	15	82.67	N/A	tbd
4.143	29	7	82.86	N/A	tbd
4.154	54	13	83.08	N/A	tbd
4.167	25	6	83.33	N/A	tbd
4.182	46	11	83.64	N/A	tbd
4.200	42	10	84.00	N/A	tbd
4.214	59	14	84.29	N/A	tbd
4.222	38	9	84.44	N/A	tbd
4.231	55	13	84.62	N/A	tbd
4.250	34	8	85.00	N/A	tbd
4.267	64	15	85.33	N/A	tbd
4.273	47	11	85.45	N/A	tbd
4.286	30	7	85.71	N/A	tbd
4.300	43	10	86.00	N/A	tbd
4.308	56	13	86.15	N/A	tbd
4.333	26	6	86.67	N/A	tbd
4.357	61	14	87.14	N/A	tbd
4.364	48	11	87.27	N/A	tbd
4.375	35	8	87.50	N/A	tbd
4.385	57	13	87.69	N/A	tbd
4.400	44	10	88.00	N/A	tbd
4.417	53	12	88.33	N/A	tbd
4.429	31	7	88.57	N/A	tbd
4.444	40	9	88.89	N/A	tbd
4.455	49	11	89.09	N/A	tbd
4.462	58	13	89.23	N/A	tbd
4.500	27	6	90.00	N/A	tbd
4.538	59	13	90.77	N/A	tbd
4.545	50	11	90.91	65.08	tbd
4.556	41	9	91.11	65.23	tbd
4.571	32	7	91.43	65.45	tbd
4.583	55	12	91.67	65.62	tbd
4.600	46	10	92.00	65.86	tbd
4.615	60	13	92.31	66.08	tbd
4.625	37	8	92.50	66.22	tbd

Table 11. Sample Pixel Clock Rates.

Applications Information *(continued)*

Reference Frequence:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
4.636	51	11	92.73	66.38	tbd
4.667	28	6	93.33	66.82	tbd
4.692	61	13	93.85	67.19	tbd
4.700	47	10	94.00	67.30	tbd
4.714	33	7	94.29	67.50	tbd
4.727	52	11	94.55	67.69	tbd
4.750	38	8	95.00	68.01	tbd
4.769	62	13	95.38	68.29	tbd
4.778	43	9	95.56	68.41	tbd
4.800	48	10	96.00	68.73	tbd
4.818	53	11	96.36	68.99	tbd
4.833	29	6	96.67	69.20	tbd
4.846	63	13	96.92	69.39	tbd
4.857	34	7	97.14	69.55	tbd
4.875	39	8	97.50	69.80	tbd
4.889	44	9	97.78	70.00	tbd
4.900	49	10	98.00	70.16	tbd
4.909	54	11	98.18	70.29	tbd
4.917	59	12	98.33	70.40	tbd
4.923	64	13	98.46	70.49	tbd
5.000	25	5	100.00	71.59	tbd
5.083	61	12	101.67	72.78	tbd
5.091	56	11	101.82	72.89	tbd
5.100	51	10	102.00	73.02	tbd
5.111	46	9	102.22	73.18	tbd
5.125	41	8	102.50	73.38	tbd
5.143	36	7	102.86	73.64	tbd
5.167	31	6	103.33	73.98	tbd
5.182	57	11	103.64	74.19	tbd
5.200	26	5	104.00	74.45	tbd
5.222	47	9	104.44	74.77	tbd
5.250	42	8	105.00	75.17	tbd
5.273	58	11	105.45	75.50	tbd
5.286	37	7	105.71	75.68	tbd
5.300	53	10	106.00	75.89	tbd
5.333	32	6	106.67	76.36	tbd
5.364	59	11	107.27	76.80	tbd
5.375	43	8	107.50	76.96	tbd
5.400	27	5	108.00	77.32	tbd
5.429	38	7	108.57	77.73	tbd
5.444	49	9	108.89	77.95	tbd
5.455	60	11	109.09	78.10	tbd
5.500	33	6	110.00	78.75	tbd
5.545	61	11	110.91	79.40	tbd
5.556	50	9	111.11	79.55	tbd
5.571	39	7	111.43	79.77	tbd
5.600	28	5	112.00	80.18	tbd
5.625	45	8	112.50	80.54	tbd
5.636	62	11	112.73	80.70	tbd

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
5.667	34	6	113.33	81.14	tbd
5.700	57	10	114.00	81.61	tbd
5.714	40	7	114.29	81.82	tbd
5.727	63	11	114.55	82.00	tbd
5.750	46	8	115.00	82.33	tbd
5.778	52	9	115.56	82.73	tbd
5.800	29	5	116.00	83.05	tbd
5.818	64	11	116.36	83.31	tbd
5.833	35	6	116.67	83.52	tbd
5.857	41	7	117.14	83.86	tbd
5.875	47	8	117.50	84.12	tbd
5.889	53	9	117.78	84.32	tbd
5.900	59	10	118.00	84.48	tbd
6.000	30	5	120.00	85.91	tbd
6.100	61	10	122.00	87.34	tbd
6.111	55	9	122.22	87.50	tbd
6.125	49	8	122.50	87.70	tbd
6.143	43	7	122.86	87.95	tbd
6.167	37	6	123.33	88.30	tbd
6.200	31	5	124.00	88.77	tbd
6.222	56	9	124.44	89.09	tbd
6.250	25	4	125.00	89.49	tbd
6.286	44	7	125.71	90.00	tbd
6.300	63	10	126.00	90.20	tbd
6.333	38	6	126.67	90.68	tbd
6.375	51	8	127.50	91.28	tbd
6.400	32	5	128.00	91.64	tbd
6.429	45	7	128.57	92.05	tbd
6.444	58	9	128.89	92.27	tbd
6.500	26	4	130.00	93.07	tbd
6.556	59	9	131.11	93.86	tbd
6.571	46	7	131.43	94.09	tbd
6.600	33	5	132.00	94.50	tbd
6.625	53	8	132.50	94.86	tbd
6.667	40	6	133.33	95.45	tbd
6.714	47	7	134.29	96.14	tbd
6.750	27	4	N/A	96.65	tbd
6.778	61	9	N/A	97.05	tbd
6.800	34	5	N/A	97.36	tbd
6.833	41	6	N/A	97.84	tbd
6.857	48	7	N/A	98.18	tbd
6.875	55	8	N/A	98.44	tbd
6.889	62	9	N/A	98.64	tbd
7.000	28	4	N/A	100.23	tbd
7.111	64	9	N/A	101.82	tbd
7.125	57	8	N/A	102.02	tbd
7.143	50	7	N/A	102.27	tbd
7.167	43	6	N/A	102.61	tbd
7.200	36	5	N/A	103.09	tbd

Table 11 (continued). Sample Pixel Clock Rates.

Applications Information *(continued)*

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
7.250	29	4	N/A	103.81	tbd
7.286	51	7	N/A	104.32	tbd
7.333	44	6	N/A	105.00	tbd
7.375	59	8	N/A	105.60	tbd
7.400	37	5	N/A	105.95	tbd
7.429	52	7	N/A	106.36	tbd
7.500	30	4	N/A	107.39	tbd
7.571	53	7	N/A	108.41	tbd
7.600	38	5	N/A	108.82	tbd
7.625	61	8	N/A	109.18	tbd
7.667	46	6	N/A	109.77	tbd
7.714	54	7	N/A	110.45	tbd
7.750	31	4	N/A	110.97	tbd
7.800	39	5	N/A	111.68	tbd
7.833	47	6	N/A	112.16	tbd
7.857	55	7	N/A	112.50	tbd
7.875	63	8	N/A	112.76	tbd
8.000	32	4	N/A	114.55	tbd
8.143	57	7	N/A	116.59	tbd
8.167	49	6	N/A	116.93	tbd
8.200	41	5	N/A	117.41	tbd

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
8.250	33	4	N/A	118.12	tbd
8.286	58	7	N/A	118.64	tbd
8.333	50	6	N/A	119.32	tbd
8.400	42	5	N/A	120.27	tbd
8.429	59	7	N/A	120.68	tbd
8.500	34	4	N/A	121.70	tbd
8.571	60	7	N/A	122.73	tbd
8.600	43	5	N/A	123.14	tbd
8.667	52	6	N/A	124.09	tbd
8.714	61	7	N/A	124.77	tbd
8.750	35	4	N/A	125.28	tbd
8.800	44	5	N/A	126.00	tbd
8.833	53	6	N/A	126.48	tbd
8.857	62	7	N/A	126.82	tbd
9.000	36	4	N/A	128.86	tbd
9.143	64	7	N/A	130.91	tbd
9.167	55	6	N/A	131.25	tbd
9.200	46	5	N/A	131.73	tbd
9.250	37	4	N/A	132.44	tbd
9.333	56	6	N/A	133.64	tbd
9.400	47	5	N/A	134.59	tbd

Table 11 (continued). Sample Pixel Clock Rates.

Note: All Pixel Clock frequencies shown are prior to the "L" divider section. All of the listed frequencies may be divided by 1, 2, 4, or 8 to provide lower pixel clock rates.

Applications Information *(continued)*

Frame Buffer Interface Configurations

The Bt445 may be operated with an internal PLL or an external clock generator. Additionally, the Bt445 may be used to generate the VRAM serial shift clock signal, or this signal may be generated externally. The following figures show examples of the frame buffer interface when using the Bt445 in various modes.

Externally Generated Pixel Clock with Externally Generated VRAM Serial Shift Clock

In this configuration, neither the SCLK* nor VIDCLK* outputs of the Bt445 are used, and thus they should be disabled via the command registers. The pixel clock, load clock, and VRAM serial shift clock are externally generated by a device such as the Bt438 or Bt440. Figure 15 illustrates this configuration.

The multiplex rates supported are limited by the modes for which the external clock divider (i.e., the Bt440 in this case) can be configured. The SYNC* and BLANK* information loaded correspond to the pixel data loaded on the same LD clock rising edge. The maximum pixel clock rate is 150 MHz.

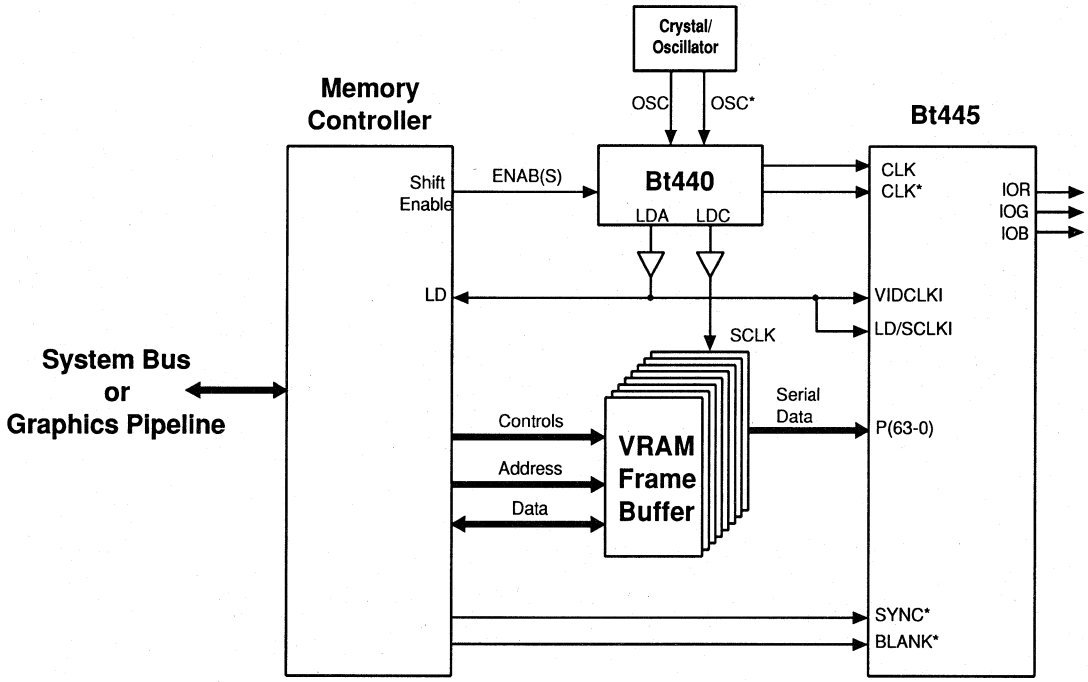

Figure 15. Frame Buffer Interface, External Pixel Clock, and Serial Clock Generation.

Applications Information *(continued)*

PLL-Generated Pixel Clock with Externally Generated VRAM Shift Clock

In this configuration, the Bt445 generates the pixel clock internally from the M and N values contained in the control registers. The VRAM shift clock is still externally generated, but the system must use the Bt445's VIDCLK* output, as there is no other system reference that is phase related to the pixel clock. The memory controller produces a clock gate signal for generating the VRAM shift clock from VIDCLK*. Figure 16 illustrates this configuration.

The inverting drivers used to generate LD/SCLKI and the VRAM shift clock should ideally have correlated delays and high-impedance, low capacitance inputs.

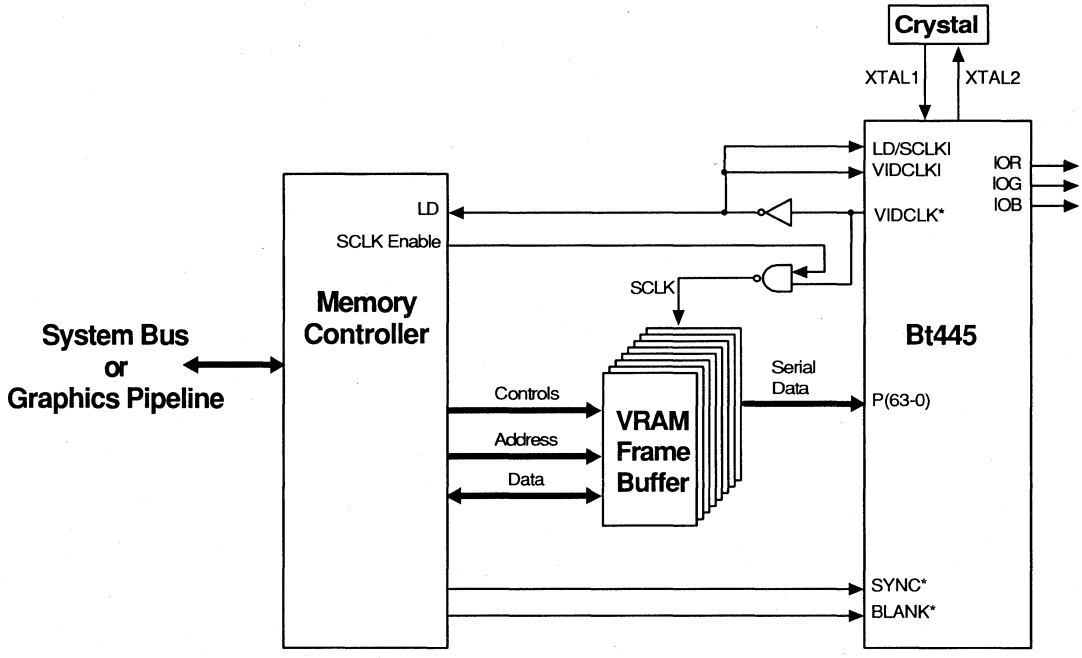

Figure 16. Frame Buffer Interface, with PLL Pixel Clock and no Bt445-Provided Shift Clock.

Bt445-Generated VRAM Shift Clock, Externally-Generated Pixel Clock

In this configuration, the pixel clock is generated in an external oscillator. The Bt445 provides two clocks to the system: VIDCLK* and SCLK*. VIDCLK* is always free running and is used to control the CRT timing generator, usually part of the controller. VIDCLKI is used to register the SYNC*, and BLANK* signals. LD/SCLKI is used to register the pixel data. Figure 17 illustrates this configuration.

SCLK* is asserted as needed to shift out pixel data from the VRAMs, according to the MPX rate specified by a control register. Generally, VIDCLK* and SCLK* do not run at the same rate; hence, the granularity with which SYNC* and BLANK* are specified is not the same as the MPX rate. As a result, the last group of pixels loaded with LD/SCLKI at the end of an active scan line, may not all be displayed. It should be noted that in this configuration, the SYNC* and BLANK* information does not correlate to the data on the Bt445's pixel input port; however, the Bt445 internally aligns the CRT timing controls with the pixel data for output. Also, the buffer delays for VIDCLK* and SCLK* need not be correlated.

The SCLK control signal supplied by the memory controller is used only to insert shift clocks for the purpose of loading the shift register tap address required by VRAMs supporting split-shift register operations.

The pixel rate in this configuration may be up to 150 MHz.

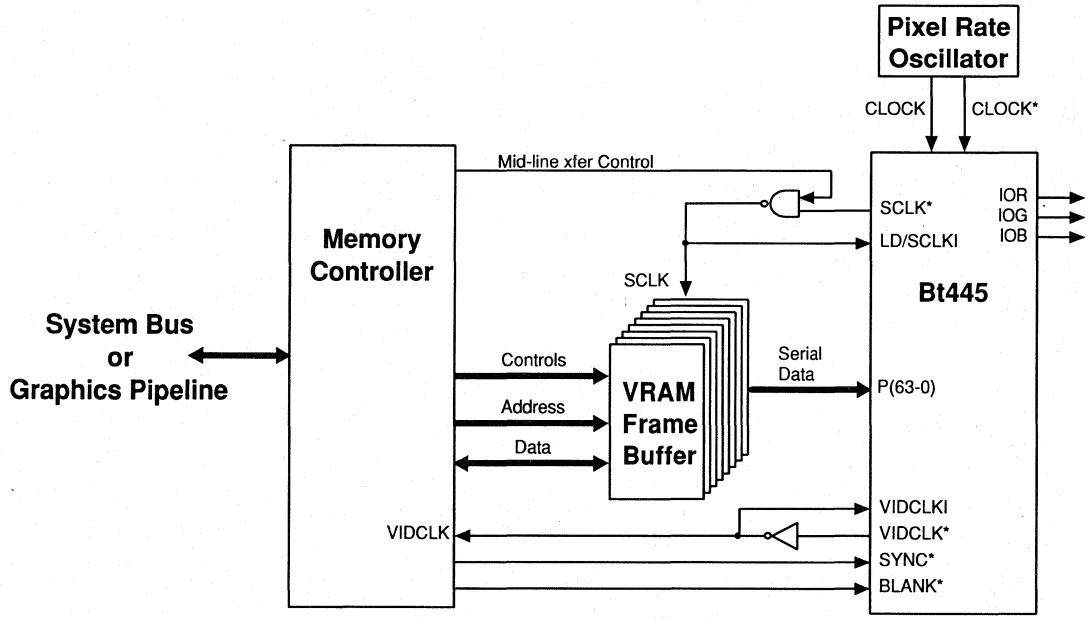

Figure 17. Frame Buffer Interface with Externally Generated Pixel Clock and Bt445-Generated SCLK.

Applications Information *(continued)*

The Bt445-Generated VRAM Shift Clock and PLL-Generated Pixel Clock

This configuration is very similiar to the previous one without the PLL generated pixel clock. Here, a relatively low frequency crystal is connected to the OSC, OSC* inputs, instead of using an ECL oscillator operated on a pseudo-ECL supply (i.e., +5 and GND) connected to the CLOCK and CLOCK* inputs of the Bt445.

In this configuration, the maximum pixel rate is limited by the PLL maximum operational frequency of 135 MHz. See Figure 18.

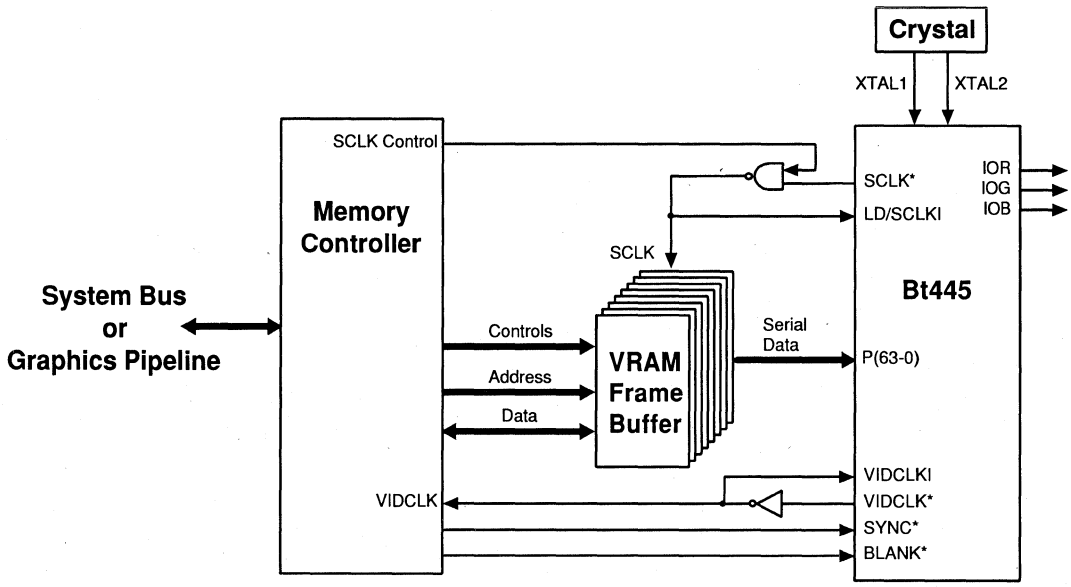

Figure 18. Frame Buffer Interface for Bt445-Generated VRAM Serial Clock and Pixel Clock.

Applications Information *(continued)*

Digital Output Port

Figure 19 shows a simplified typical connection between the Bt445, a CRT display, and a typical VGA resolution TFT flat-panel display. The VSYNC* and HSYNC* inputs to the Bt445 are not internally used; they are only synchronized with the pixel data and presented on the PVSYNC* and PHSYNC* outputs, respectively. This allows for variations between CRT and flat-panel SYNC signal timings and durations. However, the horizontal line rates and pixel rates must be identical if both displays are to be driven simultaneously.

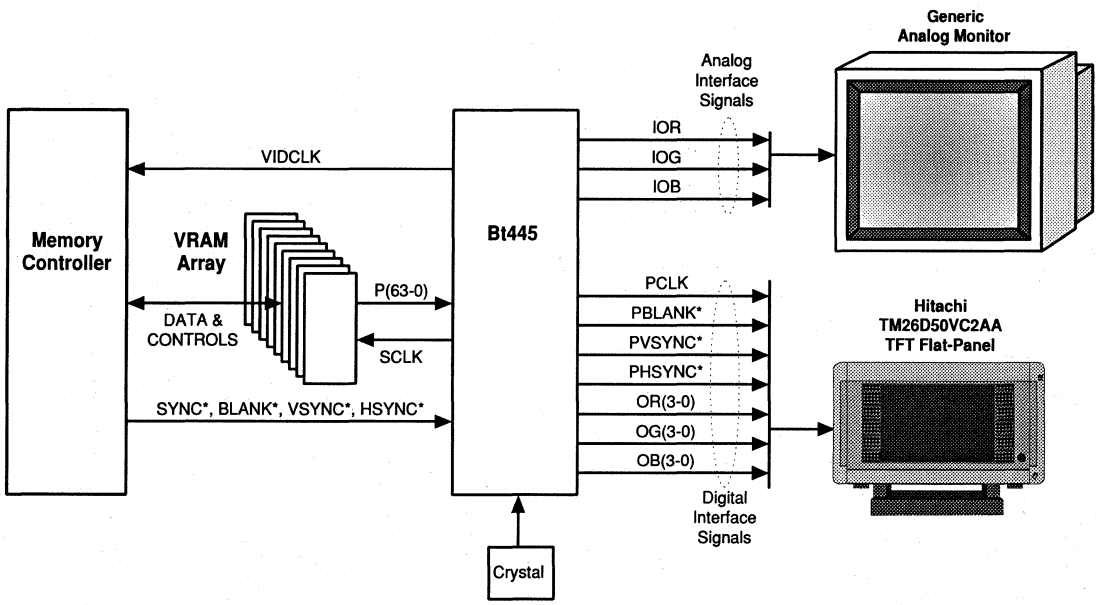

Figure 19. Typical Connection Diagram for Digital Output Port to 640 x 480 TFT Flat-Panel Display.

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Applications Information *(continued)*

Interfacing to High-Resolution Flat-Panel Displays

Preliminary information suggests that high-resolution flat-panel displays will achieve the required pixel rates without using excessive clock speeds if more than 1 pixel per clock cycle is provided, in the same fashion that high-resolution Brooktree RAMDACs accept pixels at the input pixel port. The Bt445's digital output port may operate up to 55 MHz, providing the bandwidth required, for example, for a 1024 x 768 active matrix panel. However, to provide 2 pixels at half the clock rate, some intervening logic may be used. Refer to Figure 20.

For proper operation, the control signals PBLANK*, PVSYNC*, and PHSYNC* should only change on an even pixel. The sample logic shown resets the generated clock and pixel data on each edge of PBLANK*. Also note that the clock-to-Q delay on the flip-flop, which generates LD Clock to the panel, should be faster than the clock-to-Q delay of the pixel data registers.

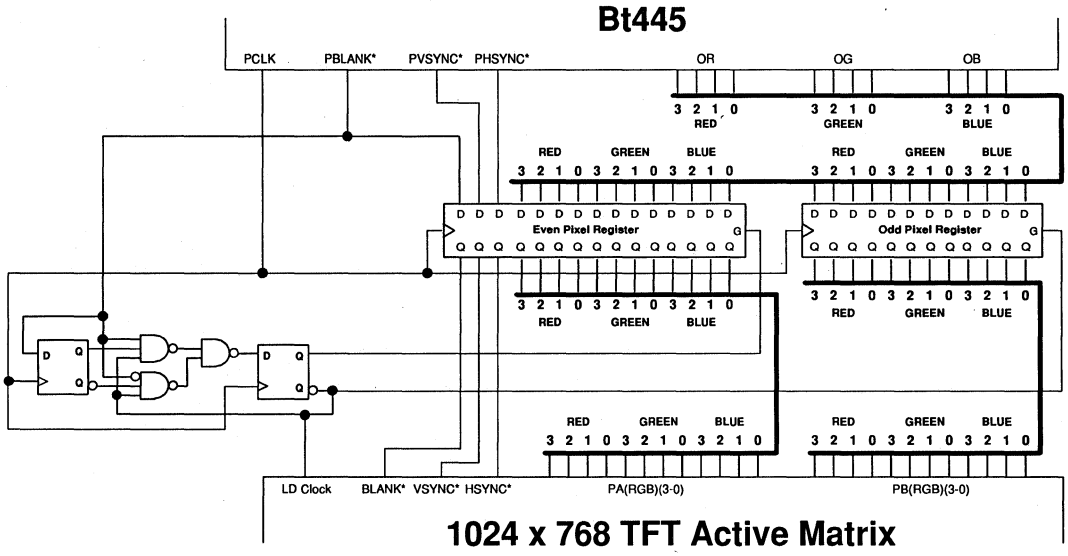

Figure 20. Interfacing the Bt445 with a 1024 x 768 TFT Active Matrix Flat Panel.

Applications Information *(continued)*

Digital Output Connection in 8-8-8 True-Color Mode

Figure 21 shows a simplified typical connection diagram using 8-8-8 true-color mode, to a Bt858 video encoder.

The registers are used to hold the data presented in the first half of the PCLK cycle; data presented during the second half of the PCLK cycle is held in the transparent latches, which are open during the clock high level. The configuration shown assumes that the external CRT timing generator provides the appropriate SYNC* and BLANK* signals at the input of the Bt445 for running the Bt858 in master mode 0. The PCLK may need to be re-driven and/or delayed to minimize PCLK loading and to meet hold time requirements of the Bt858.

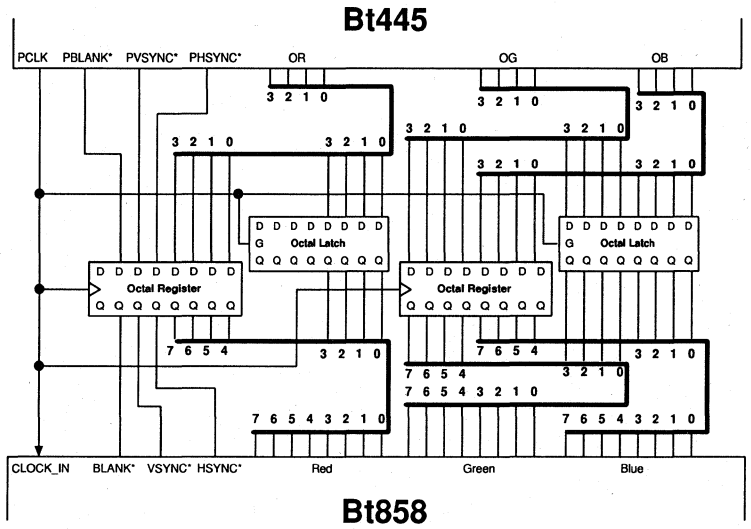

Figure 21. Interfacing the Bt445 to the Bt858.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω
Junction Temperature	Tjmax			+125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55			°C
Storage Temperature	TS	–65		+125	°C
Junction Temperature	TJ			+150	
Ceramic Package					°C
Plastic Package				+175	°C
				+150	
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL				°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS device on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*, VIDCLKI, and LD/SCLKI)					
Input High Voltage	VIH	2.0		VAA+0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Digital Inputs with Internal Pullups (Pixel Inputs and JTAG Pins)					
Input High Voltage	VIH	2.0		VAA+0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			60	µA
Input Low Current (Vin = 0.4 V)	IIL			–60	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Pixel Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA–1.0		VAA+0.5	V
Input Low Voltage	VKIL	GND–0.5		VAA-1.6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Clock Inputs (VIDCLKI, LD/SCLKI)					
Positive going threshold	VT+		1.7		V
Negative going threshold	VT–		0.9		V
Hysteresis	$(V_{T+}-V_{T-})$		0.8		V
Input High Current (Vin = 2.4 V)	Iih			1	µA
Input Low Current (Vin = 0.4 V)	Iil			–1	µA
Input Capacitance (f=1 MHz, Vin = 4.0 V)	Cin		4	10	pF
Digital Outputs (except D(7–0), PCLK, VIDCLK*, SCLK*)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			10	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			10	pF

See test conditions on the next page.

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DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs with Internal Pullups (except D(7–0), VIDCLK*, SCLK*)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			60	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			10	pF
Digital Outputs (VIDCLK*, SCLK*)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			10	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			20	pF
Digital Outputs (PCLK)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			60	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			20	pF
Digital Outputs (D(7–0))					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
Three-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC- to-DAC Matching			2	5	%
Output Compliance	VOC	–1.0		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % VAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

AC Characteristics

Input Clock

		150 MHz Devices			135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			150			135			110	MHz
Clock Cycle Time	12	6.7			7.4			9.09			ns
Clock Pulse Width High	13	2.7			3			4			ns
Clock Pulse Width Low	14	2.7			3			4			ns

MPU Port

		150 MHz Devices			135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
R/W, C0, C1 Setup	1	0			0			0			ns
R/W, C0, C1 Hold	2	15			15			15			ns
CE* Low Time	3	50			50			50			ns
CE* High Time	4	25			25			25			ns
CE* ↓ to Data Driven	5	7			7			7			ns
CE* ↓ to Data Valid	6			75			75			75	ns
CE* ↑ to Data Three-Stated	7			15			15			15	ns
Write Data Setup Time	8 (Note 1)	35			35			35			ns
Write Data Hold Time	9	3			3			3			ns

Note 1: The parameter shown guarantees write data capture. To prevent unnecessary pixel disturbances when writing control registers, the write data should be valid throughout the CE* active duration.

Input Pixel

		150 MHz Devices			135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
LD/SCLKI	LDmax			75			75			75	MHz
Pixel and Control Setup	10	3			3			3			ns
Pixel and Control Hold	11	2			2			2			ns

AC Characteristics *(continued)*

VIDCLKI

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
VIDCLKI Cycle Time	15	13.3			13.3			13.3			ns
VIDCLKI Pulse Width High	16	5.32			5.32			5.32			ns
VIDCLKI Pulse Width Low	17	5.32			5.32			5.32			ns
BLANK*, HSYNC*/SYNC*, VSYNC* Setup											
BLANK*, HSYNC*/SYNC*, VSYNC* Hold											

Analog Output

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog Output Delay	18		TBD			TBD			20		ns
Analog Output Rise/Fall	19		2			2			2		ns
Analog Output Settling (Note 1)	20			8			8			8	ns
TTL Output Skew	21			TBD			TBD			TBD	ns
Clock/Data Feedthrough (Note 2)			35			35			35		pV–sec
Glitch Impulse (Note 3)			50			50			50		pV–sec
Analog Output Skew (Note 4)			0	2		0	2		0	2	ns
Pipeline Delay		TBD		TBD	TBD		TBD	6		10	Clocks
VAA Supply Current (Note 5)	IAA			TBD			TBD			TBD	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10 percent and 90 percent points. ECL input values are VAA – 0.8 to VAA – 1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20 percent and 80 percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 40 pF. See timing notes in Figures 22–26. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Note 1: Output settling time measured from 50 percent point of full-scale transition to output settling within ±1 LSB.

Note 2: Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74 HC logic. Settling time does not include clock and data feedthrough.

Note 3: Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

Note 4: Output delay time measured from 50 percent point of the rising clock edge to 50 percent point of full-scale transition.

Note 5: At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20°C. IAA (max) at VAA = 5.25 V, TA = 0°C.

AC Characteristics *(continued)*

System Clock Generation AC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
VAA valid to VIDCLK stable				tbd	ns
VAA valid to CPUCLK stable				tbd	ns
VAA valid to MCLK stable				tbd	ns
RESET* active pulse width	33	tbd			ns
S0, S1 to RESET* setup time	34			tbd	ns
S0, S1 to RESET* hold time	35			tbd	ns
CE* rise to new VIDCLK rate	36	tbd		tbd	ns
CE* rise to new CPUCLK rate	37	tbd		tbd	ns
S0, S1 to new CPUCLK rate	38			tbd	ns
RESET* to new CPUCLK rate	39			tbd	ns
CPUCLK	Fmax			50	MHz
MCLK20	Fmax			20	MHz
MCLK25	Fmax			25	MHz
CPUCLK, MCLK20, MCLK25 rise/fall time				5	ns
CPUCLK, MCLK20, MCLK25 duty cycle		40	50	60	%
CPUCLK, MCLK20, MCLK25 Jitter				tbd	

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PLL Clock Generation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Crystal/Oscillator Frequency		6	20	25	MHz
PLL Clock Generator Multiplicand	M	25		63	
PLL Clock Generator Divisor	N	4		15	
PLL M/N Ratio		tbd		tbd	
PLL M/N Generated Pixel Clock Rate		65		135	MHz
PLL M/N Generated Pixel Clock Accuracy		tbd		tbd	%
PLL M/N Generated Pixel Clock Jitter				tbd	

Above parameters apply to predivided (i.e., before applying 1/L) pixel clock generation.

AC Characteristics *(continued)*

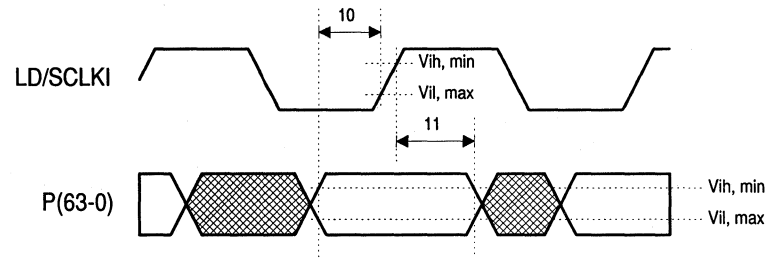


Figure 22. Input Pixel Timing.

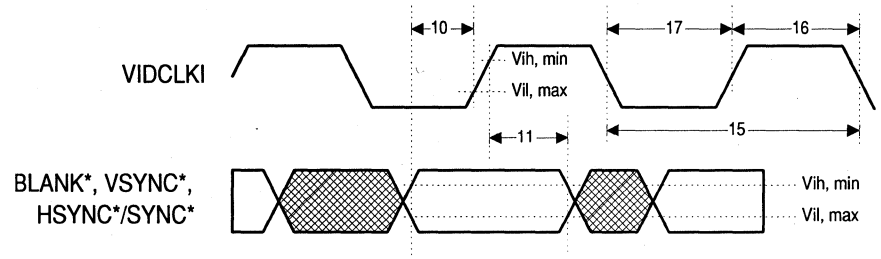


Figure 23. Input Control Timing.

AC Characteristics *(continued)*

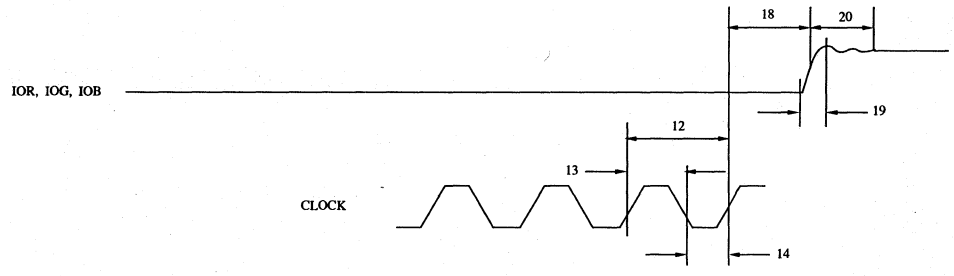


Figure 24. Video Output Timing.

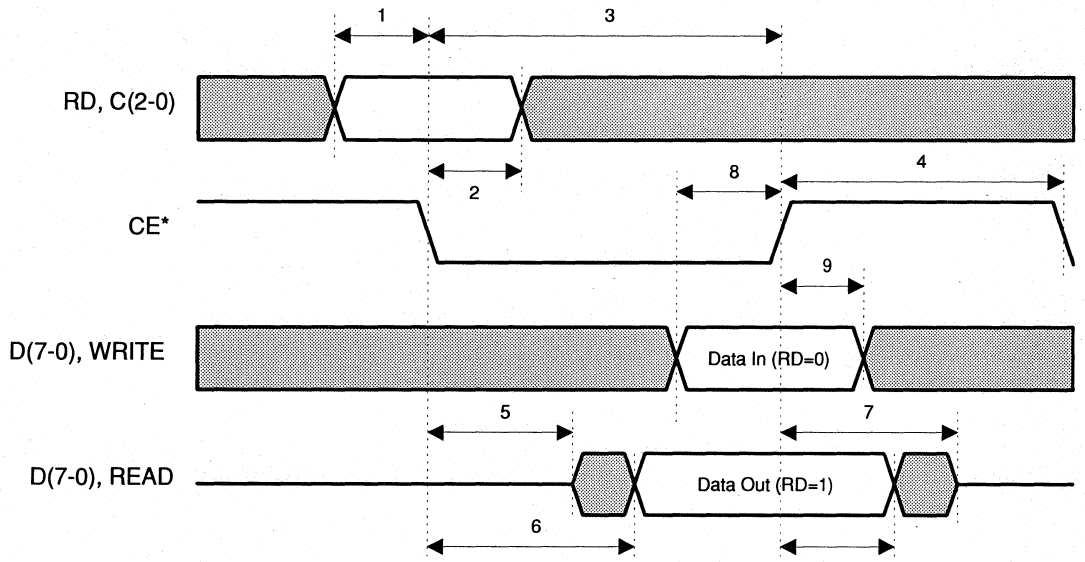


Figure 25. MPU Read/Write Timing.

AC Characteristics *(continued)*

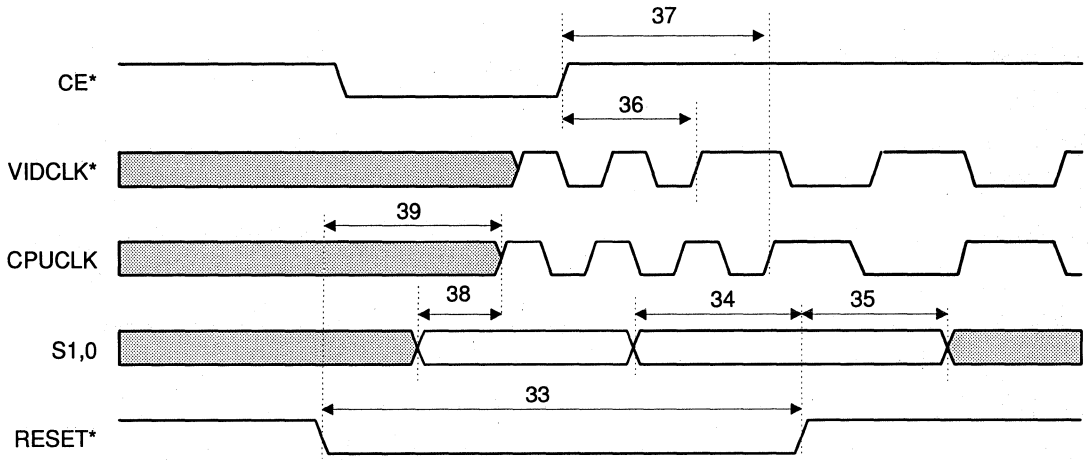


Figure 26. Reset, CPU Clock, and VIDCLK* Output Timing.

AC Characteristics *(continued)*

Digital Pixel Output Port AC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
PCLK Cycle Time (Note 1) 4-4-4 Mode 8-8-8 Mode	40	 18.2 36.4			ns
PCLK Edge to Data, Control Delay	41			15	ns
PCLK Edge to Data, Control Hold	42	10			ns
PCLK Pulse High Duty Cycle	43	40		60	%
PCLK VIDCLK*, SCLK* rise/fall time			3		ns
PSYNC*, PBLANK*, PVSYNC*, PHSYNC* rise/fall time			7		ns
O(R,G,B)(3–0) cycle time		36.4			ns
O(R,G,B)(3–0) rise/fall time			5		ns

Note 1: The cycle time parameters apply only when the PCLK output is enabled. See Figure 27.

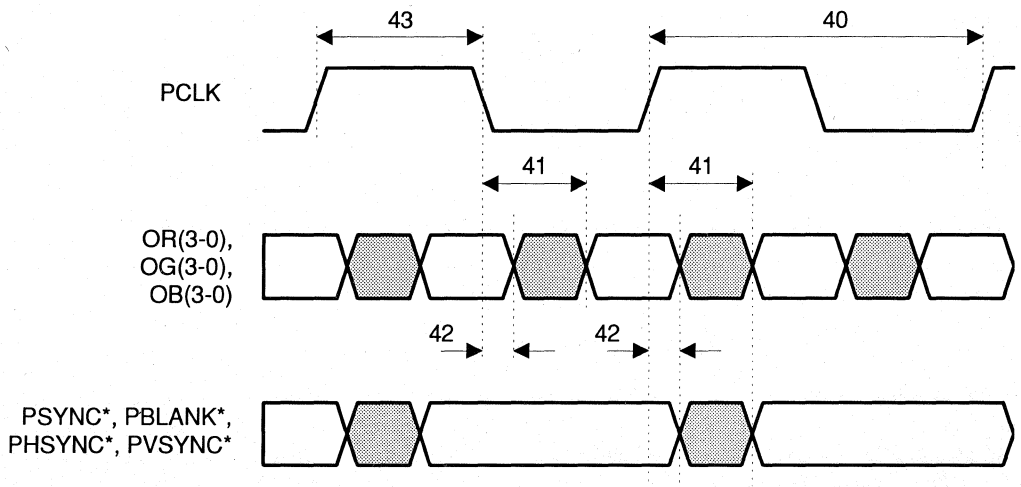


Figure 27. Pixel Output Port Timings.

Ordering Information

Model Number	Speed (MHz)	Package	Ambient Temperature Range
Bt445KPF150	150	160-pin Plastic Quad Flatpack	0° to +70° C
Bt445KPF135	135	160-pin Plastic Quad Flatpack	0° to +70° C
Bt445KPF110	110	160-pin Plastic Quad Flatpack	0° to +70° C

Bt451
Bt457
Bt458

125 MHz/135 MHz/ 165 MHz Monolithic CMOS 256 Color Palette RAMDAC™

Distinguishing Features

- 165, 135, 125, 110, 80 MHz Operation
- 4:1 or 5:1 Input MUX
- 256-Word Dual-Port Color Palette
- 4 Dual-Port Overlay Registers
- RS-343A-Compatible Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- 84-pin PLCC or PGA Package
- +5 V CMOS Monolithic Construction

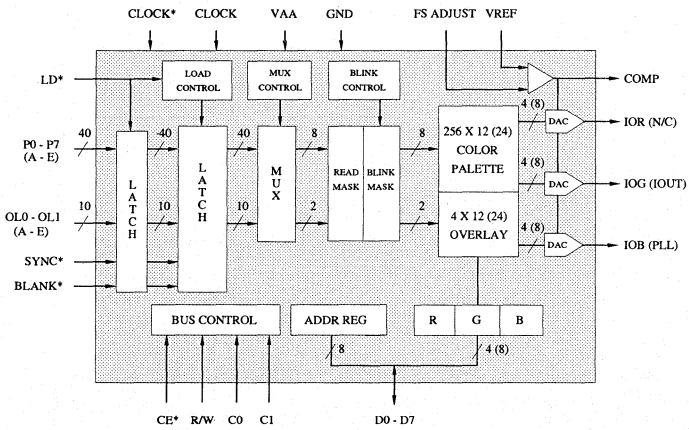
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt462, Bt468

Functional Block Diagram



Product Description

The Bt451, Bt457, and Bt458 are pin-compatible and software-compatible RAMDACs designed specifically for high-performance, high-resolu- tion color graphics. The architecture enables the display of 1280 x 1024 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enable TTL-compatible interface (up to 32 MHz) to the frame buffer, while maintaining the 165 MHz video data rates required for sophisticated color graphics.

The Bt451 has a 256 x 12 color lookup table with triple 4-bit video D/A converters.

The Bt458 contains a 256 x 24 color lookup table with triple 8-bit video D/A converters.

The Bt457 is a single-channel version of the Bt458 and has a 256 x 8 color lookup table with a single 8-bit video D/A converter. It includes a PLL output to enable subpixel synchronization of multiple Bt457s.

On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

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L458001 Rev. M

Brooktree®

MPU Interface

As illustrated in the functional block diagram, the Bt451/457/458 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

As presented in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Bt451/458 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (12-bit word for the Bt451) and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. The Bt451 uses only the 4 most significant bits of color data (D4–D7) and ignores D0–D3.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by reading another sequence of red, green, and blue data. The Bt451 outputs only 4 bits of color data onto D4–D7 and forces D0–D3 to logical zeros.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

ADDR0–7	C1	C0	Addressed by MPU
$xx	0	0	address register
$00–,$FF	0	1	color palette RAM
$00	1	1	overlay color 0
$01	1	1	overlay color 1
$02	1	1	overlay color 2
$03	1	1	overlay color 3
$04	1	0	read mask register
$05	1	0	blink mask register
$06	1	0	command register
$07	1	0	control/test register

Table 1. Address Register (ADDR) Operation.

Bt457 Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette RAM or the overlay registers. The address register then increments to the next location, which the MPU may modify by writing another color.

Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (8 bits each of red, green, and blue) may be read or written to three Bt457s in a single MPU cycle. In this application, the CE* inputs of all three Bt457s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, and green CE* during green write cycle).

When accessing the color palette RAM, the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a read or write cycle to overlay register 3.

Bt457 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt457 is programmed to be a red, green, or blue RAMDAC and will respond only to the assigned color read or write cycle. In this application, the Bt457s share a common 8-bit data bus. The CE* inputs of all three Bt457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

Additional Information

Although the color palette RAM and overlay registers are dual ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU during the write cycle, 1 or more of the pixels on the display screen can be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers are also accessed through the address register in conjunction with the C0 and C1 inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Circuit Description *(continued)*

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt451/457/458 incorporates internal latches and multiplexers. As illustrated in Figure 1, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either 4 or 5 consecutive pixels, are latched into the device. With this configuration, the sync and blank timing will be recognized only with 4- or 5-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

Each clock cycle, the Bt451/457/458 outputs color information based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis. Or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 4 or 5 independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than four, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

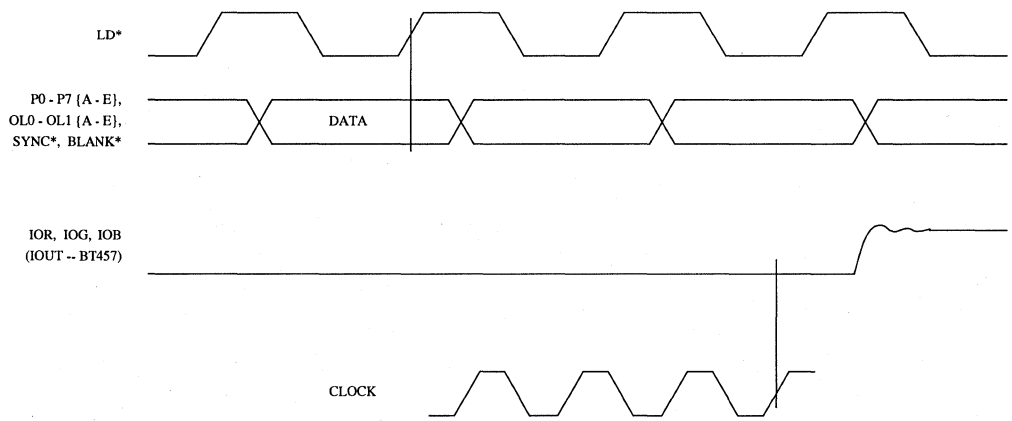


Figure 1. Video Input/Output Timing.

Circuit Description *(continued)*

Color Selection

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure blinking does not cause a color change to occur during the active display time (i.e., in the middle of the screen), the Bt451/457/458 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAM. Table 2 is the truth table used for color selection.

Video Generation

Every clock cycle, the selected color information from the color palette RAMs or overlay registers is presented to the D/A converters.

The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Only the green output (IOG) on the Bt451 and Bt458 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt451, Bt457, and Bt458 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

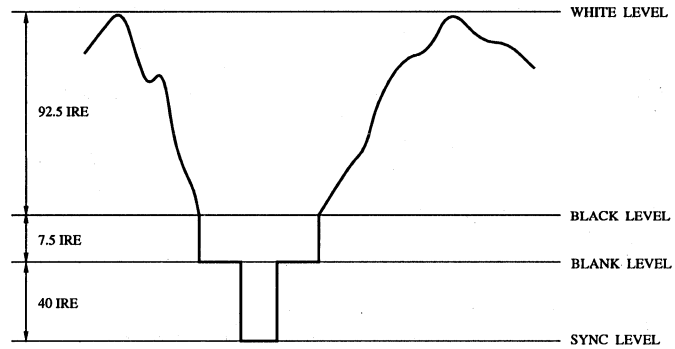
5

CR6	OL1	OL0	P0–P7	Addressed by Frame
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description *(continued)*

IOR, IOB		IOG (IOUT)	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. RS-343A levels and tolerances are assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (IOUT) (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω and VREF = 1.235 V. The Bt451 uses only the upper 4 DAC input data bits.

Table 3. Video Output Truth Table.

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR0 corresponds to data bus bit D0.

CR7	Multiplex select (0) 4:1 multiplexing (1) 5:1 multiplexing	This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth the CLOCK rate. The pipeline delay of the Bt457/458 can be reset to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt457/458 must again be reset to a fixed pipeline delay.
CR6	RAM enable (0) use overlay color 0 (1) use color palette RAM	When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
CR5, CR4	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).
CR3	OL1 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL1 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to pallett selection. A value of logical zero does not affect the value of the OL1 {A–E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.
CR2	OL0 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL0 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to pallett selection. A value of logical zero does not affect the value of the OL0 {A–E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Internal Registers *(continued)*

Command Register (continued)

CR1	OL1 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL1 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A–E} inputs.
CR0	OL0 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL0 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A–E} inputs.

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–E}), and D7 corresponds to bit plane 7 (P7 {A–E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A–E}), and D7 corresponds to bit plane 7 (P7 {A–E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Internal Registers *(continued)*

Bt451/458 Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting only one of the (red, green, or blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the (red, green, blue, and low or high nibble) enable information previously written. Either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then reads the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits and D0–D3 containing (red, green, blue, and low or high nibble) enable information, as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Since the Bt451 has 4-bit D/A converters, bit D3 of the test register will always be a logical zero.

Bt457 Control/Test Register

The control/test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converter. It may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information
D3	low (logical one) or high (logical zero) nibble
D2	blue channel enable
D1	green channel enable
D0	red channel enable

To use the control/test register, the MPU writes to it, specifying the low or high nibble of color information. When the MPU reads the register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain whatever was previously written to the register. Either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green, and blue enable bits are used to specify the mode in which color data is written to and read from, the Bt457. If all three enable bits are logical zeros, each write cycle to the color palette RAM or overlay registers loads 8 bits of color data. During each read cycle of the color palette RAM or overlay registers, 8 bits of color data are output onto the data bus. If a 24-bit data bus is available, three Bt457s can be accessed simultaneously.

If any of the red, green, or blue enable bits is a logical one, the Bt457 assumes the MPU is reading and writing color information using red-green-blue cycles, such as are used on the Bt451 and Bt458. Setting the appropriate enable bit configures the Bt457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logical one, and a red-green-blue write cycle occurred, the Bt457 would input data only during the green write cycle. If a red-green-blue read cycle occurred, the Bt457 would output data only during the green read cycle. CE* must be a logical zero during each of the red-green-blue cycles. Only 1 of the enable bits must be a logical one. This mode of operation is useful when only an 8-bit data bus is available and the software drivers are written for RGB operation.

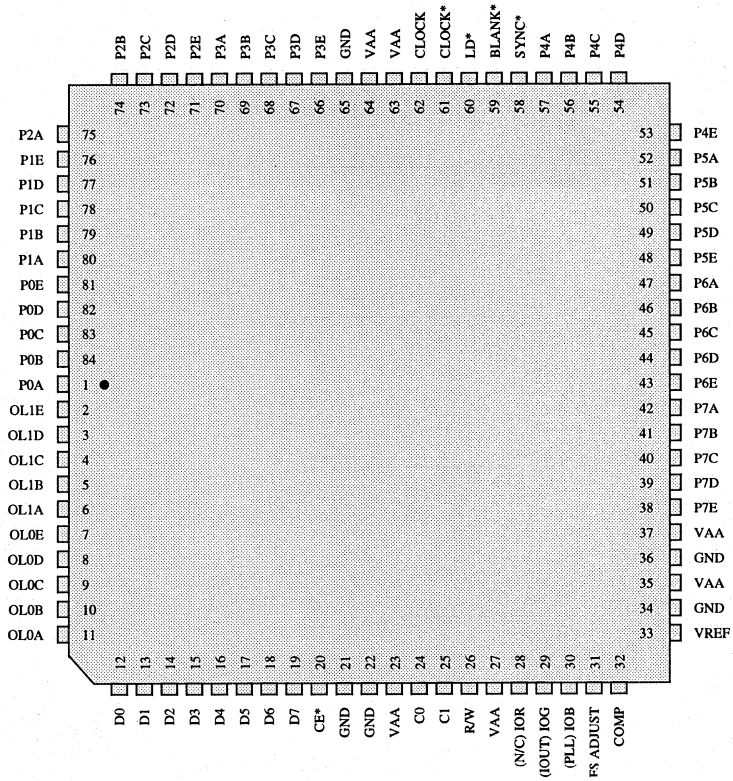
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Table 3. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL1 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is either one fourth or one fifth the CLOCK rate, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which 1 of the 256 entries in the color palette RAM is to be used to provide color information. Either 4 or 5 consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. The {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats.
OL0–OL1 {A–E}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD*. In conjunction with bit 6 of the command register, they specify which palette is to be used for color information, as follows: **OL1 / OL0 / CR6 = 1 / CR6 = 0** 0 / 0 / color palette RAM / overlay color 0 0 / 1 / overlay color 1 / overlay color 1 1 / 0 / overlay color 2 / overlay color 2 1 / 1 / overlay color 3 / overlay color 3 When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for either 4 or 5 consecutive pixels are input through this port. Unused inputs should be connected to GND.
IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figure 4 in the PC Board Layout Considerations section). The Bt457 outputs IOUT rather than IOR, IOG, and IOB.
PLL	Phase lock loop current output—Bt457 only. This high-impedance current source is used to enable multiple Bt457s to be synchronized with subpixel resolution when used with an external PLL. A logical one on the BLANK* input results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and to maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *The PC Board Layout Considerations section contains critical layout criteria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 3). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG (or IOUT for the Bt457) is: RSET (Ω) = 11,294 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB (for the Bt451 and Bt458) for a given RSET is: IOR, IOB (mA) = 8,067 * VREF (V) / RSET (Ω)
VREF	Voltage reference input. An external voltage reference circuit, such as that shown in Figure 4, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 4. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as presented in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Pin Descriptions *(continued)*—84-Pin J-Lead Package



Note: Bt457 pin names are in parentheses.

Pin Descriptions *(continued)*—84-pin PGA Package

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L9	P5A	K11	VAA	C12
SYNC*	M10	P5B	L12	VAA	C11
LD*	M9	P5C	K12	VAA	A9
CLOCK*	L8	P5D	J11	VAA	L7
CLOCK	M8	P5E	J12	VAA	M7
				VAA	A7
P0A	G1	P6A	H11		
P0B	G2	P6B	H12	GND	B12
P0C	H1	P6C	G12	GND	B11
P0D	H2	P6D	G11	GND	M6
P0E	J1	P6E	F12	GND	B6
				GND	A6
P1A	J2	P7A	F11		
P1B	K1	P7B	E12	COMP	A12
P1C	L1	P7C	E11	FS ADJUST	B10
P1D	K2	P7D	D12	VREF	C10
P1E	L2	P7E	D11		
				CE*	A5
P2A	K3	OL0A	A1	R/W	B8
P2B	M1	OL0B	C2	C1	A8
P2C	L3	OL0C	B1	C0	B7
P2D	M2	OL0D	C1		
P2E	M3	OL0E	D2	D0	C3
				D1	B2
P3A	L4	OL1A	D1	D2	B3
P3B	M4	OL1B	E2	D3	A2
P3C	L5	OL1C	E1	D4	A3
P3D	M5	OL1D	F1	D5	B4
P3E	L6	OL1E	F2	D6	A4
				D7	B5
P4A	M11	IOG (IOUT)	A10		
P4B	L10	IOB (PLL)	A11		
P4C	L11	IOR (N/C)	B9		
P4D	K10				
P4E	M12				

Note: Bt457 pin names are in parentheses.

Pin Descriptions *(continued)*—84-pin PGA Package

	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	GND	VAA	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	VAA	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	VREF							P4D	P4B	SYNC*
9	VAA	IOR									BLK*	LD*
8	C1	R/W									CLK*	CLK
7	VAA	C0									VAA	VAA
6	GND	GND									P3E	GND
5	CE*	D7									P3C	P3D
4	D6	D5									P3A	P3B
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B

Bt451/457/458

(TOP VIEW)

alignment marker (on top)

	M	L	K	J	H	G	F	E	D	C	B	A
12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	VAA	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	VAA	GND	IOB
10	SYNC*	P4B	P4D							VREF	FS ADJ	IOG
9	LD*	BLK*									IOR	VAA
8	CLK	CLK*									R/W	C1
7	VAA	VAA									C0	VAA
6	GND	P3E									GND	GND
5	P3D	P3C									D7	CE*
4	P3B	P3A									D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A

(BOTTOM VIEW)

Pin	Bt451/458	Bt457
A10	IOG	IOUT
A11	IOB	PLL
B9	IOR	N/C

PC Board Layout Considerations

PC Board Considerations

The Bt451, Bt457, and Bt458 layouts should be optimized for lowest noise on their power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt451, Bt457, and Bt458 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 3.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 10 µF capacitor shown in Figure 4 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt451, Bt457, and Bt458 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For

PC Board Layout Considerations *(continued)*

example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt451, Bt457, and Bt458 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt451, Bt457, and Bt458 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

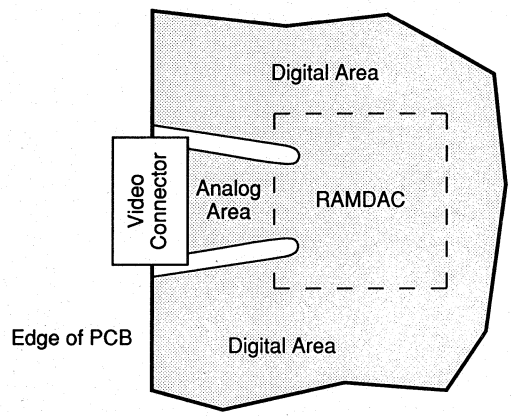
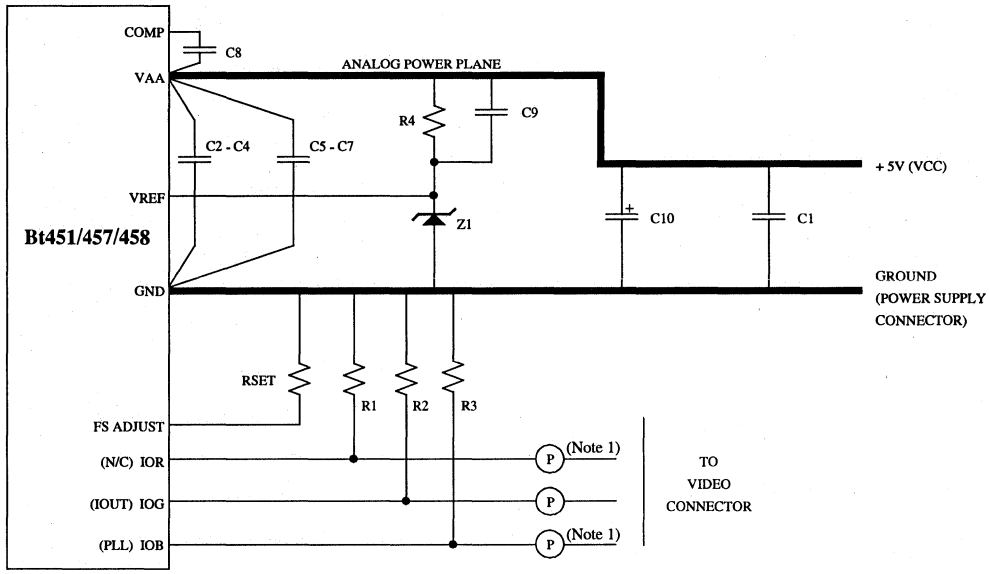


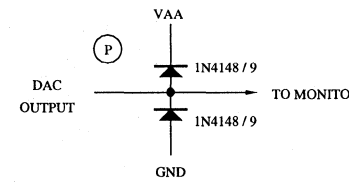
Figure 3. Sample Layout Showing Power and Ground Plane Isolation Gaps.

PC Board Layout Considerations *(continued)*



Note: Bt457 pin names are in parenthesis. Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Note 1: Not used with Bt457.



Location	Description	Vendor Part Number
C1–C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt451/457/458. R3 is not used with Bt457 (see the Application Information section).

Figure 4. Typical Connection Diagram and Parts List.

Clock Interfacing

Because of the high clock rates at which the Bt451, Bt457, and Bt458 may operate, they are designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 5.)

Applications of 165 MHz require robust ECL clock signals with strong pulldown (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt451/457/458 will not function if it uses a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by 4 or 5 (depending on whether 4:1 or 5:1 multiplexing was specified) and translating the result to TTL levels. As LD* may be phase shifted relative to CLOCK, propagation delays need not be considered when the LD* signal is derived. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC* and BLANK*).

It is recommended that the Bt438 or Bt439 Clock Generator Chips be used to generate the clock and load signals. Both support the 4:1 and 5:1 input multiplexing of the Bt451/457/458, and set the pipeline delay of the Bt457 and Bt458 to eight clock cycles. Figures 5 and 6 illustrate use of the Bt438 with the Bt451/457/458.

When a single Bt457 is used, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

5

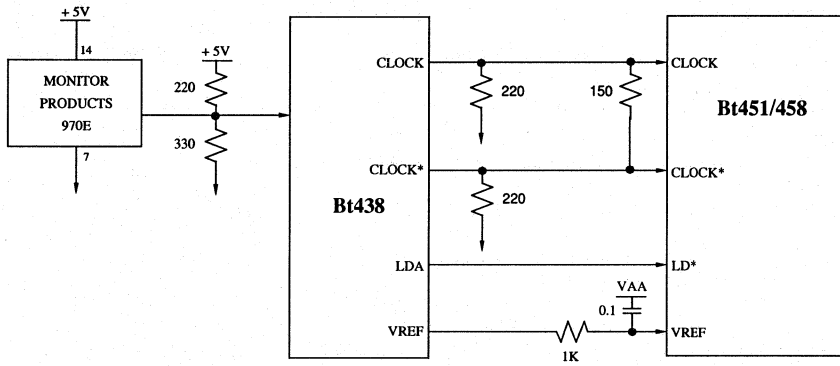


Figure 5. Generating the Bt451/458 Clock Signals.

Application Information *(continued)*

Setting the Pipeline Delay (Bt457 and Bt458)

The pipeline delay of the Bt457/458, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt457/458 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when they are used with the Bt457/458.

To reset the Bt457/458, it should be powered up with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for at least three rising edges of LD*. The device can be held with CLOCK and CLOCK* stopped for an unlimited time.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When the clocks are restarted, the minimum clock pulse width must not be violated.

When the Bt457/458 is reset to an eight-clock-cycle pipeline delay, the blink counter circuitry is not reset. Therefore, if the multiple Bt457/458s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00, and the overlay blink enable bits should be logical zeros. Software may control blinking through the read mask register and overlay display enable bits.

In standard operation, the Bt457/458 must be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

Bt457 Color Display Applications

For color display applications in which up to four Bt457s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt457, synchronizes the clock and load signals to subpixel resolution, and sets the pipeline delay of the Bt457 to eight clock cycles. The Bt439 may also be used to interface the Bt457 to a TTL clock. Figure 7 illustrates use of the Bt439 with the Bt457.

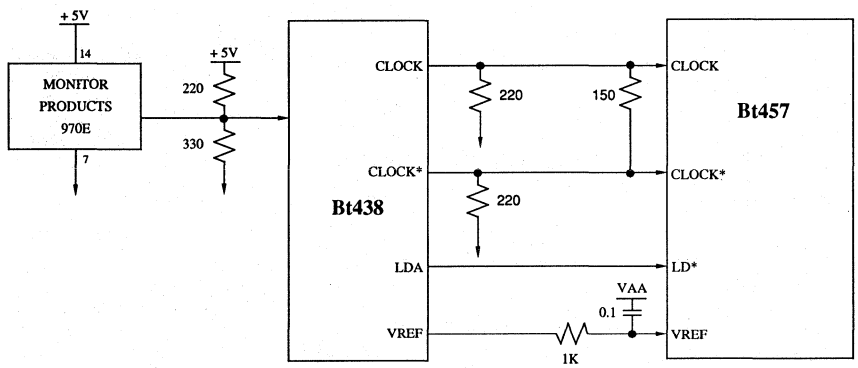


Figure 6. Generating the Bt457 Clock Signals (Monochrome Application).

Application Information *(continued)*

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt457 relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt457s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt457s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

If subpixel synchronization of multiple Bt457s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt457s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt457s must still have a 0.1 µF bypass capacitor to VAA. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

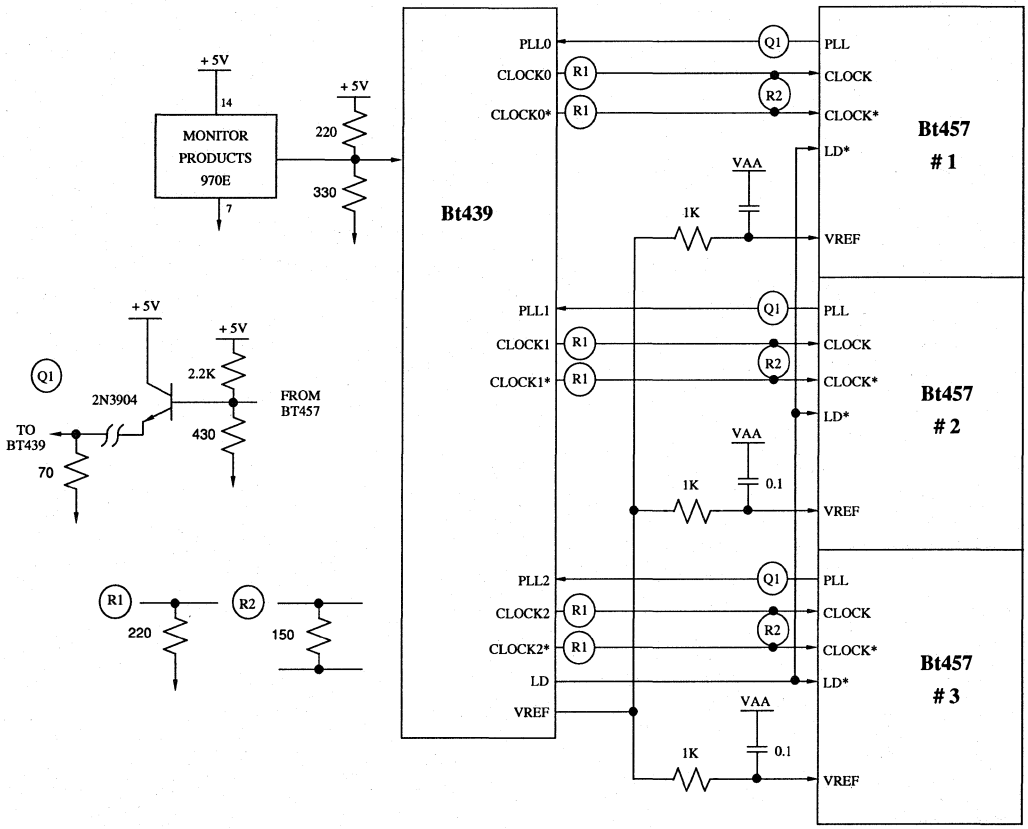


Figure 7. Generating the Bt457 Clock Signals (Color Application).

Application Information *(continued)*

Using Multiple Devices

When multiple RAMDACs are used, each RAMDAC should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each RAMDAC has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Bt457 Nonvideo Applications

The Bt457 may be used in nonvideo applications by disabling the video-specific control signals. SYNC* should be a logical zero, and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}457 * VREF\ (V) / Iout\ (mA)$$

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 610 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

Initializing the Bt451/458

Following a power-on sequence, the Bt451/458 must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt458 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be reinitialized when the multiplex selection is changed (e.g., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt451/458 as follows:

4:1 multiplexed operation
no overlays
no blinking

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

Application Information *(continued)*

Initializing the Bt457 (Monochrome)

Following a power-on sequence, the Bt457 must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt457 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be reinitialized when the multiplex selection is changed (e.g., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457 as follows:

4:1 multiplexed operation
no overlays
no blinking
color data written/read every cycle

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write data to RAM (location $00)	01
Write data to RAM (location $01)	01
:	:
Write data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write data to overlay (location $00)	11
Write data to overlay (location $01)	11
:	:
Write data to overlay (location $03)	11

Initializing the Bt457 (Color) 24-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. A 24-bit MPU data bus is available to access all three Bt457s in parallel.

The operation and initialization are the same as the monochrome application of the Bt457.

Initializing the Bt457 (Color) 8-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. An 8-bit MPU data bus is available to access the Bt457s.

While accessing the command, read mask, blink mask, and control/test and address registers, each Bt457 must be accessed individually. While accessing the color palette RAM or overlay registers, all three Bt457s are accessed simultaneously.

Following a power-on sequence, the Bt457s must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt457s to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be reinitialized when the multiplex selection is changed (e.g., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457s as follows:

4:1 multiplexed operation
no overlays
no blinking
each Bt457 initialized as a red, green, or blue device

Control Register Initialization	C1, C0
Red Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $01 to test register	10
Green Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $02 to test register	10

Application Information *(continued)*

Blue Bt457

Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $04 to test register	10

Color Palette RAM Initialization

Write $00 to all three address registers	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization

Write $00 to all three address registers	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short-Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA				
Storage Temperature	TS	–55		+125	°C
Junction Temperature	TJ	–65		+150	°C
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8 (4)	8 (4)	8 (4)	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1 (1/8)	LSB
Differential Linearity Error	DL			±1 (1/16)	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size					
Bt451			1.175		mA
Bt457, Bt458			69.1		µA
DA0-to-DAC Matching (Note 1)			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Does not apply to the Bt457.

AC Characteristics

		165 MHz Devices			135 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			165			135	MHz
LD* Rate	LDmax			41.25			33.75	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	6.06			7.4			ns
Clock Pulse Width High Time	13	2.6			3			ns
Clock Pulse Width Low Time	14	2.6			3			ns
LD* Cycle Time	15	24.24			29.63			ns
LD* Pulse Width High Time	16	10			12			ns
LD* Pulse Width Low Time	17	10			12			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough (Note 1)			35			35		pV–sec
Glitch Impulse (Note 1)			50			50		pV–sec
Analog Output Skew (Note 2)			0	2		0	2	ns
Pipeline Delay		6		10				Clocks
VAA Supply Current (Note 3)	IAA							
Bt451			n/a	n/a		320	410	mA
Bt458			310	370		235	340	mA
Bt457			n/a	n/a		207	257	mA

See test conditions and notes at the end of this section.

AC Characteristics *(continued)*

		125 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			125			110	MHz
LD* Rate	LDmax			31.25			27.5	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	8			9.09			ns
Clock Pulse Width High Time	13	3.2			4			ns
Clock Pulse Width Low Time	14	3.2			4			ns
LD* Cycle Time	15	32			36.36			ns
LD* Pulse Width High Time	16	13			15			ns
LD* Pulse Width Low Time	17	13			15			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough (Note 1)			35			35		pV–sec
Glitch Impulse (Note 1)			50			50		pV–sec
Analog Output Skew (Note 2)			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current (Note 3)	IAA							
Bt451			310	400		295	385	mA
Bt458			225	330		210	315	mA
Bt457			200	250		190	240	mA

See test conditions and notes at the end of this section.

5

AC Characteristics *(continued)*

Parameter	Symbol	80 MHz Devices			Units
		Min	Typ	Max	
Clock Rate	Fmax			80	MHz
LD* Rate	LDmax			20	MHz
R/W, C0, C1 Setup Time	1	0			ns
R/W, C0, C1 Hold Time	2	15			ns
CE* Low Time	3	50			ns
CE* High Time	4	25			ns
CE* Asserted to Data Bus Driven	5	7			ns
CE* Asserted to Data Valid	6			75	ns
CE* Negated to Data Bus 3-Stated	7			15	ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	3			ns
Pixel and Control Setup Time	10	4			ns
Pixel and Control Hold Time	11	2			ns
Clock Cycle Time	12	12.5			ns
Clock Pulse Width High Time	13	5			ns
Clock Pulse Width Low Time	14	5			ns
LD* Cycle Time	15	50			ns
LD* Pulse Width High Time	16	20			ns
LD* Pulse Width Low Time	17	20			ns
Analog Output Delay	18		12		ns
Analog Output Rise/Fall Time	19		2		ns
Analog Output Settling Time	20			8	ns
Clock and Data Feedthrough (Note 1)			35		pV–sec
Glitch Impulse (Note 1)			50		pV–sec
Analog Output Skew (Note 2)			0	2	ns
Pipeline Delay		6		10	Clocks
VAA Supply Current (Note 3)	IAA				
Bt451			265	355	mA
Bt458			200	285	mA
Bt457			170	220	mA

See test conditions and notes on next page.

AC Characteristics *(continued)*

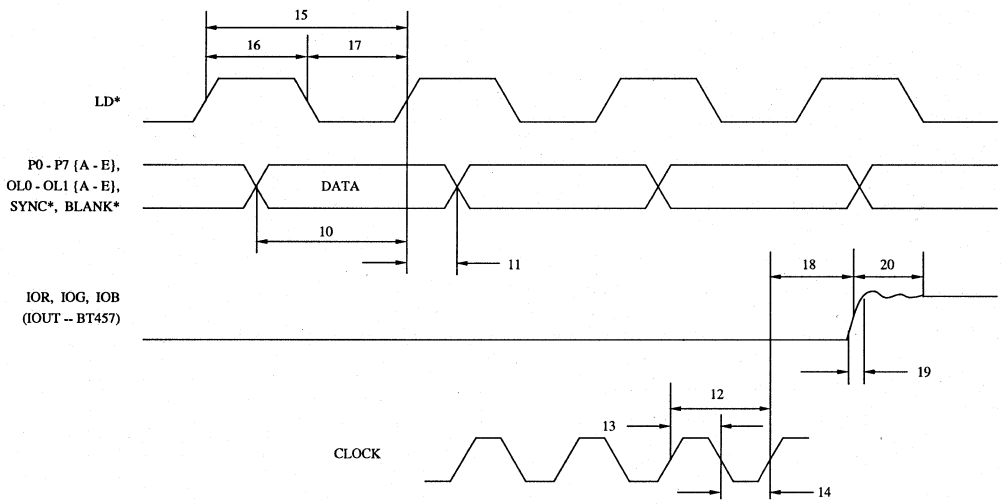
Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: Does not apply to the Bt457.

Note 3: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms



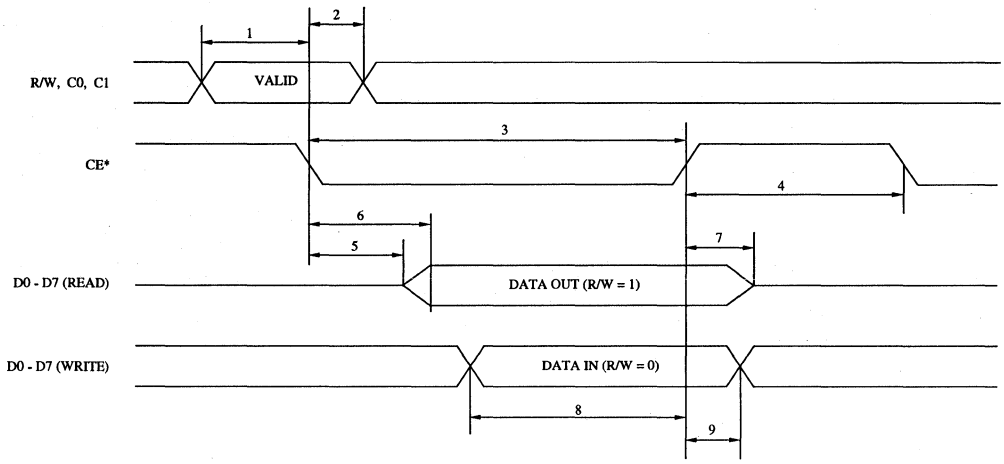
Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB for the Bt457/458 or ± 1/8LSB for the Bt451.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. Video Input/Output Timing.

Timing Waveforms *(continued)*



MPU Read/Write Timing.

Ordering Information

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LG165	256 x 24	triple 8-bit	165 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG135	256 x 24	triple 8-bit	135 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG125	256 x 24	triple 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG110	256 x 24	triple 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG80	256 x 24	triple 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458LPJ165	256 x 24	triple 8-bit	165 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ135	256 x 24	triple 8-bit	135 MHz	84-Pin Plastic J-Lead	0° to +70° C

Ordering Information *(continued)*

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LPJ125	256 x 24	triple 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ110	256 x 24	triple 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ80	256 x 24	triple 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KG135	256 x 12	triple 4-bit	135 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG125	256 x 12	triple 4-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG110	256 x 12	triple 4-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG80	256 x 12	triple 4-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KPJ135	256 x 12	triple 4-bit	135 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ125	256 x 12	triple 4-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ110	256 x 12	triple 4-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ80	256 x 12	triple 4-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KG135	256 x 8	single 8-bit	135 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG125	256 x 8	single 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG110	256 x 8	single 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG80	256 x 8	single 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KPJ135	256 x 8	single 8-bit	135 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ125	256 x 8	single 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ110	256 x 8	single 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ80	256 x 8	single 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C

Bt454

Bt455

170 MHz
Monolithic CMOS
16 Color Palette
RAMDAC™

Distinguishing Features

- 170, 135, 110 MHz Operation
- 4:1 Multiplexed TTL Pixel Ports
- Triple 4-bit D/A Converters
- 16-Word Dual-Port Color Palette
- 1 Dual-Port Overlay Palette
- RS-343A-Compatible Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 1 W

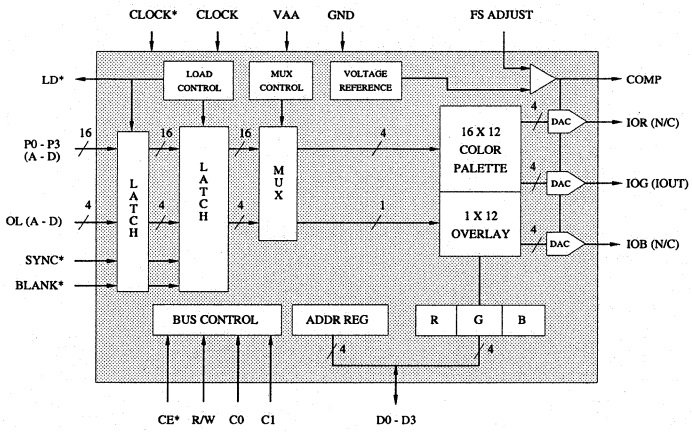
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Desktop Publishing

Related Products

- Bt451, Bt457, Bt458, Bt459 Bt460, Bt468

Functional Block Diagram



Product Description

The Bt454 and Bt455 are pin-compatible and software-compatible RAMDACs designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1600 x 1200 bit-mapped color graphics (up to 4 bits per pixel plus 1 bit of overlay information), minimizing the necessity of costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing (up to 42.5 MHz) to the frame buffer, while maintaining the 170 MHz video data rates required for sophisticated color graphics.

The Bt454 is a triple 4-bit video RAM-DAC that supports up to 17 simultaneous colors from a 4096 color palette. On-chip features include a temperature-compensated precision voltage reference, divide-by-4 of the clock for load generation, color overlay capability, and a dual-port color palette RAM.

The Bt455 is a single-channel version of the Bt454, well suited for high-performance monochrome or gray-scale applications.

The Bt454/455 generates RS-343A-compatible video signals and can drive doubly-terminated 75 Ω coax directly without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/4 LSB over the full temperature range.

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Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt454/455 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay register allow color updating without contention with the display refresh process.

As shown in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which color palette RAM entry or overlay register will be accessed by the MPU. The address register is used to address the internal RAM, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data to the color palette RAM, the MPU loads the address register with the desired RAM location to be modified. The MPU performs three successive write cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue write cycle, the address register increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read color data from the color palette RAM, the MPU loads the address register with the desired RAM location to be read. The MPU performs three successive read cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location, which the MPU may read by reading another sequence of red, green, and blue data.

When the MPU is accessing the color palette RAM, the address register resets to $0 following the blue read or write cycle to location $F.

To read from or write to the overlay register, the MPU uses C0 and C1 to select the overlay register and performs three successive read or write cycles (4 bits each of red, green, and blue). ADDR0–3 are not used.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as presented in Table 1. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 4 bits of the address register (ADDR0–3) are accessible to the MPU and are used to address the color palette RAM locations.

Although the Bt455 uses only the green channel, it must still go through the count-modulo-three write sequence. The values loaded into the red and blue color palette should be $0.

When the MPU is reading or writing the color values, the RAM or overlay register is accessed each time a 4-bit color value is read or written.

Although the color palette RAM and overlay register are dual ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU, one or more of the pixels on the display screen can be disturbed.

Figure 1 illustrates the MPU read/write timing when it is accessing the device.

Circuit Description (continued)

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0–3 (counts binary)	$x	0	0	address register
	$0–$F	0	1	color palette RAM
	$x	1	0	0 --> ADDRa, b (Note 1)
	$x	1	1	overlay register

Note 1: During writes D0–D3 are ignored, during reads 0 --> D0–D3.

Table 1. Address Register (ADDR) Operation.

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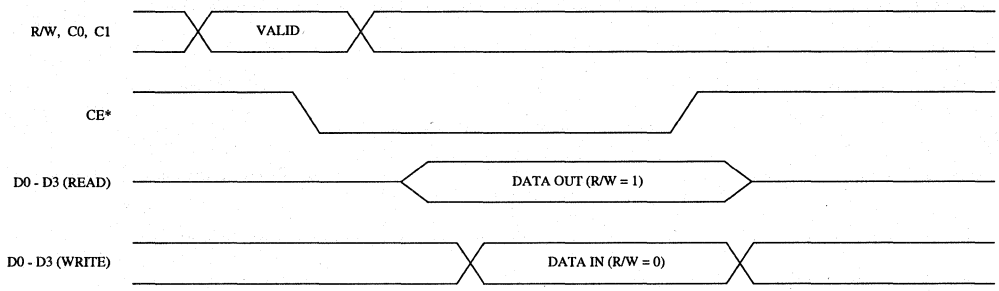

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at reasonable data rates (up to 42.5 MHz), the Bt454/455 incorporates internal latches and multiplexers. As illustrated in Figure 2, the SYNC*, BLANK*, P0–P3 {A–D}, and OL {A–D} inputs are latched on the rising edge of LDOUT. With this configuration, the sync and blank timing will be recognized only with 4-pixel resolution. Typically, the LDOUT signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs of the frame buffer.

The overlay inputs may have pixel timing, facilitating the use of an additional bit plane in the frame buffer to control overlay selection on a pixel basis. Or they may be controlled by external character or cursor generation logic.

The Bt454/455 generates the LDOUT signal internally by dividing the clock by 4. LDOUT is the setup-and-hold time reference for the pixel, overlay, sync, and blank inputs. It is recommended that LDOUT be buffered to clock the shift registers of the video DRAMs. To prevent LDOUT from inducing noise artifacts in the analog outputs, LDOUT must be series terminated to match the impedance of the LDOUT PCB trace. Resistance values of 33–68 Ω are recommended.

When the pixel and overlay data are latched by LDOUT, they are internally multiplexed at the pixel clock rate. On each clock cycle, the Bt454/455 outputs color information based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until all 4 pixels have been output, at which point the cycle repeats.

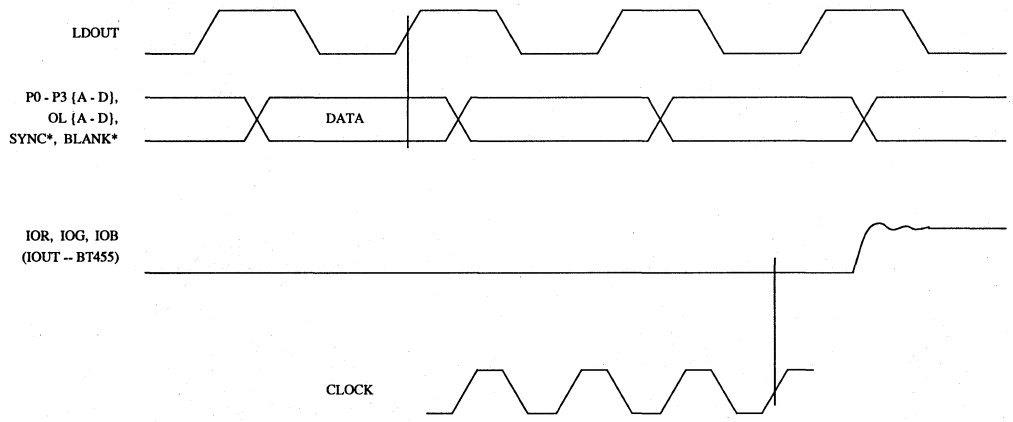

Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Video Generation

Each clock cycle, 4 bits of color information (P0–P3) and 1 bit of overlay information (OL) for each pixel are used to determine the sourch of color information—a color palette entry in the RAM or the overlay register. P0 is the LSB when addressing the color palette RAM. Table 2 is the truth table used for color selection.

Every clock cycle, the selected information is presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3.

The varying output current from each of the D/A converters produces a corresponding voltage level that is used to drive the color CRT monitor. Only the green output (IOG) on the Bt454 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt454/455 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

CRT Monitor Interface

The analog outputs can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable, when the outputs are soldered directly to a PC board. When the device is socketed, the device junction must not exceed a safe operating temperature.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

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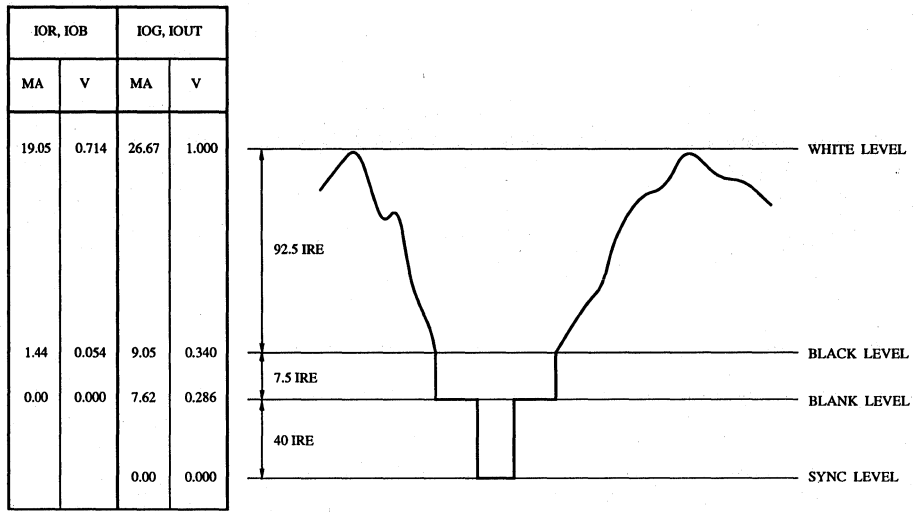
OL	P0–P3	Addressed by frame buffer
0	$0	color palette entry $0
0	$1	color palette entry $1
:	:	:
0	$F	color palette entry $F
1	$x	overlay color

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)



Note: 75 Ω doubly-terminated load and RSET = 523 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG, IOUT (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$F
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$0
BLACK - SYNC	1.44	1.44	0	1	$0
BLANK	7.62	0	1	0	$x
SYNC	0	0	0	0	$x

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω.

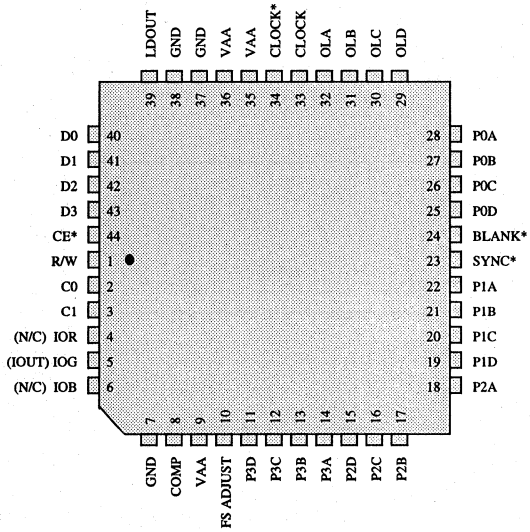
Table 3. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Table 3. It is latched on the rising edge of LDOUT. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, SYNC* should be asserted only during the blanking interval. It is latched on the rising edge of LDOUT. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LDOUT	Load control output (TTL compatible). The P0–P3 {A–D}, OL {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LDOUT. LDOUT is internally generated by dividing the clock by 4. LDOUT can drive only one TTL load. LDOUT must be series terminated with a 33–68 Ω resistor to match the impedance of the PCB trace. Incorrect impedance matching may cause display artifacts.
P0–P3 {A–D}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which 1 of the 16 entries in the color palette RAM is to be used to provide color information. Four consecutive pixels (up to 4 bits per pixel) are input through this port. They are latched on the rising edge of LDOUT. P0 is the LSB. Unused inputs should be connected to GND. The {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 4 pixels have been output, at which point the cycle repeats.
OL {A–D}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LDOUT. They specify which palette is to be used for color information. A logical zero indicates the color palette RAM is to provide color information, while a logical one indicates the overlay register is to provide color information. When the MPU is accessing the overlay palette, the P0–P3 {A–D} inputs are ignored. Unused inputs should be connected to GND.
IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 5 in the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load. The Bt455 outputs IOUT rather than IOR, IOG, and IOB.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). The IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = 13,948 / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = 9,963 / RSET (Ω)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin (Figure 5). Connecting the capacitor to VAA rather than to GND provides the highest possible low-frequency power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. (See Figure 1.)
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as presented in Table 1. They are latched on the falling edge of CE*.
D0 - D3	Data bus (TTL compatible). Data is transferred into and out of the device over this 4-bit bidirectional data bus. D0 is the least significant bit.



Note: Bt455 pin names are in parentheses.

PC Board Layout Considerations

PC Board Considerations

The Bt454 and Bt455 layouts should be optimized for lowest noise on the Bt454 and Bt455 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt454 and Bt455 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 4.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 5 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt454 and Bt455 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ring-

PC Board Layout Considerations (continued)

ing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt454 and Bt455 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt454 and Bt455 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 5 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

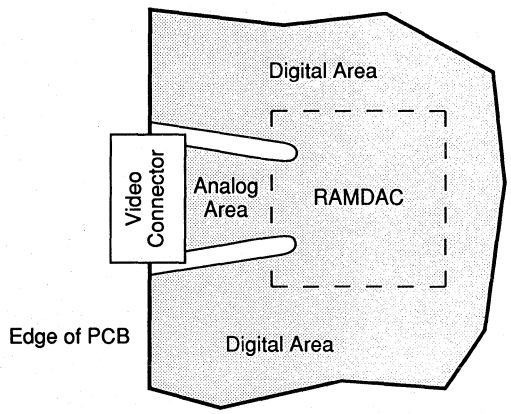
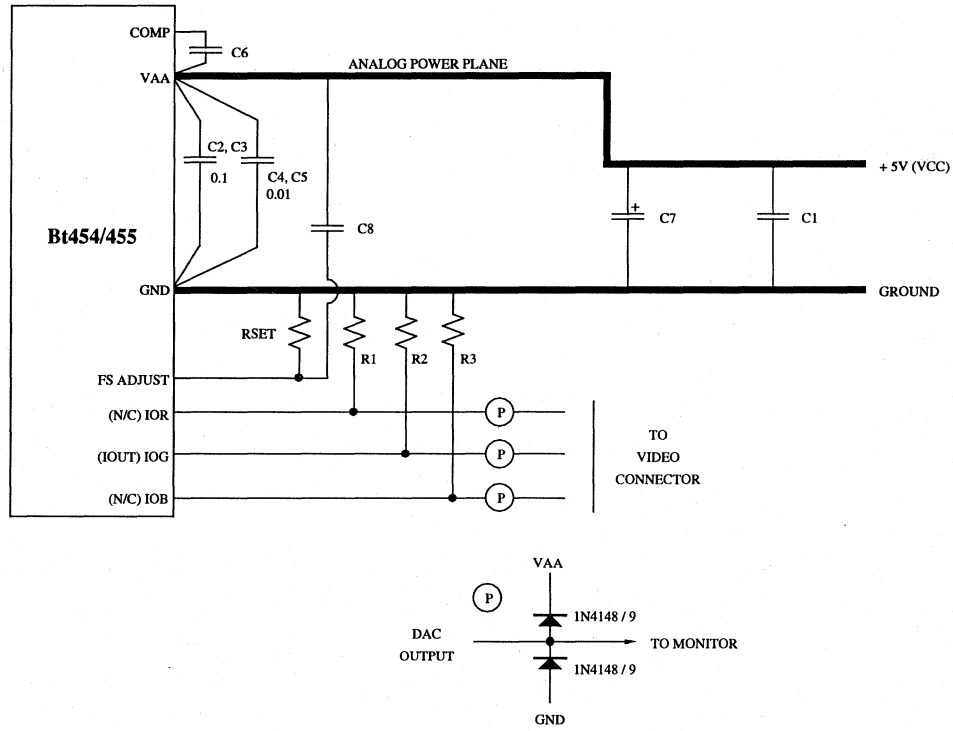


Figure 4. Sample Layout Showing Power and Ground Plane Isolation Gaps.

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C7	10 µF tantalum capacitor	Mallory CSR13G106KM
C1, C2, C3, C6, C8	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C4, C5	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R500S41W103KP
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt454/455.

Figure 5. Typical Connection Diagram and Parts List.

Application Information

LDOUT Termination

To reduce reflections on the LDOUT signal, it must be series-terminated to match the PCB trace impedance. Resistor values of 33–68 Ω are recommended. Impedance mismatch on the LDOUT signal may cause display artifacts.

LDOUT can drive only one TTL load.

Using Multiple Bt455s

When multiple Bt455s are used, each Bt455 should share a common power plane with one ferrite bead.

Each Bt455 must have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, and COMP capacitor.

TTL Clock Interfacing

Figure 6 illustrates the Bt454/455 interface to a TTL clock. The MC10H116 is operated from a single +5 V supply. The resistor network attenuates the TTL levels to MECL input levels. The CLOCK and CLOCK* inputs require 220 Ω pulldown termination resistors, which should be located as close to the driver as possible. A 150 Ω crossing resistor is also required, located as close to the RAMDAC as possible.

ECL Clock Generation

Because of the high clock rates at which the Bt454/455 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require 220 Ω pulldown termination resistors, which should be located as close to the driver as possible. A 150 Ω crossing resistor is also required, located as close to the RAMDAC as possible.

Applications of 170 MHz require robust ECL clock signals with strong pulldown (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals because of the CMOS process noise margins. The Bt454/455 will not function if it uses a single-ended CLOCK with CLOCK* connected to ground.

A 10K or 10KH ECL crystal oscillator that generates differential outputs, operating between +5 V and ground, may be interfaced directly to the B454/455, as shown in Figure 7. If the crystal oscillator generates only a single-ended output, an MC10H116 may be used to generate the differential clock signals, as illustrated in Figure 8. If the MC10H116 is not readily available, an MC10H101, MC10H105, or MC10H107 may be used.

Although ECL works well with a single +5 V supply, the TTL power supply lines must be isolated from the ECL power supply. Further information on ECL design may be obtained in the *MECL Device Data Catalog* and the *MECL System Design Handbook* by Motorola.

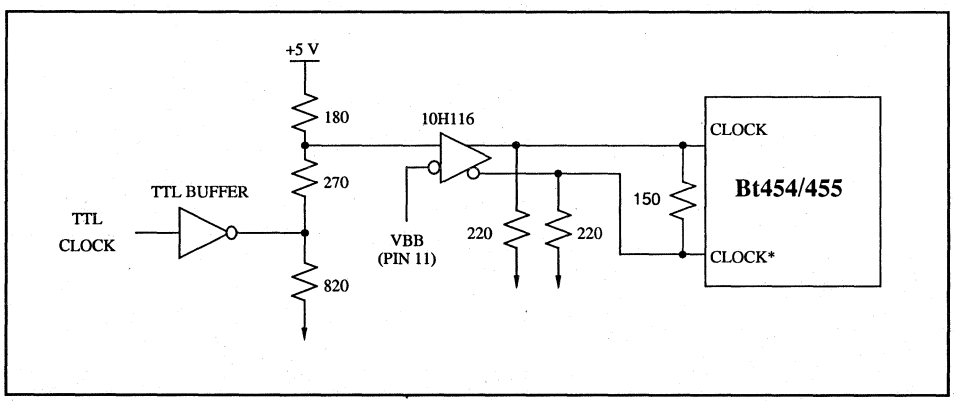


Figure 6. Interfacing the Bt454/455 to a TTL Clock.

Application Information (continued)

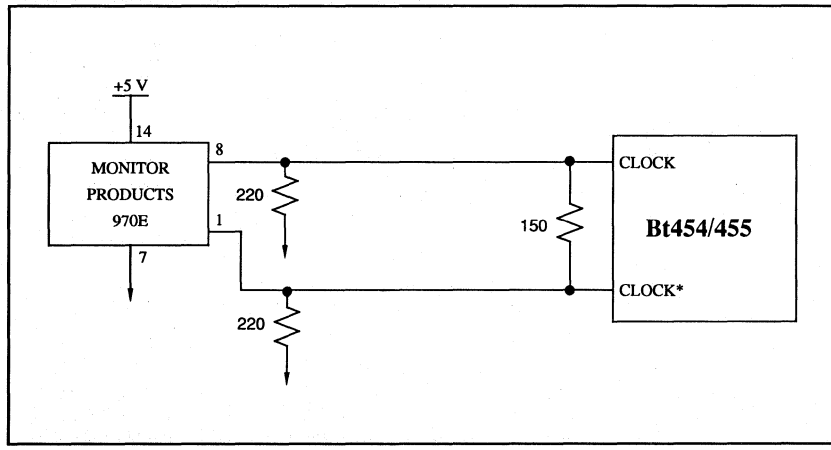


Figure 7. Interfacing to a Differential ECL Oscillator.

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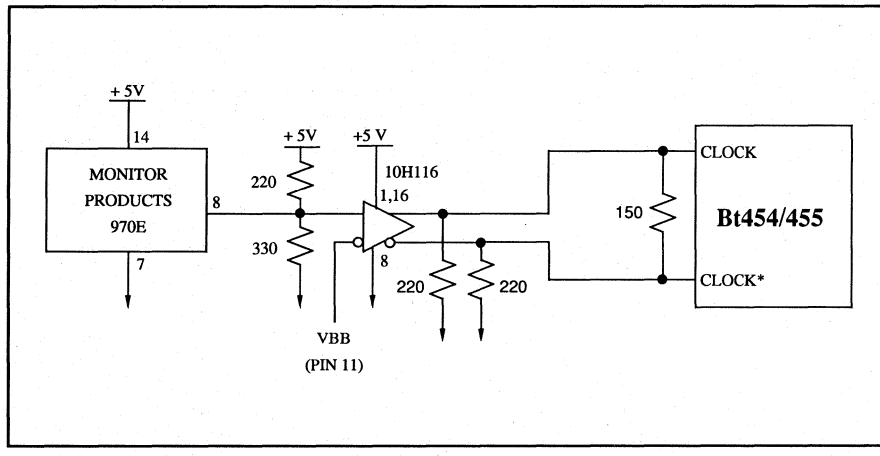

Figure 8. Interfacing to a Single-Ended ECL Oscillator.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/4	LSB
Differential Linearity Error	DL			±1/4	LSB
Gray-Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	0.6		6	V
Input High Current (Vin = 4.2 V)	IKIH			1	µA
Input Low Current (Vin = 3.2 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.2 V)	CKIN		10		pF
Digital Outputs					
Output High Voltage	VOH				
D0–D3 (IOH = –400 µA)		2.4			V
LDOUT (IOH = –12 mA)		2.4			V
Output Low Voltage	VOL				
D0–D3 (IOL = 3.2 mA)				0.4	V
LDOUT (IOL = 24 mA)				0.5	V
3-State Current (D0–D3)	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

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DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		16.81	19.05	21.30	mA
White Level Relative to Black		15.86	17.62	19.40	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size			1.175		mA
DAC-to-DAC Matching				5	%
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		20		pF
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	170 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			170			135			110	MHz
R/W, C0, C1 Setup Time	1	0			0			0			ns
R/W, C0, C1 Hold Time	2	15			15			15			ns
CE* Low Time	3	50			50			50			ns
CE* High Time	4	25			25			25			ns
CE* Asserted to Data Bus	5	10			10			10			ns
CE* Asserted to Data Valid	6			75			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15			15	ns
Write Data Setup Time	8	35			35			35			ns
Write Data Hold Time	9	10			10			10			ns
LDOUT Pulse Width High	10	9			11.5			13			ns
LDOUT Pulse Width Low	11	9			11.5			13			ns
Clock to LDOUT	12	4	7.5	14.3	4	7.5	14.3	4	7.5	14.3	ns
Pixel and Control Setup Time	13	0			0			0			ns
Pixel and Control Hold Time	14	3			5			5			ns
Clock Cycle Time	15	5.88			7.4			9			ns
Clock Pulse Width High	16	2			3			3.6			ns
Clock Pulse Width Low	17	2			3			3.6			ns
Analog Output Delay	18		20			20			20		ns
Analog Output Rise/Fall Time	19		2			2			2		ns
Analog Output Settling Time (Note 1)	20			6			9			9	ns
Clock and Data Feedthrough (Note 1)			70			70			70		pV - sec
Glitch Impulse (Note 1)			50			50			50		pV - sec
Analog Output Skew			0	2		0	2		0	2	ns
Pipeline Delay		6	6	6	6	6	6	6	6	6	Clocks
VAA Supply Current (Note 2)	IAA		200	tbd		150	tbd		120	200	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are 3.2–4.2 V with input rise/fall times ≤ 2 ns, measured between 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D3 output load ≤ 75 pF. See timing waveforms and notes in Figures 9 and 10. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

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Timing Waveforms

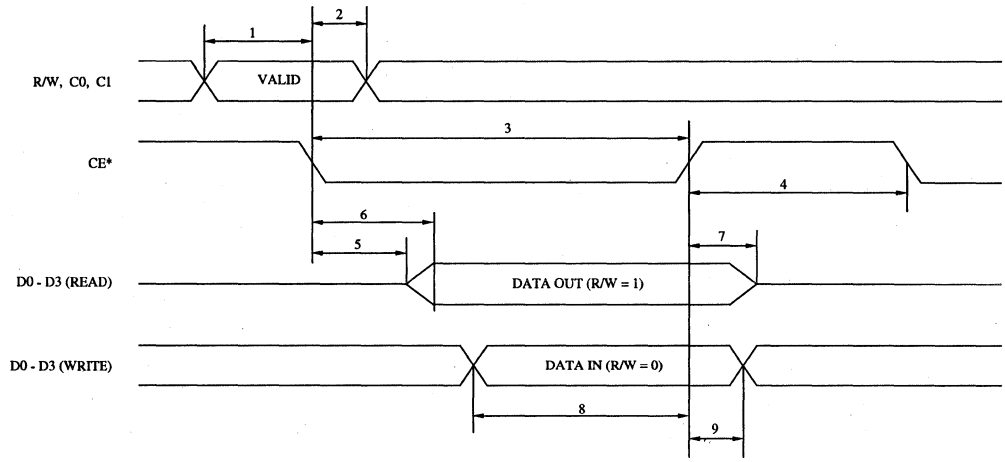
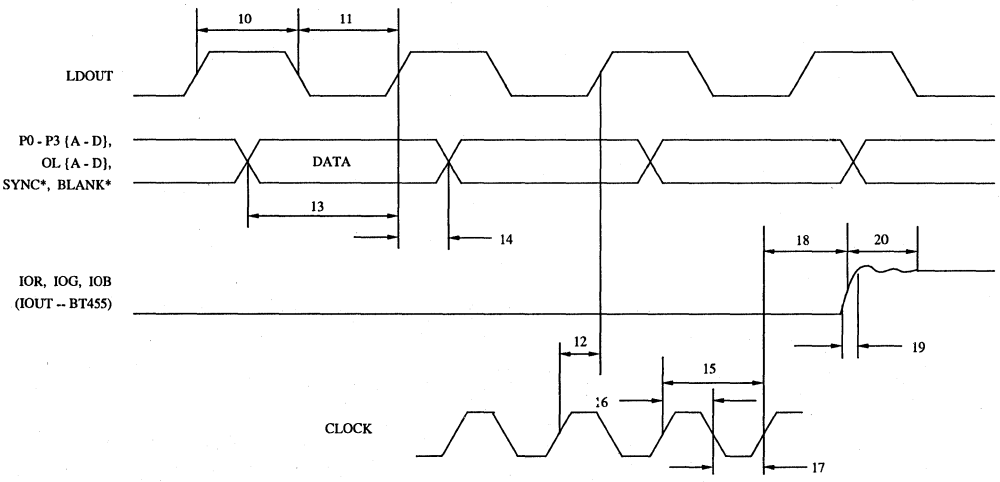


Figure 9. MPU Read/Write Timing Dimensions.

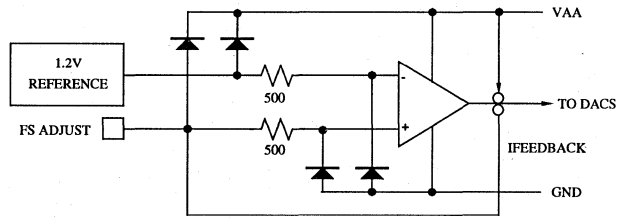


Note 1: Output delay time is measured from 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

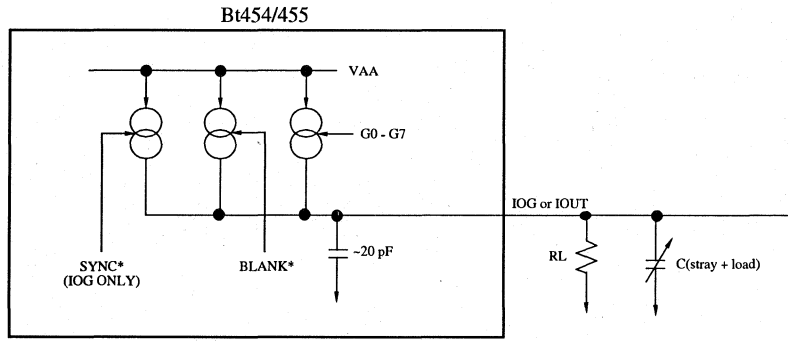
Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1/4 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 10. Video Input/Output Timing.



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output (IOG or IOUT).

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt454KPJ	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt454KPJ135	135 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt454KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ110	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ135	135 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C

Bt459

150 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

Distinguishing Features

- 150, 135, 110, 80 MHz Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- 1x to 16x Integer Zoom Support
- 1, 2, 4, or 8 Bits per Pixel
- Frame Buffer Interleave Support
- Pixel Panning Support
- On-Chip User-Definable 64 x 64 Cursor
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support for Overlays/ Cursor
- 132-pin PGA or PQFP Package

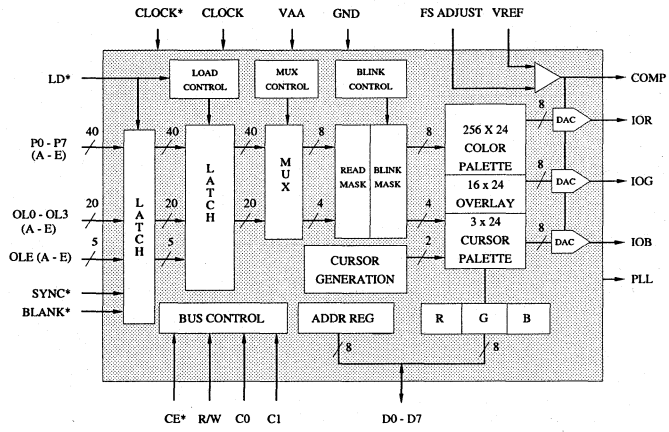
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt460, Bt462, Bt468

Functional Block Diagram



Product Description

The Bt459 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On-chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, 1x to 16x integer zoom support, and independent cursor generation.

Pixel data may be input as 1, 2, 4, or 8 bits per pixel. Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis for X Windows hardware support.

The Bt459 has an on-chip three-color 64 x 64 pixel cursor and a three-color full-screen (or full- window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with subpixel resolution.

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L459001 Rev. N

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MPU Interface

As illustrated in the functional block diagram, the Bt459 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As detailed in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles when it reads color data.

When the MPU is accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

The only time the address register resets to $0000 is after accessing location $0FFF (due to wraparound).

Although the color palette RAM, overlay RAM, and cursor color registers are dual ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0 (Note 1)
:	10	:
$010F	10	overlay color 15 (Note 1)
$0181	10	cursor color register 1 (Note 1)
:	:	cursor color register 2 (Note 1)
$0183	10	cursor color register 3 (Note 1)
$0200	10	ID register ($4A)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	interleave register
$020B	10	test register
$020C	10	red signature register
$020D	10	green signature register
$020E	10	blue signature register
$0220	10	revision register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$00FF	11	color palette RAM (Note 1)

Note 1: Indicates a requirement of three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers and cursor RAM are also accessed through the address register in conjunction with the C0 and C1 inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt459.

Bt459 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles when it reads color data.

This mode is useful if only an 8-bit data bus is available. Each Bt459 is programmed to be a red, green, or blue RAMDAC and will respond only to the assigned color read or write cycle. In this application, the Bt459s share a common 8-bit data bus. The CE* inputs of all three Bt459s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

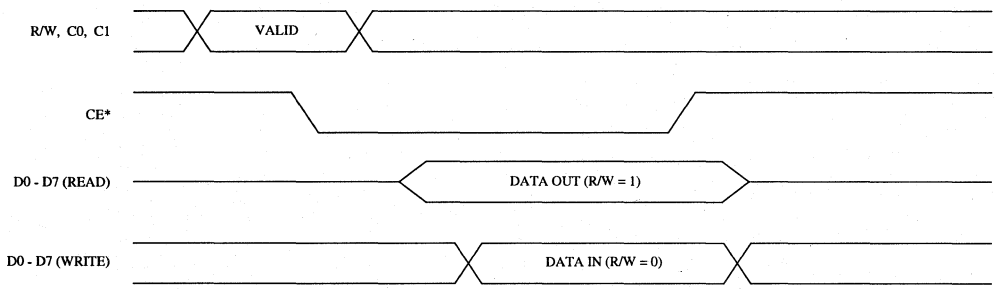


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt459 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either one, four, or five consecutive pixels, are latched into the device. With this configuration, the sync and blank timing will be recognized only with one, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 4:1 or 5:1 input multiplexing, the Bt459 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, followed by the {C} inputs, etc., until all four or five pixels have been output. At this point, the cycle repeats. In the 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 4 or 5, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one but not more than three clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

If 1:1 multiplexing is specified, LD* is also used to clock the Bt459 (at a maximum of 50 MHz). The rising edge of LD* still latches the P0–P7 {A}, OL0–OL3 {A}, OLE {A}, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. CLOCK must still run but is ignored.

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

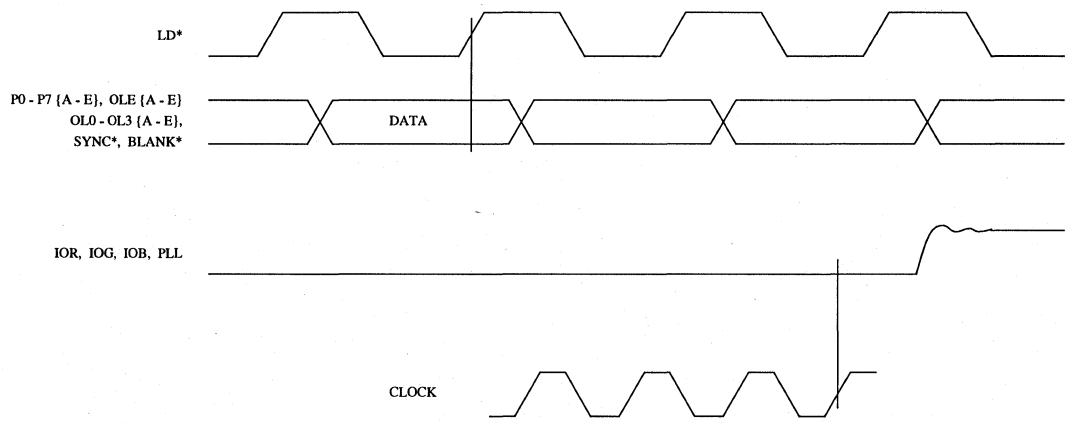


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

To ensure that a color change caused by blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt459 monitors the BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when the MPU is addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM.

The read and blink mask registers are not initialized. They must be initialized by the user after power-up for proper operation.

Pixel Panning

Panning is achieved through the delay of SYNC* and BLANK* by an additional one, two, three, or four clock cycles. To support pixel panning, command register_1 specifies the number of clock cycles to pan. Only the pixel inputs and underlays are panned—overlays and cursors are not.

If 0 pixel panning is specified, pixel {A} is output first, followed by pixel {B}, followed by pixel {C}, etc., until all 4 or 5 pixels have been output. At this point, the cycle repeats (assuming the interleave select is pixel {A}).

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, followed by pixel {D}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels. When a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt459 during the first LD* cycle that BLANK* is a logical zero.

In the 1:1 multiplex mode, 0-pixel panning should be specified.

The cursor position does not change relative to the edge of the display screen during panning.

Pixel Zoom

The Bt459 supports 1x to 16x integer zoom through pixel replication. Only the P0–P7 inputs are zoomed.

If 2x zooming is specified, the {A} pixel is output for two clock cycles, followed by the {B} pixel for two clock cycles, followed by the {C} pixel for two clock cycles, etc. The 3x zooming is similar, except each pixel is output for three clock cycles. For 1:1 multiplexing, only the {A} pixel is output.

LD* must be the pixel clock (1:1 multiplex mode), or one fourth or one fifth the CLOCK rate. Regardless of the zoom factor, P0–P7 data is latched every LD* cycle.

During 2x zoom, new P0–P7 data must be presented every two LD* cycles. During 3x zoom, new P0–P7 data must be presented every three LD* cycles. The pixel data must be held at the P0–P7 {A–E} inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

In the 1:1 multiplex mode, 1x zoom must be specified. Also, while in the block mode (1, 2, or 4 bits per pixel), 1x zoom must be specified. Figure 3 illustrates the zoom timing.

Block Mode Operation

The Bt459 supports loading of pixel data at 1, 2, 4, or 8 bits per pixel. Only the P0–P7 inputs are affected.

LD* must be the pixel clock (1:1 multiplex mode), or one fourth or one fifth the CLOCK rate. Regardless of the block mode, P0–P7 data is latched every LD* cycle.

For 8 bits per pixel, new P0–P7 information must be presented every LD* cycle. For 4 bits per pixel, new P0–P7 information must be presented every two LD* cycles. For 2 bits per pixel, new P0–P7 information must be presented every four LD* cycles. For 1 bit per pixel, new P0–P7 information must be presented every eight LD* cycles.

The pixel data must be held at the P0–P7 inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC* and BLANK* information are still latched every LD* cycle.

Figure 4 illustrates the block mode timing (4 bits per pixel).

Tables 2 and 3 detail the block mode operation and address of the color palette RAM.

In the 1:1 multiplex mode, 8 bits per pixel must be specified. Also, for block modes other than 8 bits per pixel, a 0-pixel interleave must be selected.

Circuit Description (continued)

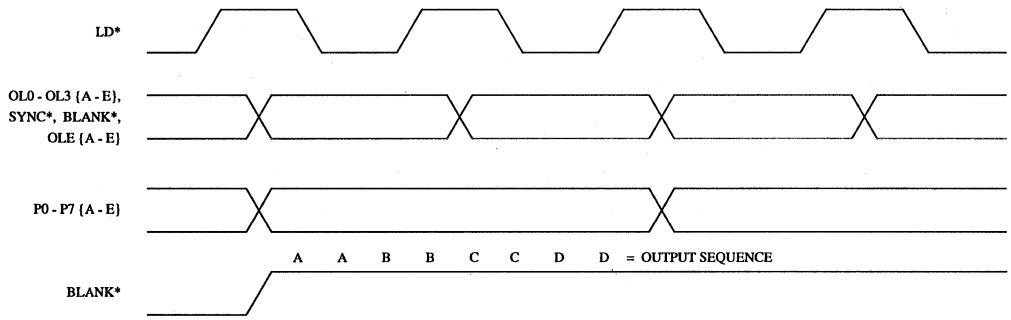


Figure 3. Zoom Input Timing (8 Bits per Pixel, 2x Zoom).

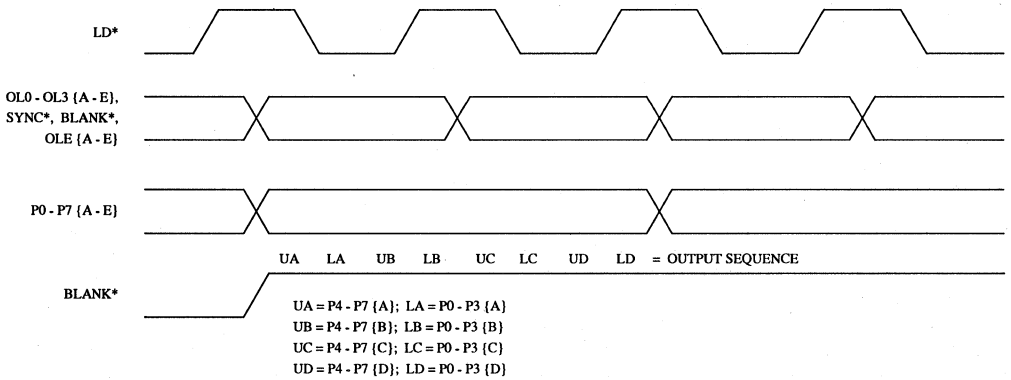


Figure 4. Block Mode Input Timing (4 Bits per Pixel, 1x Zoom, 4:1 Multiplexing).

Circuit Description (continued)

Bits per Pixel	Pixels per LD* (1:1 muxing)	Pixels per LD* (4:1 muxing)	Pixels per LD* (5:1 muxing)	Colors Displayed
1	8	32	40	2
2	N/A	16	20	4
4	N/A	8	10	16
8	N/A	4	5	256

Table 2. Block Mode Operation.

1 Bit per Pixel (RA1–RA7 = 0) RA0 =	2 Bits per Pixel (RA2–RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4–RA7 = 0) RA3–RA0 =	8 Bits per Pixel RA7–RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0–P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode.

Table 3. Block Mode Operation (RA = Color Palette RAM Address).

Circuit Description (continued)

On-Chip Cursor Operation

The Bt459 has an on-chip, three-color, 64 x 64 pixel user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor (x,y) register. The Bt459 expects (x) to increase to the right and (y) to increase down, as displayed on the screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 5.)

Three-Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

A (0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each plane of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the thirty-first column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the thirty-first row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63).

Cross Hair Cursor

The three-color cross hair cursor is also positioned through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than 1 pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) specifies the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is displayed only within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, *the software must ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.*

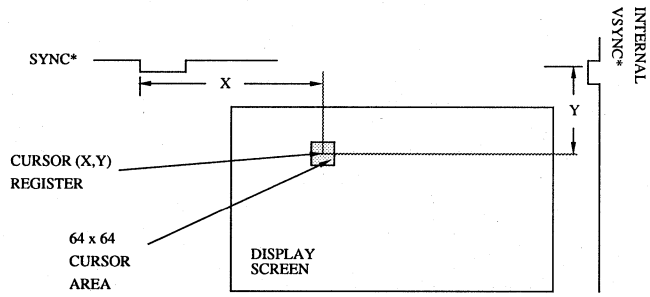


Figure 5. Cursor Positioning.

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000, and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 6.)

Dual-Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.
The cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, it will be 1 pixel off from being truly centered about the cross hair cursor.

Figure 7 illustrates dual-cursor display.

In the 64 x 64 pixel area in which the user-definable cursor is displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will depend on the cursor pattern, whether it is logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 8 shows the equivalent cursor generation circuitry.

X Windows Cursor Mode

In the X Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Figure 12 in the Internal Registers section shows the organization of the cursor RAM while in the X Windows mode..

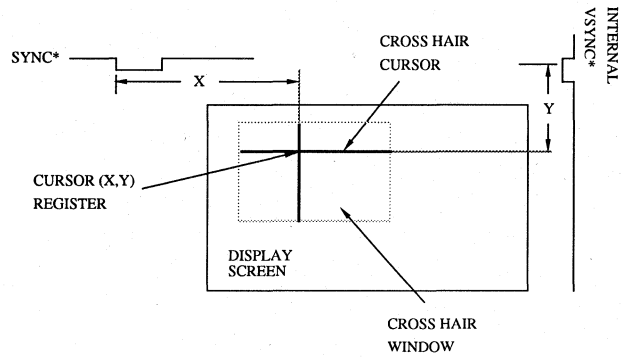


Figure 6. Cross Hair Cursor Positioning.

Circuit Description (continued)

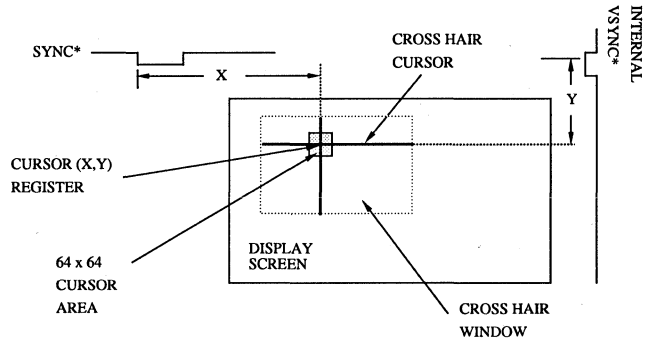


Figure 7. Dual-Cursor Positioning.

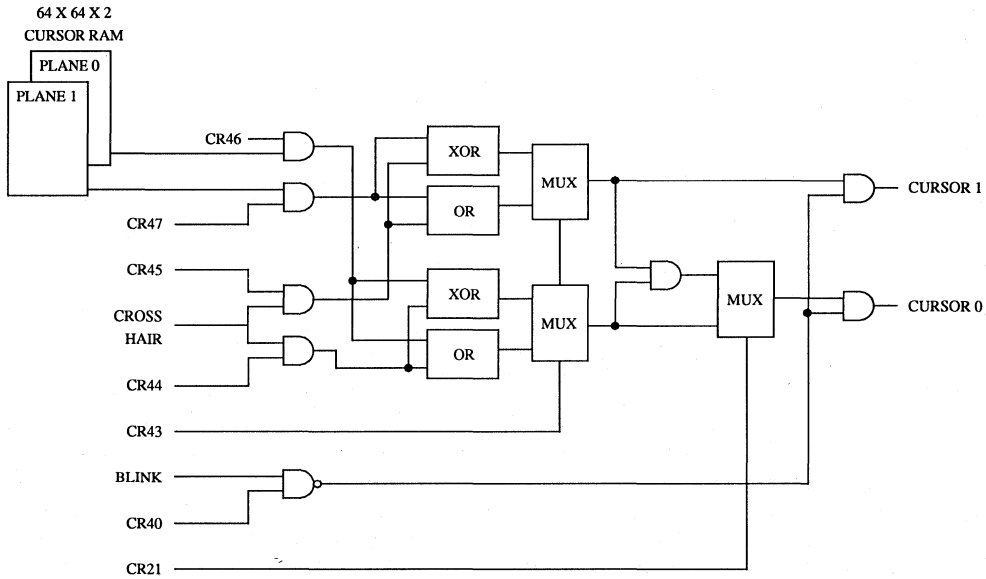


Figure 8. Cursor Control Circuitry.

Circuit Description (continued)

Overlay/Underlay Operation

The overlay inputs (OL0–OL3 and OLE) may operate in three modes: normal overlays, X Windows overlays, or an underlay, as specified in Tables 4 and 5.

Overlay and underlay information may be displayed on a pixel basis. Overlays and underlay may both be used. If X Windows overlays are used, the underlay is not available.

The priority of display operation is:

1. Cursor
2. Overlays
3. Pixel Data
4. Underlays

The Bt459 must be reset to an eight-cycle pipeline delay for proper cursor pixel alignment.

Cursor1, Cursor0	CR30	CR22	OLE	CR05	OL0–OL3	P0–P7	Addressed by frame buffer	Overlay Mode
11	x	x	x	x	$x	$xx	cursor color 3	
10	x	x	x	x	$x	$xx	cursor color 2	
01	x	x	x	x	$x	$xx	cursor color 1	
00	0	0	x	x	$F	$xx	overlay color 15	normal
:	:	:	:	:	:	:	:	
00	0	0	x	x	$1	$xx	overlay color 1	
00	0	0	x	1	$0	$xx	overlay color 0	
00	0	0	x	0	$0	$00	RAM location $00	
00	0	0	x	0	$0	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	0	0	x	0	$0	$FF	RAM location $FF	
00	x	1	1	x	$F	$xx	overlay color 15	X Windows
:	:	:	:	:	:	:	:	
00	x	1	1	x	$1	$xx	overlay color 1	
00	x	1	1	x	$0	$xx	overlay color 0	
00	x	1	0	0	$x	$00	RAM location $00	
00	x	1	0	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	x	1	0	0	$x	$FF	RAM location $FF	
00	1	0	x	x	$F	$xx	overlay color 15	underlay
:	:	:	:	:	:	:	:	
00	1	0	x	x	$1	$xx	overlay color 1	
00	1	0	1	x	$0	$00	overlay color 0 (underlay)	
00	1	0	0	0	$x	$00	RAM location $00	
00	1	0	x	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	1	0	x	0	$x	$FF	RAM location $FF	

Figure 8 shows generation of Cursor1 and Cursor0 control bits.

Table 4. Palette and Overlay Select Truth Table.

Circuit Description (continued)

In normal overlay mode, the overlay enable inputs OLE {A–E} are ignored. Typically, only 15 overlays are available. Graphics information (P0–P7) is displayed only when no overlay information is present (OL0–OL3 = 0000).

In the X Windows overlay mode, the overlay enable inputs specify whether overlay information is present (OLE = 1) or not (OLE = 0). If OLE = 1, overlay information is displayed as determined by OL0–OL3. If OLE = 0, the OL0–OL3 inputs are ignored and P0–P7 pixel data is displayed.

In the underlay mode (CR30 = 1), if OLE = 0, pixel data is displayed. If OLE = 1, the underlay is displayed if P0–P7 = 0; if P0–P7 ≠ 0, pixel data is displayed. Overlay color 0 is used for underlay color information.

	P0–P7 Pixel Inputs						
	1:1 Mux	Block Mode	Interleave	Panning	Zooming	Overlays	Underlay
Block Mode	no	-	yes	yes	n/s	n/a	n/a
Interleave	n/s	yes	-	yes	yes	yes	yes
Panning	n/s	n/s	yes	-	yes	n/a	yes
Zooming	n/s	n/s	yes	yes	-	n/a	n/a
Overlays	yes	yes	yes	n/a	n/a	-	yes
Underlay	yes	yes	yes	yes	n/a	yes	-
Cursor	n/a	n/a	n/a	n/a	n/a	n/a	n/a

yes: fully functional together.
n/s: functions not supported together.
n/a: functions operate together, but do not affect each other.

Table 5. Features and Function Compatibility Table.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

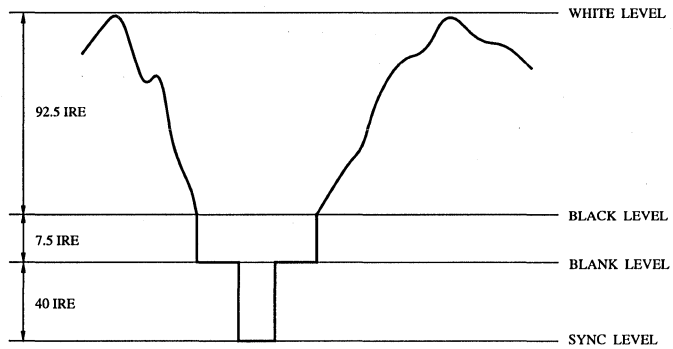
The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 9 and 10. Command Register 2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt459 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 9. Composite Video Output Waveform (SETUP = 7.5 IRE).

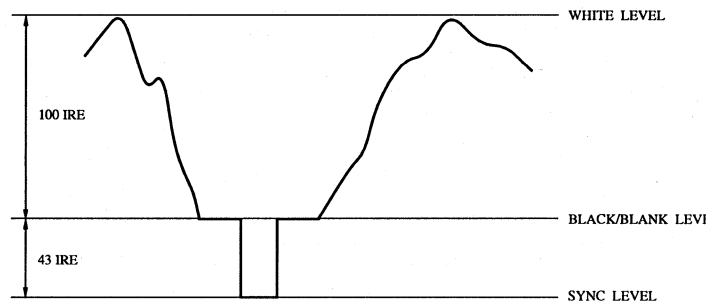
Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET =523 and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 10. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06 — Multiplex select

- (00) reserved
- (01) 4:1 multiplexing
- (10) 1:1 multiplexing
- (11) 5:1 multiplexing

These bits specify whether 1:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth the CLOCK rate. If 1:1 is specified, the {B}, {C}, {D}, and {E} inputs are ignored.

In the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

It is possible to reset the pipeline delay of the Bt459 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt459 must again be reset to a fixed pipeline delay.

CR05 — Overlay 0 enable

- (0) use color palette RAM
- (1) use overlay color 0

When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 4.

CR04 — reserved (logical zero)

CR03, CR02 — Blink rate selection

- (00) 16 on, 48 off (25/75)
- (01) 16 on, 16 off (50/50)
- (10) 32 on, 32 off (50/50)
- (11) 64 on, 64 off (50/50)

These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off). The counters that determine the blink rate are reset when command register_0 is written to.

CR01, CR00 — Block mode

- (00) 8 bits per pixel
- (01) 4 bits per pixel
- (10) 2 bits per pixel
- (11) 1 bit per pixel

These bits specify whether the pixel data is input as 1, 2, 4, or 8 bits per pixel. Only the P0–P7 inputs are affected.

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15 Pan select

(000)	0 pixels	{pixel A}
(001)	1 pixel	{pixel B}
(010)	2 pixels	{pixel C}
(011)	3 pixels	{pixel D}
(100)	4 pixels	{pixel E}
(101)	reserved	
(110)	reserved	
(111)	reserved	

These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval, and should be set to 000 in the 1:1 multiplex mode. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, {pixel C} indicates pixel C will be output first, etc.

Only pixel and underlay information is panned. Overlay and cursor information is not panned.

CR14 reserved (logical zero)

In the 1:1 multiplex mode, 0 pixels should be specified.

CR13–CR10 Zoom factor

(0000)	1x
(0001)	2x
:	
(1111)	16x

These bits specify the amount of zooming to implement. For 2x zoom, pixel {A} is output for two clock cycles, followed by pixel {B} for two clock cycles, followed by pixel {C} for two clock cycles, etc. For 3x zoom, pixel {A} is output for three clock cycles, and so on.

In the 1:1 multiplex mode, only the {A} pixels are output, and 1x zoom should be selected.

Only P0–P7 are zoomed.

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt459 with three write cycles (red, green, and blue), and color data is output with three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt459 to emulate a single-channel RAMDAC using only the green channel. The Bt459 expects color data to be input and output with (red, green, blue) cycles. The exact value indicates during which *one* of the three color cycles it is to load or output color information. The value is loaded into or read from the green color palette RAM.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* to generate PLL information.
CR22	X Windows overlay select (0) normal overlays (1) X Windows overlays	This bit specifies whether the overlays are to operate normally (logical zero) or in an X Windows environment (logical one).
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X Windows-compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37–CR35 Interleave select

(000) 0 pixels
(001) 1 pixel
(010) 2 pixels
(011) 3 pixels
(100) 4 pixels
(101) reserved
(110) reserved
(111) reserved

These bits specify the order in which the pixels are to be output, as listed in Table 8. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line.

The phrase "repeats every x" in Table 8 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1-pixel interleave select, ABCD would be repeated every fourth scan line.

When the Bt459 is in the 1:1 input multiplex mode, a value of 0 pixels(000) must be specified.

CR34–CR32 First pixel select

(000) pixel {A}
(001) pixel {B}
(010) pixel {C}
(011) pixel {D}
(100) pixel {E}
(101) reserved
(110) reserved
(111) reserved

These bits are used to support panning in the Y direction with an interleaved frame buffer. Because of the interleave capability, the value of the first pixel must be specified on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode.

These bits are ignored when the Bt459 is in the 1:1 multiplex mode.

CR31 Overlay interleave enable

(0) interleaving disabled
(1) interleave enabled

This bit specifies whether OL0–OL3 and OLE are to be interleaved. If interleaving is enabled, the interleave factor and first pixel selection are the same as that for P0–P7. If interleaving is disabled, pixel {A} is output first, and no interleaving occurs.

CR30 Underlay enable

(0) underlay disabled
(1) underlay enabled

If command bit CR22 is a logical zero, this bit enables or disables the underlay display. If CR22 is a logical one, this bit is ignored.

If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0–P7 data is displayed. If OLE = 1, the underlay is displayed if P0–P7 = 0, if P0–P7 ≠ 0, normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Internal Registers (continued)

Interleave Register (continued)

	5:1 multiplexing		4:1 multiplexing	
interleave select	**output sequence**	**scan line number**	**output sequence**	**scan line number**
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 8. Interleave Operation (First Pixel Select = Pixel A).

Internal Registers (continued)

Interleave Zoom Enable

If zooming while interleaving, the IZE* input pin indicates when to change the interleave sequence.

For example, while interleaving with 3x zoom, the IZE* pin should be a logical zero during the blanking interval of every third scan line (as shown in Figure 11). IZE* may be asserted coincident with the falling edge of BLANK* but must remain low at least 16 LD* cycles after the falling edge of BLANK*.

If zooming is not required (1x zoom), the IZE* should be a logical zero or be connected directly to GND.

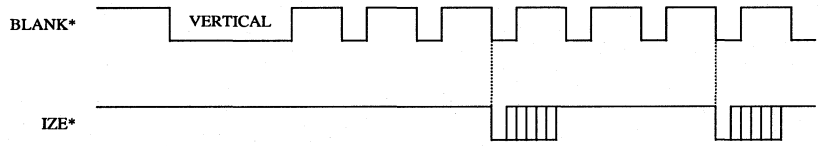


Figure 11. Interleave and Zoom Operation (3x Zoom Example).

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt459, the value read by the MPU will be $4A. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D3 corresponds to overlay plane 3 (OL3 {A–E}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D3 corresponds to overlay plane 3 (OL3 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Revision Register (Revision B only)

This 8-bit register is a read-only register, specifying the revision of the Bt459. The 4 most significant bits signify the revision letter B in hexidecimal form. The 4 least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since the Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Internal Registers (continued)

Red, Green, and Blue Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the three registers are concatenated and a 24-bit signature is acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. The Application Information, Test Register section contains more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

Test Register

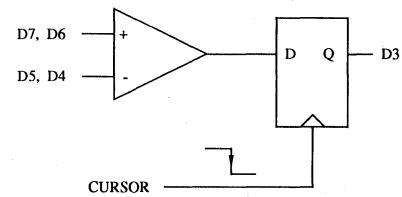
This 8-bit register is used to test the Bt459. If 1:1 pixel multiplexing is specified, signature analysis is performed on every pixel; if 4:1 pixel multiplexing is specified, signature analysis is performed on every fourth pixel; if 5:1 pixel multiplexing is specified, signature analysis is performed on every fifth pixel. D0–D2 are used for 4:1 and 5:1 multiplexing to specify whether to use the A, B, C, D, or E pixel inputs, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 150 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 150 mV reference	red > 150 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 150 mV reference	green > 150 mV	green < 145 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be a logical zero.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt459. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	This bit specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	This bit specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	This bit specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	This bit specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is 1, 3, 5, or 7 pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized, and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–P

where

P = 37 if 1:1 input multiplexing, 52 if 4:1 input multiplexing, 57 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of SYNC* to active video

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the second sync pulse during vertical blanking to active video

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized, and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

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The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–P

where

P = 5 if 1:1 input multiplexing, 20 if 4:1 input multiplexing, 25 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of HSYNC* to active video

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the second sync pulse during vertical blanking to active video

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000, and the window width and height registers with $0FFF.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized, and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 input multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels for 1:1, 4:1, and 5:1 multiplexing, respectively. The minimum window height is 2 pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers (continued)

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window and is not initialized.

For Revision A, the cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention. If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the user position the cursor offscreen in the Y direction [i.e., write to the cursor (y) registers and wait for the vertical sync interval to move the cursor offscreen], write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write-then-read sequence, and if the correct cursor RAM data was not written, perform another write then read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

For Revision B, cursor contention has been eliminated. The cursor RAM may be written to or read by the MPU at any time without contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 12 illustrates the internal format of the cursor RAM as it appears on the display screen. Addressing starts at location $400 as specified in Table 1.

In the X Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

In both modes of operation, plane1 = D7, D5, D3, D1; and plane0 = D6, D4, D2, D0.

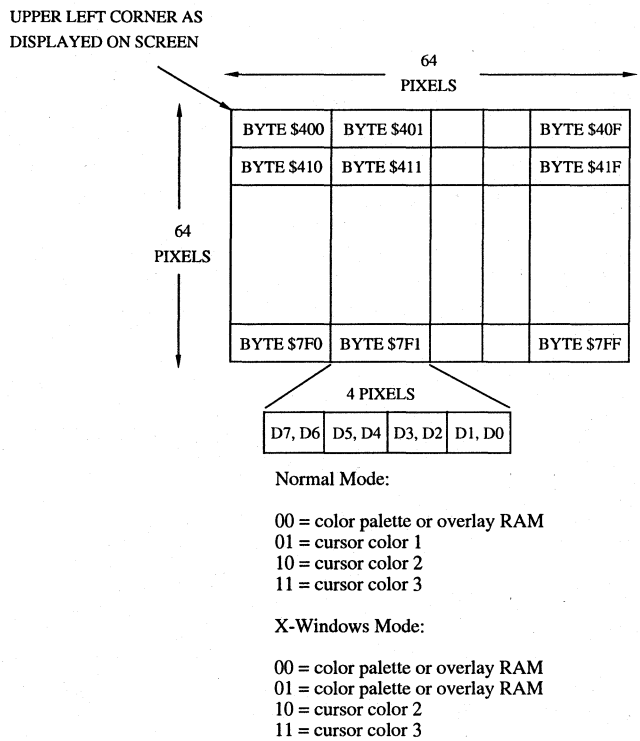

Figure 12. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 6 and 7. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL3 {A–E}, OLE {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is the output clock (1:1 multiplex mode) or while LD* is one fourth or one fifth of CLOCK, LD* may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 4). Either 1, 4, or 5 consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, followed by the {C} pixel, etc., until all pixels (1, 4, or 5) have been output, at which point the cycle repeats.
OL0– OL3 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as detailed in Table 4. When the overlay palette RAM is being accessed, the P0–P7 {A–E} inputs are ignored. Overlay information (up to 4 bits per pixel) for either 1, 4, or 5 consecutive pixels is input through this port. Unused inputs should be connected to GND.
OLE {A–E}	Overlay enable inputs (TTL compatible). In the X Windows mode for overlays, a logical one indicates overlay information is to be displayed. A logical zero indicates P0–P7 information is to be displayed. In the normal mode for overlays, these inputs are ignored. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt459s to be synchronized with subpixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND either directly or through a resistor of up to 150 Ω.
IZE*	Interleave zoom enable input (TTL compatible). This input should be a logical zero for a minimum of 16 LD* cycles after the falling edge of BLANK* during scan lines that require an interleave shift. If zoom while interleaving is not supported, this pin may be connected directly to GND.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 13). When the capacitor is connected to VAA rather than to GND, the highest possible power supply noise rejection is provided. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *The PC Board Layout Considerations section contains critical layout criteria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 13). The IRE relationships in Figures 9 and 10 are maintained regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = K1 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω) where K1 and K2 are defined as:
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 13. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as specified in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

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Pin Descriptions (continued)—132-pin PGA Package

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L1	OL0A	E1	GND	H1
SYNC*	K3	OL0B	F2	GND	H2
LD*	A5	OL0C	F1	GND	H3
CLOCK	K1	OL0D	G3	GND	C7
CLOCK*	K2	OL0E	G2	GND	G12
IZE*	B5			GND	M8
		OL1A	M1	GND	M7
P0A	E3	OL1B	L2	GND	N7
P0B	D2	OL1C	N1		
P0C	D1	OL1D	L3	COMP	N9
P0D	E2	OL1E	M2	FS ADJUST	M10
P0E	F3			VREF	P9
		OL2A	M3		
P1A	A1	OL2B	N2	CE*	P13
P1B	D3	OL2C	P1	R/W	N12
P1C	C2	OL2D	P2	C1	P12
P1D	B1	OL2E	N3	C0	M11
P1E	C1				
		OL3A	M4	D0	L13
P2A	A3	OL3B	P3	D1	M14
P2B	B3	OL3C	N4	D2	L12
P2C	A2	OL3D	P4	D3	M13
P2D	C3	OL3E	M5	D4	N14
P2E	B2			D5	P14
		OLEA	N5	D6	N13
P3A	A8	OLEB	P5	D7	M12
P3B	A7	OLEC	M6		
P3C	B7	OLED	N6	reserved	G14
P3D	A6	OLEE	P6	reserved	G13
P3E	B6			reserved	F14
		IOG	P10	reserved	F13
P4A	C9	IOB	P11	reserved	E14
P4B	B9	IOR	N10	reserved	J13
P4C	A9	PLL	N11	reserved	J14
P4D	C8			reserved	H12
P4E	B8	VAA	J1	reserved	H13
		VAA	J2	reserved	H14
P5A	B11	VAA	J3	reserved	C5
P5B	A11	VAA	C6	reserved	A4
P5C	C10	VAA	F12	reserved	B4
P5D	B10	VAA	M9	reserved	C4
P5E	A10	VAA	P7	reserved	C14
		VAA	P8	reserved	C13
P6A	A14	VAA	N8	reserved	B14
P6B	A13			reserved	C12
P6C	B12			reserved	B13
P6D	C11			reserved	L14
P6E	A12			reserved	K12
				reserved	J12
P7A	E13			reserved	K14
P7B	E12			reserved	K13
P7C	D14				
P7D	D13				
P7E	D12				

Pin Descriptions (continued)—132-pin PGA Package

Bt459

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	N/C	N/C	N/C	N/C	N/C	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	N/C	N/C	N/C	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	PLL	IOB
10	P5E	P5D	P5C									FS ADJ	IOR	IOG
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	VAA	VAA
7	P3B	P3C	GND									GND	GND	VAA
6	P3D	P3E	VAA									OLEC	OLED	OLEE
5	LD*	IZE*	N/C									OL3E	OLEA	OLEB
4	N/C	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

Alignment Marker (on Top)

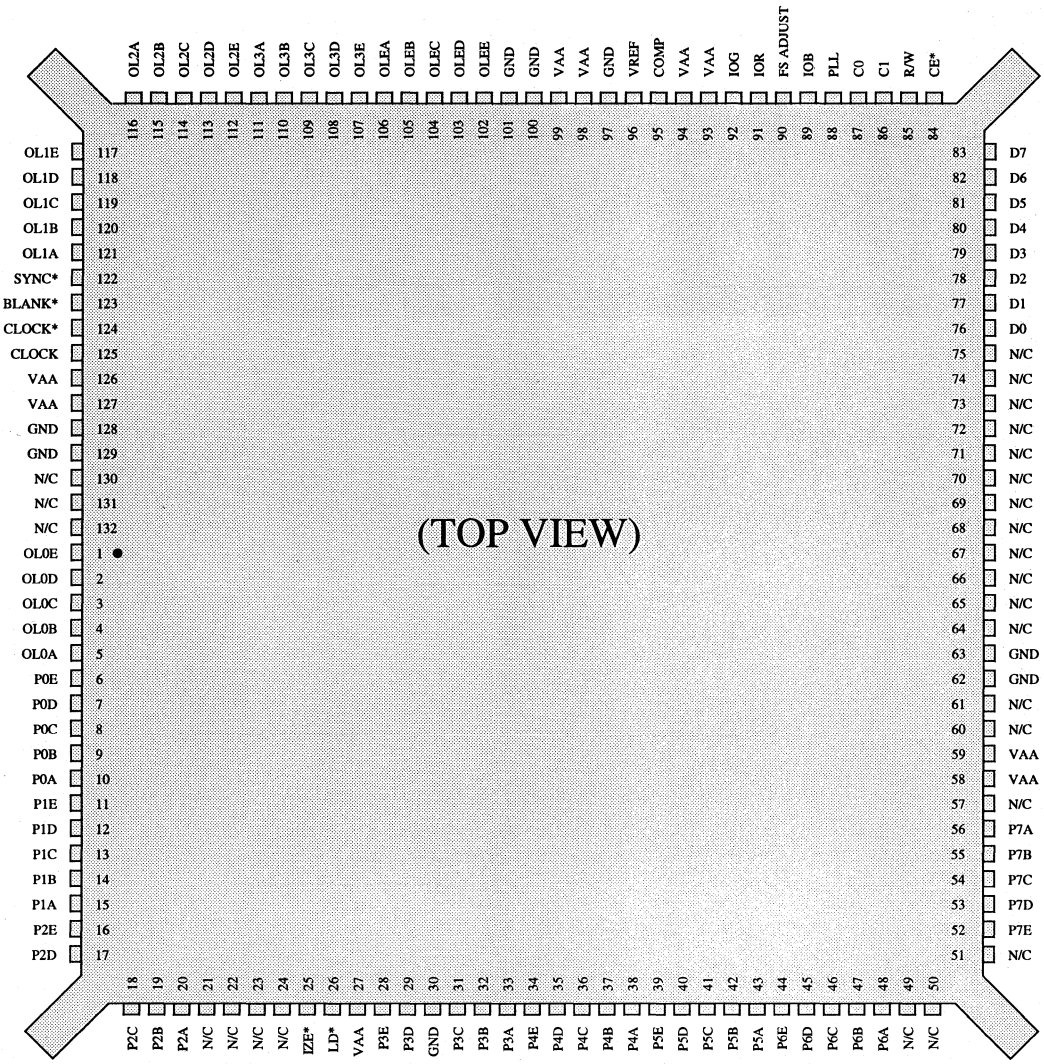
(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	N/C	N/C	N/C	N/C	N/C	N/C	N/C	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	N/C	N/C	N/C	N/C	N/C	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	N/C	N/C	N/C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	IOB	PLL	C0									P6D	P5A	P5B
10	IOG	IOR	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	VAA	VAA	GND									P4D	P4E	P3A
7	VAA	GND	GND									GND	P3C	P3B
6	OLEE	OLED	OLEC									VAA	P3E	P3D
5	OLEB	OLEA	OL3E									N/C	IZE*	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	N/C
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

Pin Descriptions (continued)—132-pin PQFP Package

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	OL0E	44	P6E	88	PLL
2	OL0D	45	P6D	89	IOB
3	OL0C	46	P6C		
4	OL0B	47	P6B	90	FS ADJUST
5	OL0A	48	P6A	91	IOR
				92	IOG
6	P0E	49	reserved	93	VAA
7	P0D	50	reserved	94	VAA
8	P0C	51	reserved	95	COMP
9	P0B			96	VREF
10	P0A	52	P7E	97	GND
		53	P7D	98	VAA
11	P1E	54	P7C	99	VAA
12	P1D	55	P7B	100	GND
13	P1C	56	P7A	101	GND
14	P1B				
15	P1A	57	reserved	102	OLEE
		58	VAA	103	OLED
16	P2E	59	VAA	104	OLEC
17	P2D	60	reserved	105	OLEB
18	P2C	61	reserved	106	OLEA
19	P2B	62	GND		
20	P2A	63	GND	107	OL3E
		64	reserved	108	OL3D
21	reserved	65	reserved	109	OL3C
22	reserved			110	OL3B
23	reserved	66	reserved	111	OL3A
24	reserved	67	reserved		
25	IZE*	68	reserved	112	OL2E
		69	reserved	113	OL2D
26	LD*	70	reserved	114	OL2C
27	VAA			115	OL2B
		71	reserved	116	OL2A
28	P3E	72	reserved		
29	P3D	73	reserved	117	OL1E
30	GND	74	reserved	118	OL1D
31	P3C	75	reserved	119	OL1C
32	P3B			120	OL1B
33	P3A	76	D0	121	OL1A
		77	D1		
34	P4E	78	D2	122	SYNC*
35	P4D	79	D3	123	BLANK*
36	P4C	80	D4	124	CLOCK*
37	P4B	81	D5	125	CLOCK
38	P4A	82	D6		
		83	D7	126	VAA
39	P5E			127	VAA
40	P5D	84	CE*	128	GND
41	P5C	85	R/W	129	GND
42	P5B	86	C1		
43	P5A	87	C0	130	reserved
				131	reserved
				132	reserved

Pin Descriptions (continued)—132-pin PQFP Package



5

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt459, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook.*

The layout should be optimized for lowest noise on the Bt459 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt459 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt459 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 13. This bead should be located within 3 inches of the Bt459. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device and should use the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins, and should be connected with short, wide traces.

The 33 µF capacitor shown in Figure 13 is for low-frequency power supply ripple. The 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1-µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

PC Board Layout Considerations (continued)

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Alternate PCB pads (one to VAA and one to GND) are recommended for the VREF decoupling capacitor.

Digital Signal Interconnect

The digital inputs to the Bt459 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt459 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt459 to minimize reflections. Unused analog outputs should be connected to GND.

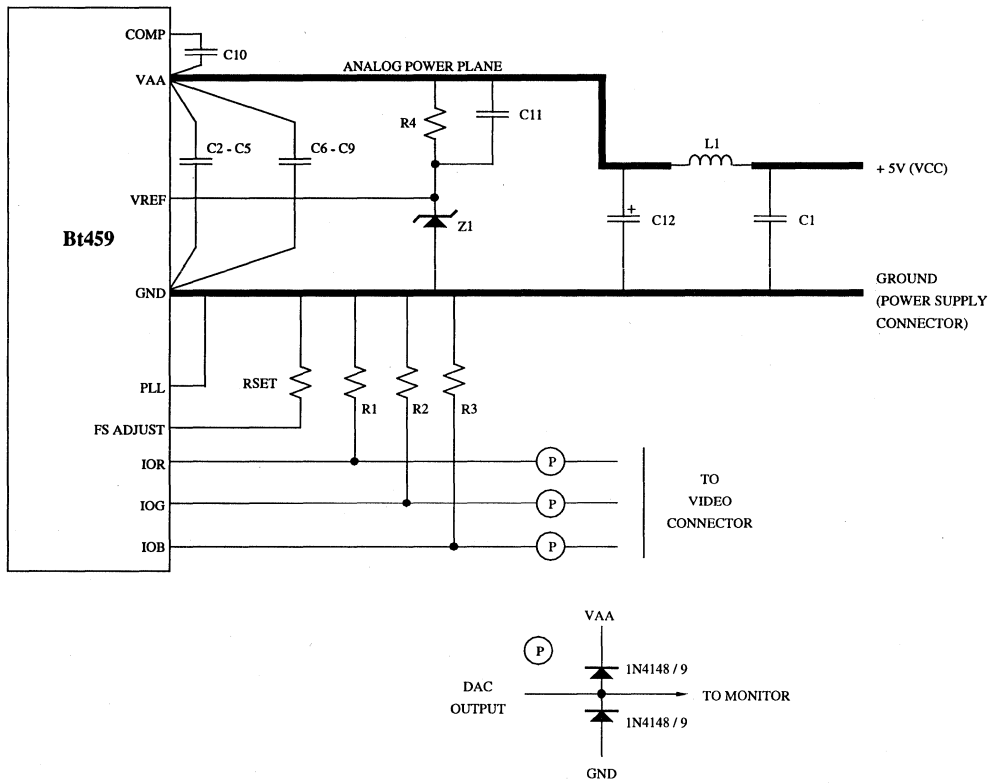
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt459 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt459.

Figure 13. Typical Connection Diagram and Parts List.

Clock Interfacing

Because of the high clock rates at which the Bt459 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 14.)

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak because of the noise margins of the CMOS process. The Bt459 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified), and translating the result to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt459 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, and will optionally set the pipeline delay of the Bt459 to eight clock cycles. The Bt438 may also be used to interface the Bt459 to a TTL clock. Figure 14 illustrates the Bt438 used with the Bt459.

When using a single Bt459, the PLL output is ignored and should be connected to GND (either directly or through a resistor of up to 150 Ω).

Using Multiple Bt459s

For display applications where up to four Bt459s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, synchronizes them to subpixel resolution and sets the pipeline delay of the Bt459 to eight clock cycles. The Bt439 may also be used to interface the Bt459 to a TTL clock. Figure 15 illustrates the Bt439 used with the Bt459.

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt459, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt459s, and adjusts the delay of each of the CLOCK and CLOCK* signals to the Bt459s to minimize the PLL delay difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

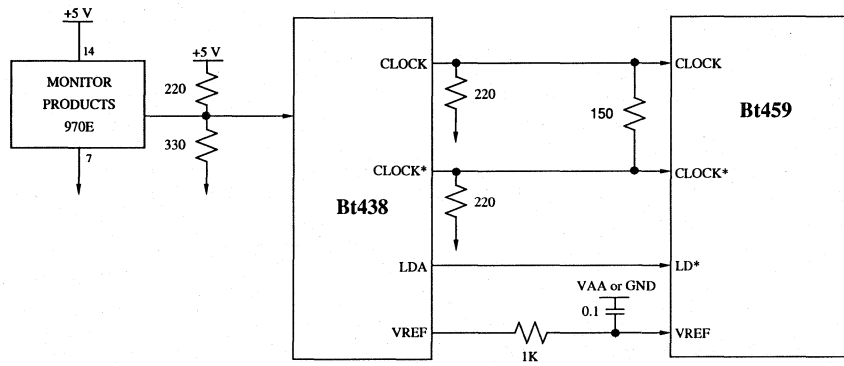


Figure 14. Generating the Bt459 Clock Signals.

Application Information (continued)

If subpixel synchronization of multiple Bt459s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt459s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt459s must still have a 0.1 µF bypass capacitor to VAA, and individual voltage references. The designer must minimize skew on the CLOCK and CLOCK* lines. The PLL outputs of the Bt459s will not be used and should be connected to GND (either directly or through a resistor of up to 150 Ω).

When multiple Bt459s are used, each Bt459 should have its own power plane ferrite bead and voltage reference. Each Bt459 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

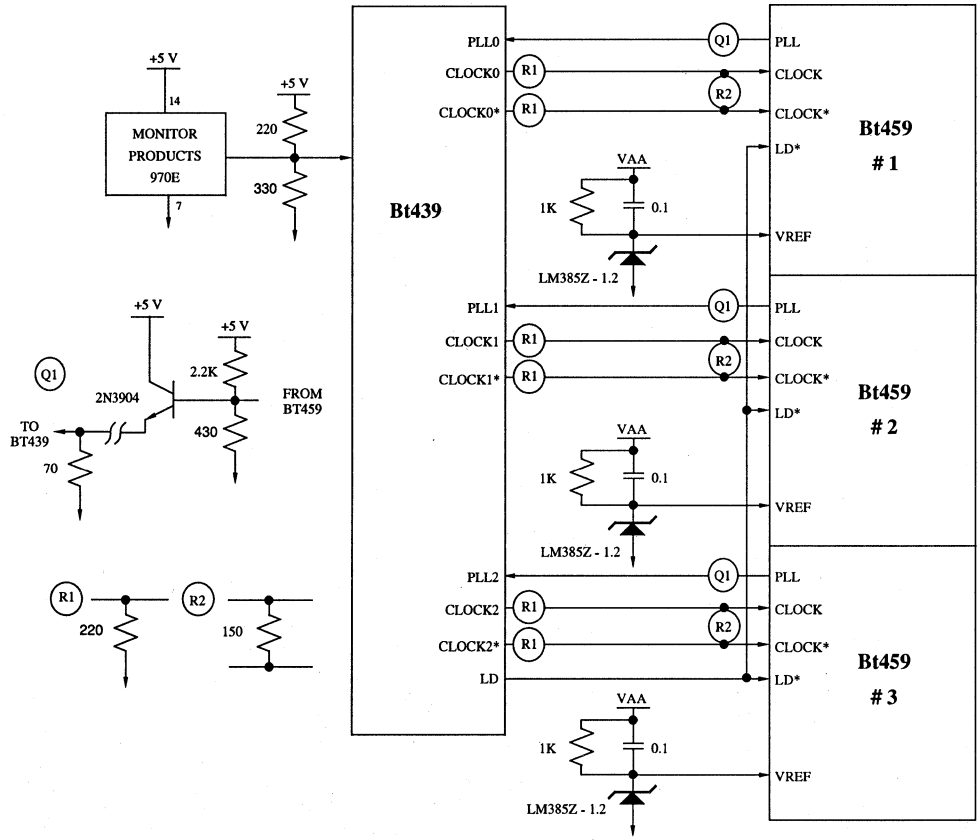


Figure 15. Generating the Clock Signals for Multiple Bt459s.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt459, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt459 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438, Bt439, and Bt440 Clock Generator Chips support this mode of operation when used with the Bt459. It is strongly recommended that the Bt438, Bt439, or Bt440 be used for clock generation when multiple Bt459s are used or when a fixed pipeline of eight clock cycles is necessary.

To reset the Bt459, it should be powered up with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

To ensure that the Bt459 has the proper configuration, all the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power-up that occurs prior to initialization of the command registers cannot be used to assume the fixed pipeline. An additional reset is required after command register writes.

When the Bt459 is reset to an eight-clock-cycle pipeline delay, the blink counter circuitry is not reset. Therefore, if the multiple Bt459s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control through the read mask register and overlay display enable bits.

The Bt459 must be reset to an eight-clock-cycle pipeline delay for proper cursor pixel alignment.

Interleave Operation

To support interleaved frame buffers, the Bt459 may be configured for various interleave factors, as shown in Table 8. Table 9 is an example of interleave operation for 4:1 multiplexing, an interleave select of 3, and starting with pixel {A}. Table 10 is an example of the same operation with pixel {B} selected as the starting pixel (with the display panned down three scan lines).

Scan line number 0 corresponds to the top of the display screen and is the first displayed scan line after a vertical blanking interval. The output sequence is shown starting at the left-most displayed pixel.

Scan Line	Output Sequence
0	ABCDABCD...
1	DABCDABC...
2	CDABCDAB...
3	BCDABCDA...
4	ABCDABCD...
5	DABCDABC...
6	CDABCDAB...
7	BCDABCDA...
:	:

Table 9. Interleave Example.

Scan Line	Output Sequence
0	BCDABCDA...
1	ABCDABCD...
2	DABCDABC...
3	CDABCDAB...
4	BCDABCDA...
5	ABCDABCD...
6	DABCDABC...
7	CDABCDAB...
:	:

Table 10. Interleave Example.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt459

The Bt459 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section explains the operating use of these test features.

Signature Register (Signature Mode)

The signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color. They are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs.

The SARs act as a 24-bit wide linear feedback shift register on each succeeding pixel that is latched. It is important to note that in either the 4:1 or 5:1 multiplexed mode the SARs latch only 1 pixel per load group. Thus, the SARs are operating on only every fourth or fifth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, or E) is latched to generate new signatures by setting bits D0–D2 in the test register.

In 1:1 mux mode, the SARs will generate signatures truly on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (Test Register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt459 will only generate signatures while it is in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt459 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan line or one frame buffer of pixels, will be input to the chip. At the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested with the signature registers.

Assuming the chip is running 4:1 or 5:1 mux modes, the above process would be repeated with all different pixel phases (A, B, C, etc.) selected.

The linear feedback configuration is shown in Figure 16. Each register internally uses XORs at each input bit (D_n) with the output (result) by 1 least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can by used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Signature Register (Data-Strobe Mode)

Setting command bit CR20 to "1" puts the SARs into data-strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the generation of signatures by the SARs. Instead, the SARs capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read out a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt459. The levels of most inputs do not matter *except* that CLOCK should be high and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

Application Information (continued)

In general, the color read out will correspond to a pixel latched on the previous load. However, because the data path is pipelined, the color may come from an earlier load cycle. To read successive pixels:

1. Toggle LD*.
2. Pulse the CLOCK pins according to the mux state (one, four, or five periods).
3. Hold all pixel-related inputs.
4. Perform the three MPU reads as described.

This process is best done on a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt459, the analog output comparator, allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected through the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register on each of the 64 scan lines of the 64 x 64 user-defined cursor block. (The 64 x 64 cursor must be enabled for display.) On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point occurs over the left-most edge of the 64 x 64 cursor block.

Because the comparator is a simple design, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading test register bit D3.

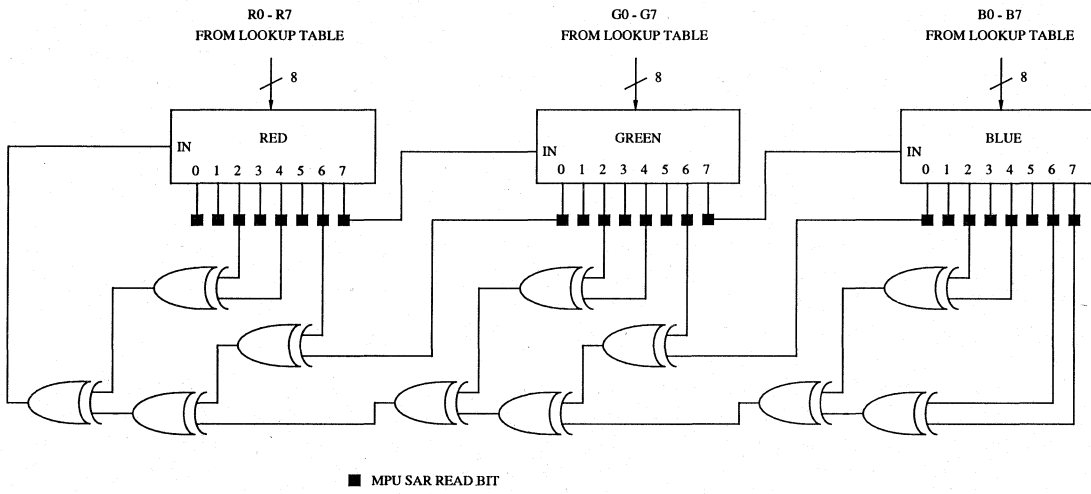


Figure 16. Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt459

Following a power-on sequence, the Bt459 must be initialized. This sequence will configure the Bt459 as follows:

- 4:1 multiplexed operation
- no overlays, no blinking, and no interleave
- 64 x 64 block cursor and no cross hair cursor
- 8 bits per pixel, no panning, and no zoom
- sync enabled on IOG and a 7.5 IRE blanking pedestal

Control Register Initialization	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to interleave register	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern	
Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization	
Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization	
Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω
Air Flow (Note 1)		50			l.f.p.m.

Note 1: Required for Bt459KPF150 only.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
PQFP	TJ			+150	°C
PGA	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance	CAOUT		13	20	pF
(f = 1 MHz, IOUT = 0 mA)					
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–0.5		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance			8	15	pF
(f = 1 MHz, PLL = 0 mA)					
Voltage Reference Input Current	IREF				
Rev. A			500		µA
Rev. B			10		µA
Power Supply Rejection Ratio	PSRR		0.5		% / % ΔVAA
(COMP = 0.1 µF, f = 1 kHz)					

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	150 MHz	135 MHz	110 MHz	80 MHz	Units
Clock Rate	Fmax	max	150	135	110	80	MHz
LD* Rate	LDmax						
1:1 multiplexing		max	50	50	50	50	MHz
4:1 multiplexing		max	37.50	33.75	27.5	20	MHz
5:1 multiplexing		max	30	27	22	16	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	10	10	10	10	ns
CE* Low Time	3	min	40	40	40	40	ns
CE* High Time	4	min	20	20	20	20	ns
CE* Asserted to Data Bus Driven	5	min	10	10	10	10	ns
CE* Asserted to Data Valid	6	max	75	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	15	15	ns
Write Data Setup Time	8	min	15	15	15	15	ns
Write Data Hold Time	9	min	2	2	2	2	ns
Pixel and Control Setup Time	10	min	3	3	3	3	ns
Pixel and Control Hold Time	11	min	2	2	2	2	ns
Clock Cycle Time	12	min	6.67	7.4	9.09	12.5	ns
Clock Pulse Width High Time	13	min	2.7	3.2	4	5	ns
Clock Pulse Width Low Time	14	min	2.7	3.2	4	5	ns
LD* Cycle Time	15						
1:1 multiplexing		min	20	20	20	20	ns
4:1 multiplexing		min	26.67	29.63	36.36	50	ns
5:1 multiplexing		min	33.33	37.04	45.45	62.5	ns
LD* Pulse Width High Time	16						
1:1 multiplexing		min	7	7	7	7	ns
4:1 or 5:1 multiplexing		min	11	12	15	20	ns
LD* Pulse Width Low Time	17						
1:1 multiplexing		min	7	7	7	7	ns
4:1 or 5:1 multiplexing		min	11	12	15	20	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	150 MHz	135 MHz	110 MHz	80 MHz	Units
Analog Output Delay	18	typ	12	12	12	12	ns
Analog Output Rise/Fall Time	19	typ	1.5	1.5	1.5	2	ns
Analog Output Settling Time	20	max	8	8	8	12	ns
Clock and Data Feedthrough (Note 1)		typ	–28	–28	–28	–28	dB
Glitch Impulse (Note 1)		typ	50	50	50	50	pV - sec
Analog Output Skew		typ	0	0	0	0	ns
		max	2	2	2	2	ns
Pipeline Delay		min	6	6	6	6	Clocks
		max	10	10	10	10	Clocks
VAA Supply Current (Note 2)	IAA	typ	260	240	220	200	mA
		max	385	360	335	300	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing notes in Figure 18. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Signature Analysis Register (SAR) functionality is not guaranteed at 150 MHz.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough; and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms

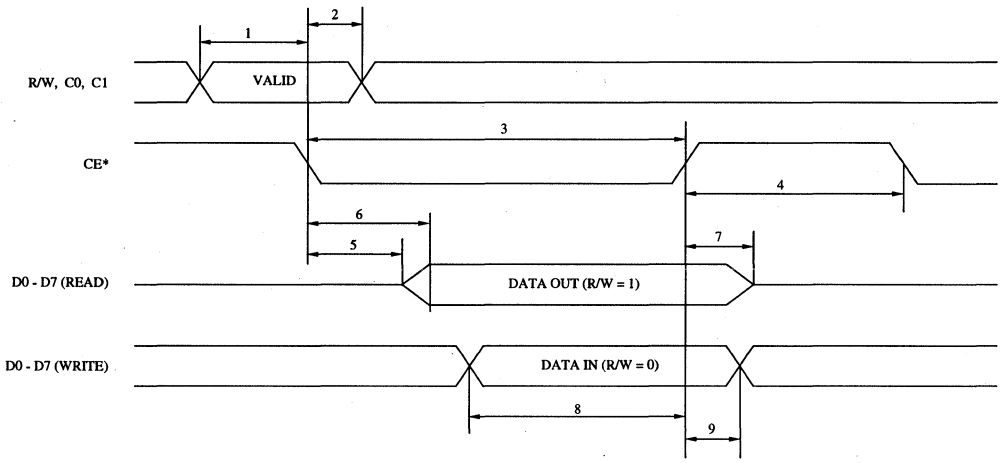
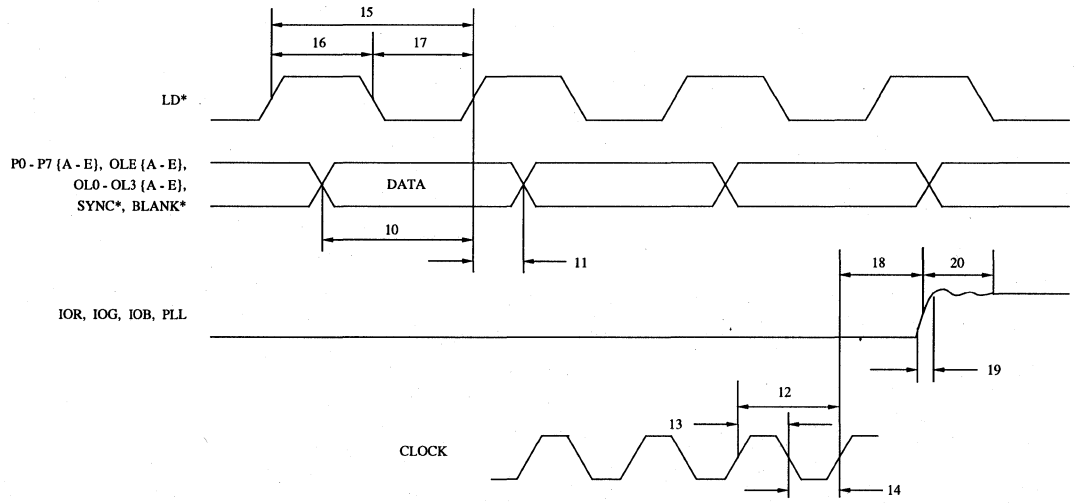


Figure 17. MPU Read/Write Timing Dimensions.



Note 1: Output delay time is measured from 50-percent point of the rising clock edge to 50-percent point of full-scale transition.

Note 2: Output settling time is measured from 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall timeis measured between 10-percent and 90-percent points of full-scale transition.

Figure 18. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt459KG150	150 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KG110	110 MHz	132-pin CeramicPGA	0° to +70° C
Bt459KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KPF150	150 MHz	132-pin Plastic Quad Flatpack	0° to +70° C with 50 LFPM Airflow
Bt459KPF135	135 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt459KPF110	110 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt459KPF80	80 MHz	132-pin Plastic Quad Flatpack	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt460

135 MHz
Monolithic CMOS
512 x 24 Color Palette
RAMDAC™

Distinguishing Features

- 135, 110 MHz Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- 512 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- 1x to 16x Integer Zoom Support
- Frame Buffer Interleave Support
- Pixel Panning Support
- On-Chip User-Definable 64 x 64 Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X-Windows Support for Overlays/ Cursor
- Standard MPU Interface
- 132-pin PGA Package

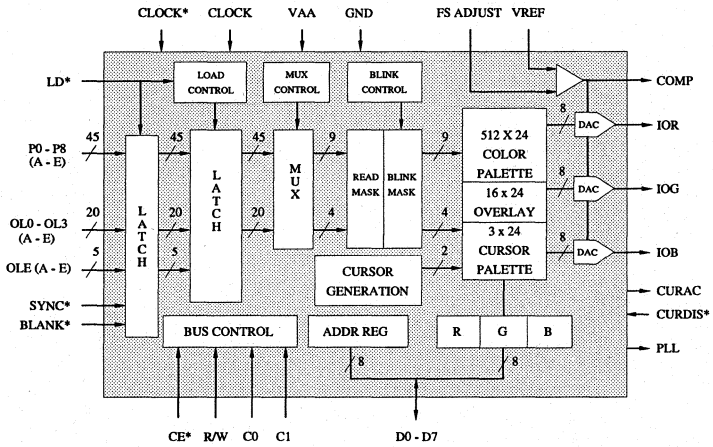
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt459, Bt462, Bt468

Functional Block Diagram



Product Description

The Bt460 triple 8-bit RAMDAC is designed specifically for high-performance, high- resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On-chip features include a 512 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, and 1x to 16x integer zoom support.

The Bt460 has an on-chip three-color 64 x 64 pixel cursor and a three-color full-screen (or full-window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

The Bt460 generates RS-343A compatible red, green, and blue video signals, and can drive doubly-terminated 75 Ω coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt460 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As shown in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

When accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

The address register resets to $0000 only after location $0FFF is accessed (because of wraparound).

Although the color palette RAM, overlay RAM, and cursor color registers are dual ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0 - 7)
$xxxx	01	address register (ADDR8 - 15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0 (Note 1)
:	10	:
$010F	10	overlay color 15 (Note 1)
$0181	10	cursor color register 1 (Note 1)
:	:	cursor color register 2 (Note 1)
$0183	10	cursor color register 3 (Note 1)
$0200	10	ID register ($4B)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register low
$0205	10	pixel read mask register high
$0206	10	pixel blink mask register low
$0207	10	pixel blink mask register high
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	interleave register
$020B	10	test register
$020C	10	red output signature register
$020D	10	green output signature register
$020E	10	blue output signature register
$020F	10	command register_3
$0210	10	input signature register
$0220	10	revision register ($B)
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$01FF	11	color palette RAM (Note 1)

Note 1: Requires three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

cycle, 1 or more of the pixels on the display screen can be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers and cursor RAM are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt460.

Single-Channel RAMDAC Operation

The Bt460 may be configured (through command register_2) to be a single-channel RAMDAC, enabling three Bt460s to be used in parallel for a 24-bit true-color system. The Bt460s share a common 8-bit data bus (D0–D7).

Each Bt460 must be configured to be either a red, green, or blue RAMDAC through command register_2. Only the green channel (IOG) of each RAMDAC is used; the IOR and IOB outputs should be connected to GND either directly or through a resistor up to 75 Ω.

To load the color palettes, the MPU performs the normal (red, green, blue) write cycles to all three RAMDACs simultaneously. The red Bt460 loads color data only during the the red write cycle, the green Bt460 loads color data only during the green write cycle, and the blue Bt460 loads color data only during the blue write cycle.

To read the color palettes, the MPU performs the normal (red, green, blue) read cycles from all three RAMDACs simultaneously. The red Bt460 outputs color data only during the the red read cycle, the green Bt460 outputs color data only during the green read cycle, and the blue Bt460 outputs color data only during the blue read cycle.

External circuitry must decode when the MPU is reading or writing to the color palettes and assert CE* to all three Bt460s simultaneously.

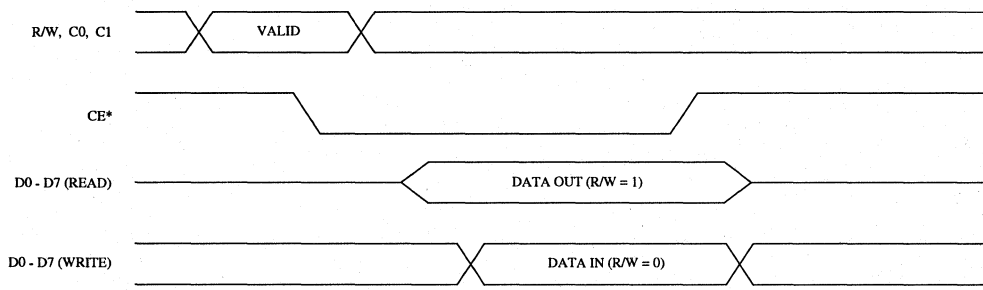


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt460 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for 1, 4, or 5 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 1-, 4-, or 5-pixel resolution. Typically, the LD* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

For 4:1 or 5:1 input multiplexing, the Bt460 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats. In the 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 4 or 5, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD-generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

If 1:1 multiplexing is specified, LD* is also used to clock the Bt460 (at a maximum of 50 MHz). The rising edge of LD* still latches the P0–P8 {A}, OL0–OL3 {A}, OLE {A}, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. CLOCK must still run but is ignored.

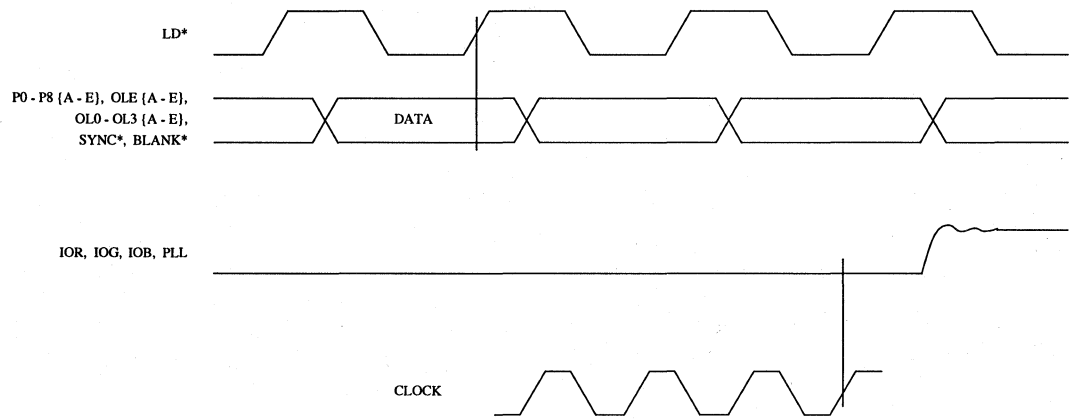


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Pixel Addressing of Color Palette RAM

Typically, the P8 pixel input port is used to select the lower (P8 = 0) or upper (P8 = 1) 256 entries in the color palette RAM.

Alternately, the Bt460 can use the cross hair cursor window to select the lower (outside the cursor window) or upper (inside the cursor window) 256 entries in the color palette RAM. In this case, the P8 pixel inputs are logically ORed with the lower/upper selection by the cursor window. Use of the P8 pixel inputs for palette selection can be disabled by the pixel read mask register (high).

Read and Blink Masking

Each clock cycle, 9 bits of color information (P0–P8) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that blinking does not cause a color change during the active display time (i.e., in the middle of the screen), the Bt460 monitors the BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register_1 specifies the number of clock cycles to pan. Only the pixel inputs and underlays are panned—overlays are not. To pan, SYNC* and BLANK* should be delayed an additional one, two, three, or four clock cycles.

If 0-pixel panning is specified, pixel {A} is output first, followed by pixel {B}, followed by pixel {C}, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats (assuming the interleave select is pixel {A}).

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, then pixel {D}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval and will not be on the display screen. At the end of the active display line, pixel {A} will be output.

Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

When a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt460 during the first LD* cycle that BLANK* is a logical zero.

In the 1:1 multiplex mode, 0-pixel panning should be specified.

The cursor position does not change relative to the edge of the display screen during panning.

5

Pixel Zoom

The Bt460 supports 1x to 16x integer zoom through the use of pixel replication. Only the P0–P8 inputs are zoomed.

If 2x zooming is specified, the {A} pixel is output for two clock cycles, followed by the {B} pixel for two clock cycles, then the {C} pixel for two clock cycles, etc. The 3x zooming is similar, except each pixel is output for three clock cycles. For 1:1 multiplexing, only the {A} pixel is output.

LD* must always be the pixel clock (1:1 multiplex mode), or one fourth or one fifth the CLOCK rate. Regardless of the zoom factor, P0–P8 data is latched every LD* cycle.

During 2x zoom, new P0–P8 data must be presented every two LD* cycles. During 3x zoom, new P0–P8 data must be presented every three LD* cycles. The pixel data must be held at the P0–P8 {A–E} inputs for the appropriate number of LD* cycles until new P0–P8 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

In the 1:1 multiplex mode, 1x zoom must be specified. Also, while in the block mode (1, 2, or 4 bits per pixel), 1x zoom must be specified.

Figure 3 illustrates the zoom timing.

Circuit Description (continued)

Cursor1, Cursor0	CR30	CR22	OLE	CR05	OL0–OL3	P0–P8	Addressed by frame buffer	Overlay Mode
11	x	x	x	x	$x	$xxx	cursor color 3	
10	x	x	x	x	$x	$xxx	cursor color 2	
01	x	x	x	x	$x	$xxx	cursor color 1	
00	0	0	x	x	$F	$xxx	overlay color 15	normal
:	:	:	:	:	:	:	:	
00	0	0	x	x	$1	$xx	overlay color 1	
00	0	0	x	1	$0	$xx	overlay color 0	
00	0	0	x	0	$0	$000	RAM location $000	
00	0	0	x	0	$0	$001	RAM location $001	
:	:	:	:	:	:	:	:	
00	0	0	x	0	$0	$1FF	RAM location $1FF	
00	x	1	1	x	$F	$xxx	overlay color 15	X Windows
:	:	:	:	:	:	:	:	
00	x	1	1	x	$1	$xxx	overlay color 1	
00	x	1	1	x	$0	$xxx	overlay color 0	
00	x	1	0	0	$x	$000	RAM location $000	
00	x	1	0	0	$x	$001	RAM location $001	
:	:	:	:	:	:	:	:	
00	x	1	0	0	$x	$1FF	RAM location $1FF	
00	1	0	x	x	$F	$xxx	overlay color 15	underlay
:	:	:	:	:	:	:	:	
00	1	0	x	x	$1	$xxx	overlay color 1	
00	1	0	1	x	$0	$000	overlay color 0 (underlay)	
00	1	0	0	0	$x	$000	RAM location $000	
00	1	0	x	0	$x	$001	RAM location $001	
:	:	:	:	:	:	:	:	
00	1	0	x	0	$x	$1FF	RAM location $1 FF	

Refer to Figure 8 for generation of Cursor1 and Cursor0 control bits.

Table 2. Palette and Overlay Select Truth Table.

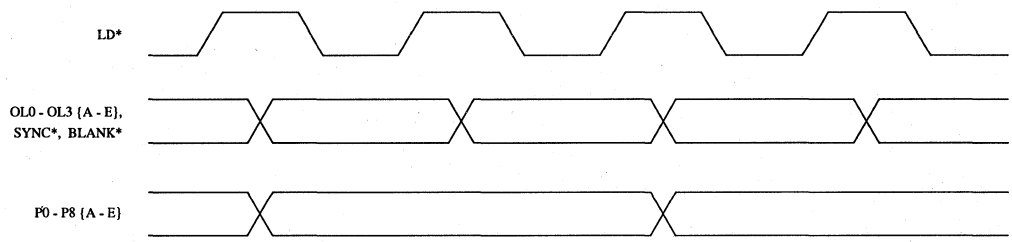


Figure 3. Zoom Input Timing (2x Zoom).

Circuit Description (continued)

Block Mode Operation

The Bt460 supports loading of the P0–P7 pixel data at 1, 2, 4, or 8 bits per pixel.

LD* must always be the pixel clock (1:1 multiplex mode), or one fourth or one fifth the CLOCK rate, regardless of the block mode. Regardless of the block mode, P0–P8 data is latched every LD* cycle.

For 8 bits per pixel (or 9 if the P8 pixel inputs are being used), new P0–P7 information must be presented every LD* cycle. For 4 (or 5) bits per pixel, new P0–P7 information must be presented every two LD* cycles. For 2 (or 3) bits per pixel, new P0–P7 information must be presented every four LD* cycles. For 1 (or 2) bits per pixel, new P0–P7 information must be presented every eight LD* cycles.

The pixel data must be held at the P0–P7 inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Tables 3 and 4 show the block mode operation and color palette RAM addressing.

Figure 4 illustrates the block mode timing (4 bits per pixel).

In the 1:1 multiplex mode, 8 bits per pixel must be specified. Also, for block modes other than 8 bits per pixel, a 0-pixel interleave must be selected.

Bits per Pixel	Pixels per LD* (1:1 muxing)	Pixels per LD* (4:1 muxing)	Pixels per LD* (5:1 muxing)	Colors Displayed
1 (2)	8	32	40	2 (4)
2 (3)	N/A	16	20	4 (8)
4 (5)	N/A	8	10	16 (32)
8 (9)	N/A	4	5	256 (512)

Numbers in parentheses indicate number of bits per pixel and number of colors if P8 pixel inputs are also used.

Table 3. P0–P7 Block Mode Operation.

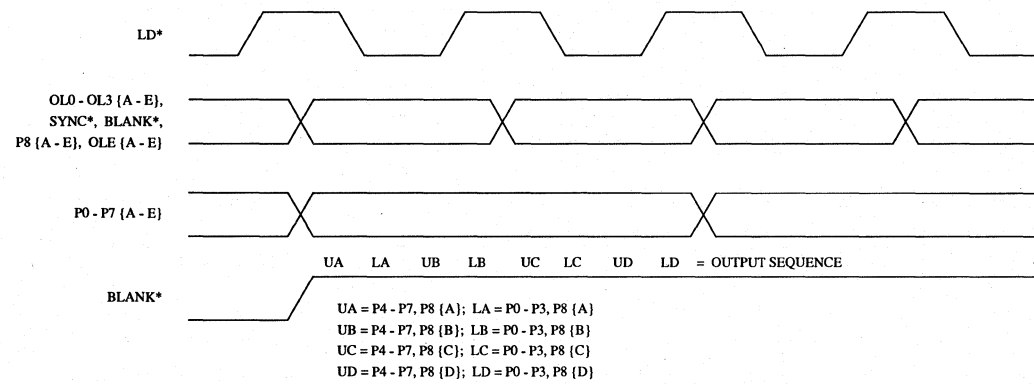


Figure 4. Block Mode Input Timing (4 Bits per Pixel, 1x Zoom, 4:1 Multiplexing).

Circuit Description (continued)

1 Bit per Pixel (RA1–RA7 = 0) RA0 =	2 Bits per Pixel (RA2–RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4–RA7 = 0) RA3–RA0 =	8 Bits per Pixel RA7–RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Note: Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0–P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode. The P8 pixel inputs are unaffected by the block mode and address the RA8 inputs of the RAM.

Table 4. Block Mode Operation (RA = Color Palette RAM Address).

On-Chip Cursor Operation

The Bt460 has an on-chip, three-color, 64 x 64 pixel, user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is done through the cursor (x,y) register. The Bt460 expects (x) to increase to the right and (y) to increase down, as shown on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 5.)

Three-Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

A (0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each plane of cursor information may also be independently enabled or disabled for display through the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM.

Circuit Description (continued)

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the thirty-first column of the 64 x 64 array (assuming the columns start with 0 for the leftmost pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the thirty-first row of the 64 x 64 array (assuming the rows start with 0 for the topmost pixel and increment to 63).

Cross Hair Cursor

Cursor positioning for the three-color cross hair cursor is also done through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than 1 pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor as follows:

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is displayed only within the cross hair window, which is specified by the window (x,y), window-width and window-height registers. Since the cursor (x,y) register must specify a point within the window boundaries, *the software must ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.*

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000, and the window- width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 6.)

5

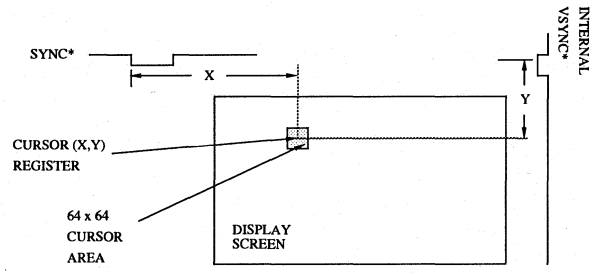


Figure 5. Cursor Positioning.

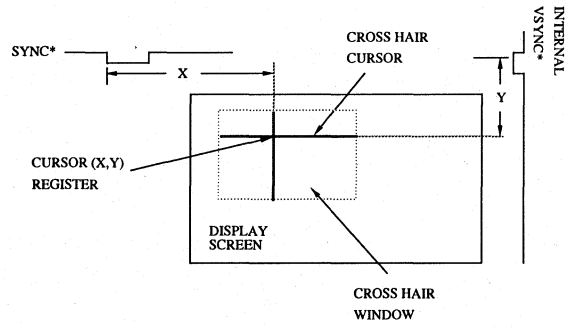


Figure 6. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical directions, it will be 1 pixel from true center about the cross hair cursor.

Figure 7 illustrates display of dual cursors.

In the 64 x 64 pixel area in which the user-definable cursor is displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair-cursor information. Thus, the color of the displayed cursor will depend on the cursor pattern, whether it is logically ORed or XORed, and the individual cursor display-enable and blink-enable bits.

Figure 8 shows the equivalent cursor generation circuitry.

X-Windows Cursor Mode

When the Bt460 is in the X-Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3.

The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Refer to Cursor RAM in the Internal Registers section for further information.

Cursor Output (CURAC)

The Bt460 optionally outputs a TTL-compatible CURAC signal. CURAC information precedes information output onto IOR, IOG, and IOB by five pixel clock cycles.

The CURAC pin may operate in one of two modes, as determined by command bit CR66. In the first mode, only cursor information is output onto CURAC. The cursor0 and cursor1 signals in Figure 8 are ORed together and output onto CURAC.

In the second mode, CURAC is also a logical one outside the cross hair window, including during blanking intervals. CURAC is a logical one inside the cross hair window while cursor information is output.

The CURDIS* input pin is used to three-state the CURAC output asynchronously to the clocks.

For a cursor positioned over an edge of the screen, CURAC (if enabled) is not driven low by a blanking condition. To avoid display noise around the cursor, it is recommended to enable and use CURAC only with a full block pattern in the cursor RAM. In addition, CURAC should be disabled during active use of the cross hair cursor.

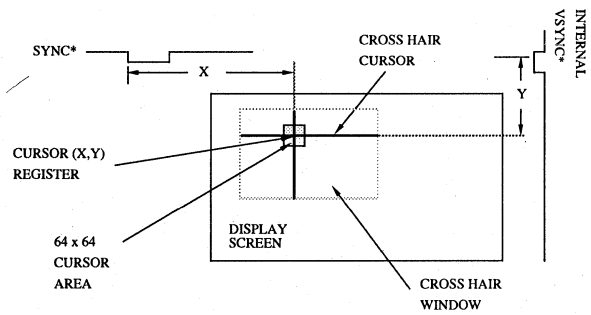


Figure 7. Dual Cursor Positioning.

Circuit Description (continued)

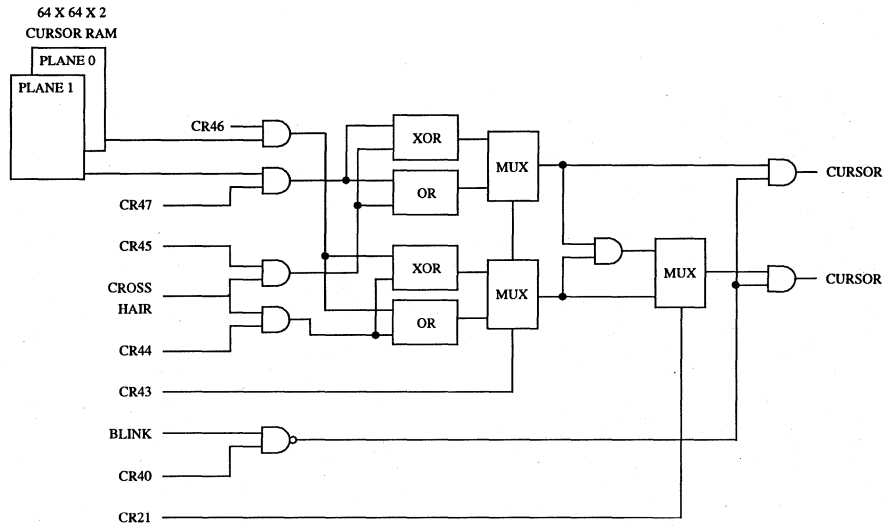


Figure 8. Cursor Control Circuitry.

Overlay / Underlay Operation

The overlay inputs (OL0–OL3 and OLE) may operate in three modes: normal overlays, X-Windows overlays, or providing underlay, as specified in Tables 2 and 5.

Overlay and underlay information may be displayed on a pixel basis. Overlays and underlay may both be used. If X-Windows overlays are used, the underlay is not available.

The priority of display operation is:

1. Cursor
2. Overlays
3. Pixel data
4. Underlays

The Bt460 must be reset to an eight-cycle pipeline delay for proper cursor pixel alignment.

In normal overlay mode, the overlay enable inputs, OLE {A–E} are ignored, and, typically, only 15 overlays are available. Graphics information (P0–P8) is displayed only when no overlay information is present (OL0–OL3 = 0000).

In the X-Windows overlay mode, the overlay enable inputs specify whether overlay information is present (OLE = 1) or not (OLE = 0). If OLE = 1, overlay information is displayed as determined by OL0–OL3. If OLE = 0, the OL0–OL3 inputs are ignored and P0–P8 pixel data is displayed.

In the underlay mode (CR30 = 1), if OLE = 0, pixel data is displayed. If OLE = 1 and P0–P8 = 0, the underlay is displayed; if P0–P8 ≠ 0, then pixel data is displayed. Overlay color 0 is used for underlay color information.

Circuit Description (continued)

	P0–P8 Pixel Inputs						
	1:1 Mux	Block Mode	Interleave	Panning	Zooming	Overlays	Underlay
Block Mode	no	-	yes	n/s	n/s	n/a	n/a
Interleave	n/s	yes	-	yes	yes	yes	yes
Panning	n/s	n/s	yes	-	yes	n/a	yes
Zooming	n/s	n/s	yes	yes	-	n/a	n/a
Overlays	yes	yes	yes	n/a	n/a	-	yes
Underlay	yes	yes	yes	yes	n/a	yes	-
Cursor	n/a	n/a	n/a	n/a	n/a	n/a	n/a

yes: fully functional together.
n/s: functions not supported together.
n/a: functions operate together, but do not affect each other.

Table 5. Features and Function Compatibility Table.

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

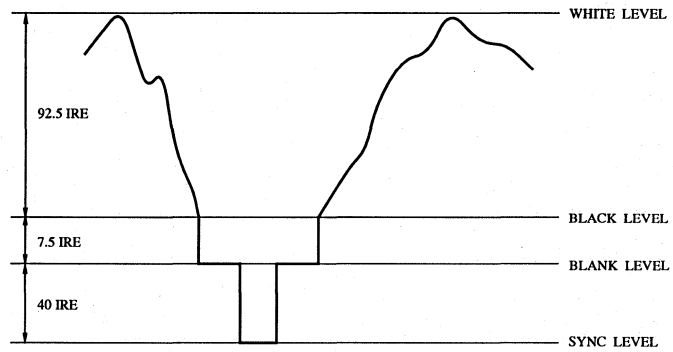
The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately-weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 9 and 10. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt460 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 9. Composite Video Output Waveform (SETUP = 7.5 IRE).

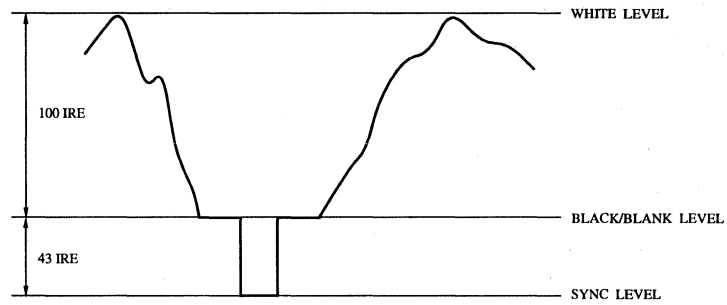
Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 10. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command register_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 5:1 multiplexing

These bits specify whether 1:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one-fifth the CLOCK rate. If 1:1 is specified, the {B}, {C}, {D}, and {E} inputs are ignored.

In the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

The pipeline delay of the Bt460 can be reset to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt460 must again be reset to a fixed pipeline delay.

CR05 Overlay 0 enable

(0) use color palette RAM
(1) use overlay color 0

When the Bt460 is in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0 (see Table 2).

CR04 reserved (logical zero)

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These 2 bits specify the blink-rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).

CR01, CR00 Block mode

(00) 8 bits per pixel
(01) 4 bits per pixel
(10) 2 bits per pixel
(11) 1 bit per pixel

These bits specify whether the P0–P7 pixel data is input as 1, 2, 4, or 8 bits per pixel. Only the P0–P7 inputs are affected.

Internal Registers (continued)

Command register_1

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR10 corresponds to data bus bit D0.

CR17 - CR15 Pan select

(000) 0 pixels {pixel A}
(001) 1 pixel {pixel B}
(010) 2 pixels {pixel C}
(011) 3 pixels {pixel D}
(100) 4 pixels {pixel E}
(101) reserved
(110) reserved
(111) reserved

These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval and should be set to 000 in the 1:1 multiplex mode. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, then {pixel C}, etc.

Only pixel and underlay information is panned. Overlay and cursor information is not panned.

In the 1:1 multiplex mode, 0 pixels should be specified.

CR14 reserved (logical zero)

CR13–CR10 Zoom factor

(0000) 1x
(0001) 2x
:
(1111) 16x

These bits specify the amount of zooming to implement. For 2x zoom, pixel {A} is output for two clock cycles, followed by pixel {B} for two clock cycles, then pixel {C}, etc. For 3x zoom, pixel {A} is output for three clock cycles, followed by pixel {B} for three clock cycles, then pixel {C}, etc.

In the 1:1 multiplex mode, only the {A} pixels are output, and 1x zoom should be selected.

Only P0–P8 are zoomed.

Internal Registers (continued)

Command register_2

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR20 corresponds to data bus bit D0.

CR27	reserved (logical zero)	
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. A 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt460 using three write cycles (red, green, and blue), and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt460 to emulate a single-channel RAMDAC using only the green channel (IOG).
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* to generate PLL information.
CR22	X Windows overlay select (0) normal overlays (1) X Windows overlays	This bit specifies whether the overlays are to operate normally (logical zero) or in an X-Window environment (logical one).
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X-Window-compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The Signature Analysis Registers (SARs) are used to hold the test result for both test methods.

Internal Registers (continued)

Command Register_3

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR60 corresponds to data bus bit D0.

CR67	reserved (logical zero)	
CR66	CURAC output format (0) cursor only (1) cursor + outside window	This bit specifies whether the CURAC output is a logical one only while cursor information is being output (logical zero) or, also, outside the cross hair cursor window (logical one).
CR65	Analysis register MSB select (0) P7 (1) P8	This bit specifies whether pixel input P7 or P8 is used as the most significant bit in the input SAR. Bits D0–D6 of the input SAR are test pixel inputs P0–P6, respectively.
CR64	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all SAR clocking. The normal mode is (0), with pixel position (A, B, C, D, or E) determined by the test register. A special mode for chip testing is (1). (In this instance, SAR operation is not guaranteed for CLOCK rates above 30 MHz.)
CR63	Red sync enable (0) disable sync on IOR (1) enable sync on IOR	This bit enables or disables generation of sync information on the IOR output.
CR62	Green sync enable (0) disable sync on IOG (1) enable sync on IOG	This bit enables or disables generation of sync information on the IOG output.
CR61	Blue sync enable (0) disable sync on IOB (1) enable sync on IOB	This bit enables or disables generation of sync information on the IOB output.
CR60	Lookup table MSB select (0) P8 (1) cursor window	This bit specifies whether to use the P8 pixel inputs or the cursor window to provide the most significant bit of the 9-bit address to the 512-entry RAM.

Internal Registers (continued)

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37–CR35 Interleave select

(000) 0 pixels
(001) 1 pixel
(010) 2 pixels
(011) 3 pixels
(100) 4 pixels
(101) reserved
(110) reserved
(111) reserved

These bits specify the order in which the pixels are to be output, as shown in Table 8. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line.

The phrase "repeats every x" in Table 8 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1-pixel interleave select, ABCD would be repeated every fourth scan line.

In the 1:1 input multiplex mode, a value of 0 pixels(000) must be specified.

CR34–CR32 First pixel select

(000) pixel {A}
(001) pixel {B}
(010) pixel {C}
(011) pixel {D}
(100) pixel {E}
(101) reserved
(110) reserved
(111) reserved

These bits are used to support panning in the Y direction with an interleaved frame buffer. Because the pixels can be interleaved, it is necessary to specify the value of the first pixel on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode.

These bits are ignored in the 1:1 multiplex mode.

CR31 Overlay interleave enable

(0) interleaving disabled
(1) interleave enabled

This bit specifies whether OL0–OL3 and OLE are to be interleaved. If interleaving is enabled, the interleave factor and first pixel selection are the same as that for P0–P8. If interleaving is disabled, pixel {A} is output first, and no interleaving occurs.

CR30 Underlay enable

(0) underlay disabled
(1) underlay enabled

If command bit CR22 is a logical zero, this bit is used to enable or disable the underlay from being displayed. If CR22 is a logical one, this bit is ignored.

If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0–P8 data is displayed. If OLE = 1, the underlay is displayed when P0–P8 = 0. If P0–P8 ≠ 0, then normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Internal Registers (continued)

Interleave Register (continued)

	5:1 multiplexing		4:1 multiplexing	
interleave select	**output sequence**	**scan line number**	**output sequence**	**scan line number**
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 8. Interleave Operation (First Pixel Select = Pixel A).

Internal Registers (continued)

Interleave Zoom Enable

If zooming while interleaving, the IZE* input pin indicates when to change the interleave sequence.

For example, while interleaving with 3x zoom, the IZE* pin should be a logical zero during the blanking interval of every third scan line (as shown in Figure 11). IZE* may be asserted coincident with the falling edge of BLANK* but must remain low at least 16 LD* cycles after the falling edge of BLANK*.

If no zooming is done (1x zoom), the IZE* should always be a logical zero or be connected directly to GND.

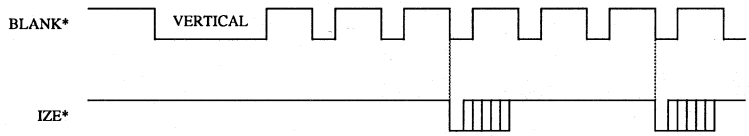


Figure 11. Interleave and Zoom Operation (3x Zoom Example).

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt460, the value read by the MPU will be $4B. Data written to this register is ignored.

Pixel Read Mask Register Low

The 8-bit pixel read mask register low is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0, and D7 corresponds to P7.

Pixel Read Mask Register High

The 8-bit pixel read mask register high is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P8, and D1–D7 are always logical zeros.

Pixel Blink Mask Register Low

The 8-bit pixel blink mask register low is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0, and D7 corresponds to P7.

Pixel Blink Mask Register High

The 8-bit pixel blink mask register high is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P8, and D1–D7 are always logical zeros.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D3 corresponds to overlay plane 3 (OL3 {A–E}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always logical zeros.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D3 corresponds to overlay plane 3 (OL3 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always logical zeros.

This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Revision Register (Revision B Only)

This 8-bit register is a read-only register, specifying the revision of the Bt459. The 4 most significant bits signify the revision letter B, in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Red, Green, and Blue Output Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. The Application Information section contains more test register information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only 1 of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Input Signature Register

Signature Operation

This 8-bit input signature register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signature is being acquired. The MPU may write to the input signature register while BLANK* is a logical zero to load the seed value. The input signature register uses P0–P7 or P0–P6 and P8 data (selected by command bit CR65) addressing the palette RAM to calculate the signatures. The 8 bits of data latched in the input signature register may be masked (forced low) by the read mask registers.

When a test display is loaded into the frame buffer, a given value for the input signature register will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the input signature register changes slightly. Rather than determining the signature, it captures and holds the 8 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the input signature register captures the 8 bits of pixel data addressing the color palette RAM. As only 1 of the (A–E) pixels can be captured each LD* cycle (or clock cycle per command bit CR64), D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

Test Register

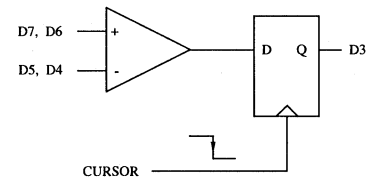
This 8-bit register is used to test the Bt460. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel; if 5:1 pixel multiplexing is specified, signature analysis is done on every fifth pixel. D0–D2 are used for 4:1 and 5:1 multiplexing to specify whether to use the A, B, C, D, or E pixel inputs, as follows:

D2 - D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should be set to 000 (pixel A).

D3–D7 are used to compare the analog RGB outputs to each other and to a 150 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	150 mV ref. select	result



D7 - D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 150 mV reference	red > 150 mV	red < 150 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 150 mV reference	green > 150 mV	green < 150 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be logical zeros.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt460. It may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is 1, 3, 5, or 7 pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	Specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window or the intersection of the cross hair cursor. The cursor (x) register is made up of the Cursor (x) Low Register (CXLR) and the Cursor (x) High Register (CXHR); the Cursor (y) Register is made up of the Cursor (y) Low Register (CYLR) and the Cursor (y) High Register (CYHR). They are not initialized and may be written to or read by the MPU at any time. For proper operation, it must be initialized by the user after power-up. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–P

where

P = 37 if 1:1 input multiplexing, 52 if 4:1 input multiplexing, 57 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used when V < 32, and the cursor must be moved off the top of the screen.

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The Window (x) Register is made up of the Window (x) Low Register (WXLR) and the Window (x) High Register (WXHR); the Window (y) Register is made up of the Window (y) Low Register (WYLR) and the Window (y) High Register (WYHR). They are not initialized and may be written to or read by the MPU at any time. For proper operation, it must be initialized by the user after power-up. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always logical zeros.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–P

where

P = 5 if 1:1 input multiplexing, 20 if 4:1 input multiplexing, 25 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of HSYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000, and the window width and height registers with $0FFF.

The cursor window may also be used to specify whether P0–P7 address the lower (outside the cursor window) or upper (inside the cursor window) 256 entries in the color palette RAM.

Internal Registers (continued)

Window-Width and -Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window-width register is made up of the Window-Width Low Register (WWLR) and the Window-Width High Register (WWHR); the window-height register is made up of the Window-Height Low Register (WHLR) and the Window-Height High Register (WHHR). They are not initialized and may be written to or read by the MPU at any time. For proper operation, it must be initialized by the user after power-up. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window-height register. Bits D4–D7 of WWHR and WHHR are always logical zeros.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window-width register, depending on whether 1:1, 4:1, or 5:1 input multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window-height register. Therefore, the minimum window width is 2, 8, or 10 pixels for 1:1, 4:1, and 5:1 multiplexing, respectively, and the minimum window height is 2 pixels.

Values from $0000 to $0FFF may be written to the window-width and -height registers.

Internal Registers (continued)

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64-pixel cursor window and is not initialized.

For Revision A, the cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention. If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the user position the cursor off-screen in the Y direction (write to the cursor (y) registers and wait for the vertical sync interval to move the cursor off-screen), write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write-then-read sequence, and if the correct cursor RAM data was not written, perform another write-then-read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

For Revision B, cursor contention has been eliminated. The cursor RAM may be written to or read by the MPU at any time without contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 12 illustrates the internal format of the cursor RAM as it appears on the display screen. Addressing starts at location $400 as specified in Table 1.

In the X-Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: In both modes of operation, plane1 = D7, D5, D3, and D1; and plane0 = D6, D4, D2, and D0.

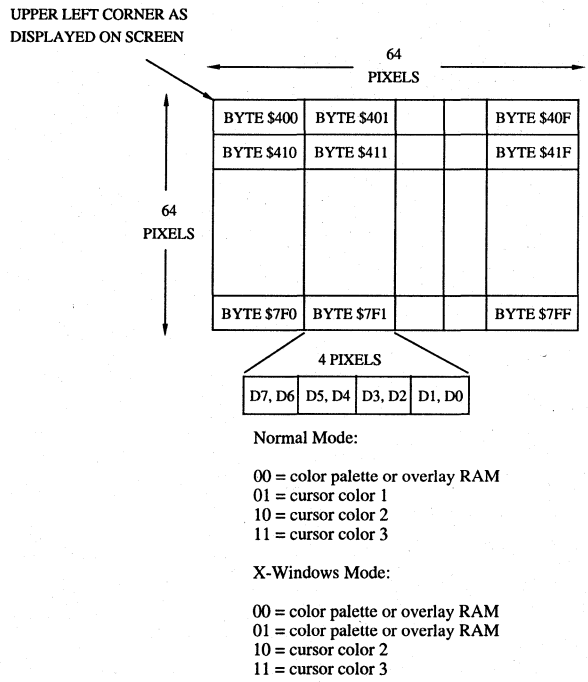


Figure 12. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 6 and 7. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as specified in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P8 {A–E}, OL0–OL3 {A–E}, OLE {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is the output clock (1:1 multiplex mode) or is one fourth or one fifth of CLOCK, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P8 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 2). One, four, or five consecutive pixels (up to 9 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then {C}, etc., until all 1, 4, or 5 pixels have been output, at which point the cycle repeats. P8 {A–E} have internal pulldown devices; if left floating, {A–E} assume logical zero states.
OL0– OL3 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as presented in Table 2. When the MPU is accessing the overlay palette RAM, the P0–P8 {A–E} inputs are ignored. Overlay information (up to 4 bits per pixel) for 1, 4, or 5 consecutive pixels is input through this port. Unused inputs should be connected to GND.
OLE {A–E}	Overlay enable inputs (TTL compatible). In the X-Windows mode for overlays, a logical one indicates overlay information is to be displayed. A logical zero indicates P0–P8 information is to be displayed. In the normal mode for overlays, these inputs are ignored. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figure 14 in the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
IZE*	Interleave zoom enable input (TTL compatible). This input should be a logical zero for a minimum of 16 LD* cycles after the falling edge of BLANK* during scan lines that require an interleave shift. If zoom-while-interleaving is not supported, this pin should be connected directly to GND.
CURAC	Cursor active output. This output is a logical one while cursor or cross hair window information is being output. It is output following the rising edge of CLOCK (see Figure 21 in the Timing Waveforms section).
CURDIS*	Cursor disable input. A logical zero three-states the CURAC output asynchronously to the clocks. A logical one enables cursor information to be output onto CURAC. CURDIS* has an internal pulldown device; if left floating, it assumes a logical zero state (see Figure 21).

Pin Descriptions (continued)

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>COMP</td><td>Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 14). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>FS ADJUST</td><td>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 14). The IRE relationships in Figures 9 and 10 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

RSET (Ω) = K1 * VREF (V) / IOG (mA)

The full-scale output current on IOR and IOB for a given RSET is:

IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)

where K1 and K2 are defined as:

<table><tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr><tr><td>7.5 IRE</td><td>K1 = 11,294</td><td>K2 = 8,067</td></tr><tr><td>0 IRE</td><td>K1 = 10,684</td><td>K2 = 7,457</td></tr></table></td></tr>
<tr><td>VREF</td><td>Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 14, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 13. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
</table>

Pin Descriptions (continued)

Pin Name	Description
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt460s to be synchronized with subpixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as shown in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L1	P8A	G14	GND	H1
SYNC*	K3	P8B	G13	GND	H2
LD*	A5	P8C	F14	GND	H3
CLOCK	K1	P8D	F13	GND	C7
CLOCK*	K2	P8E	E14	GND	G12
IZE*	B5			GND	M8
		OL0A	E1	GND	M7
P0A	E3	OL0B	F2	GND	N7
P0B	D2	OL0C	F1		
P0C	D1	OL0D	G3	COMP	N9
P0D	E2	OL0E	G2	FS ADJUST	M10
P0E	F3			VREF	P9
		OL1A	M1		
P1A	A1	OL1B	L2	CE*	P13
P1B	D3	OL1C	N1	R/W	N12
P1C	C2	OL1D	L3	C1	P12
P1D	B1	OL1E	M2	C0	M11
P1E	C1				
		OL2A	M3	D0	L13
P2A	A3	OL2B	N2	D1	M14
P2B	B3	OL2C	P1	D2	L12
P2C	A2	OL2D	P2	D3	M13
P2D	C3	OL2E	N3	D4	N14
P2E	B2			D5	P14
		OL3A	M4	D6	N13
P3A	A8	OL3B	P3	D7	M12
P3B	A7	OL3C	N4		
P3C	B7	OL3D	P4	reserved	J13
P3D	A6	OL3E	M5	reserved	J14
P3E	B6			reserved	H12
		OLEA	N5	reserved	H13
P4A	C9	OLEB	P5	reserved	H14
P4B	B9	OLEC	M6	reserved	B4
P4C	A9	OLED	N6	reserved	C4
P4D	C8	OLEE	P6	reserved	C14
P4E	B8			reserved	C13
		IOG	P10	reserved	B14
P5A	B11	IOB	P11	reserved	C12
P5B	A11	IOR	N10	reserved	B13
P5C	C10	PLL	N11	reserved	L14
P5D	B10			reserved	K12
P5E	A10	CURAC	A4	reserved	J12
		CURDIS*	C5	reserved	K14
P6A	A14			reserved	K13
P6B	A13	VAA	J1		
P6C	B12	VAA	J2		
P6D	C11	VAA	J3		
P6E	A12	VAA	C6		
		VAA	F12		
P7A	E13	VAA	M9		
P7B	E12	VAA	P7		
P7C	D14	VAA	P8		
P7D	D13	VAA	N8		
P7E	D12				

Pin Descriptions (continued)

Bt460

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	P8E	P8C	P8A	N/C	N/C	N/C	N/C	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	P8D	P8B	N/C	N/C	N/C	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	N/C	N/C	N/C	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	PLL	IOB
10	P5E	P5D	P5C									FS ADJ	IOR	IOG
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	VAA	VAA
7	P3B	P3C	GND									GND	GND	VAA
6	P3D	P3E	VAA									OLEC	OLED	OLEE
5	LD*	IZE*	CURD*									OL3E	OLEA	OLEB
4	CURAC	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

alignment marker (on top)

(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	N/C	N/C	N/C	N/C	P8A	P8C	P8E	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	N/C	N/C	N/C	P8B	P8D	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	N/C	N/C	N/C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	IOB	PLL	C0									P6D	P5A	P5B
10	IOG	IOR	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	VAA	VAA	GND									P4D	P4E	P3A
7	VAA	GND	GND									GND	P3C	P3B
6	OLEE	OLED	OLEC									VAA	P3E	P3D
5	OLEB	OLEA	OL3E									CURD*	IZE*	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	CURAC
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

PC Board Layout Considerations

PC Board Considerations

The Bt460 layout should be optimized for lowest noise on the Bt460 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt460 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 13.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 14 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt460 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths

PC Board Layout Considerations (continued)

of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt460 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt460 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 14 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

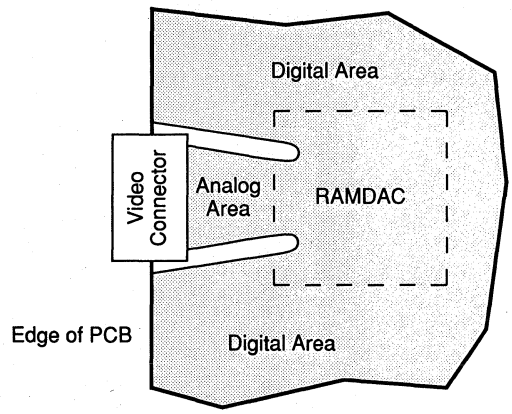
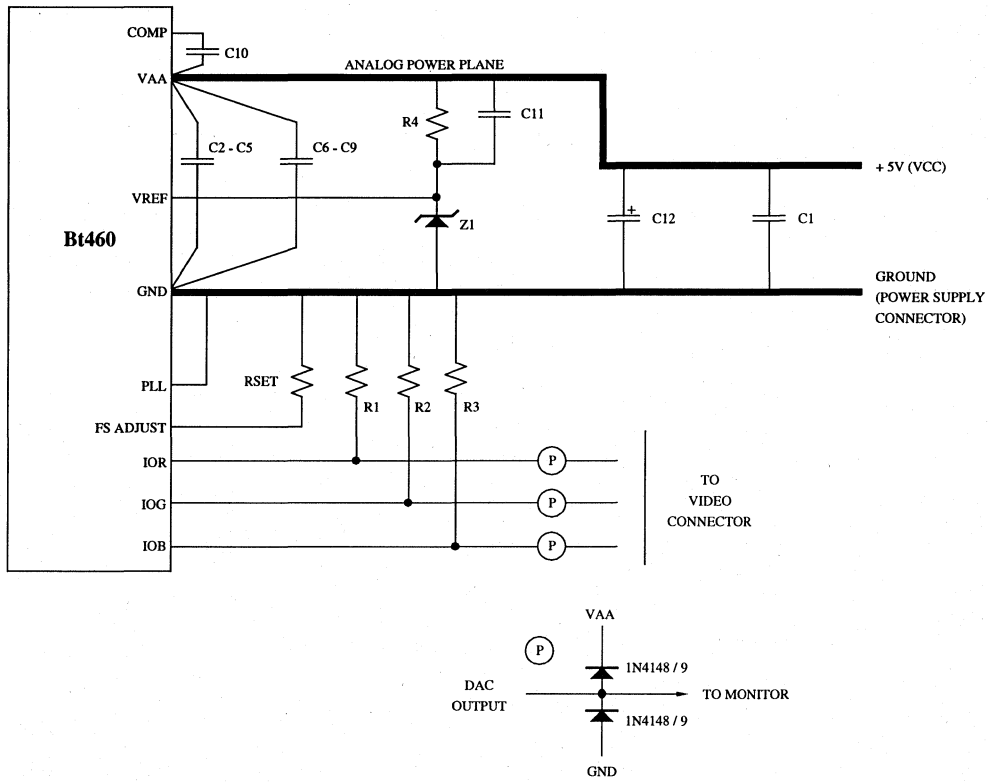


Figure 13. Sample Layout Showing Power and Ground Plane Isolation Gaps.

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt460.

Figure 14. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt460 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt460 will not function when a single-ended clock is used with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by 4 or 5 (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not consider propagation delays when deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC* and BLANK*).

When a single Bt460 is used for display, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt460 and will also set the pipeline delay of the Bt460 to eight clock cycles. The Bt438 may also be used to interface the Bt460 to a TTL clock. Figure 15 illustrates use of the Bt438 with the Bt460.

When a single Bt460 is used, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Using Multiple Bt460s

When up to four Bt460s are used for display, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt460, synchronizes them to subpixel resolution, and sets the pipeline delay of the Bt460 to eight clock cycles. The Bt439 may also be used to interface the Bt460 to a TTL clock. Figure 16 illustrates use of the Bt439 with the Bt460.

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt460, relative to CLOCK. The Bt439 compares the phase of the

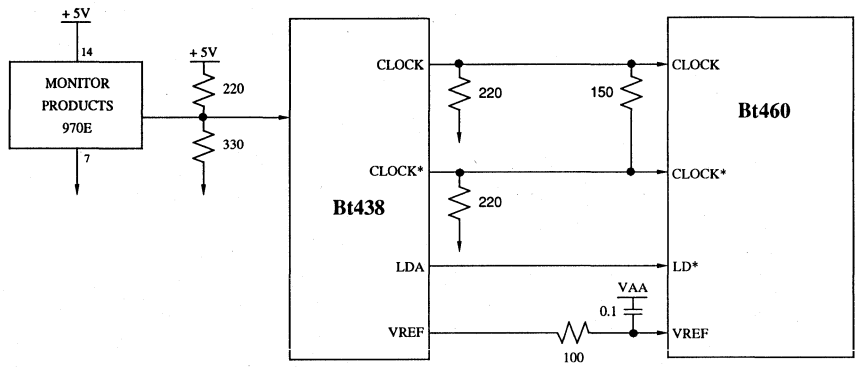


Figure 15. Generating the Bt460 Clock Signals.

Application Information (continued)

PLL signals generated by up to four Bt460s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt460s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

If subpixel synchronization of multiple Bt460s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt460s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt460s must still be isolated by 100 Ω resistors, as shown in Figure 15, and have a 0.1 µF bypass capacitor to VAA. The designer must minimize skew on the CLOCK and CLOCK* lines. The PLL outputs of the Bt460s will not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

When multiple Bt460s are used, each Bt460 should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each Bt460 has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each Bt460 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

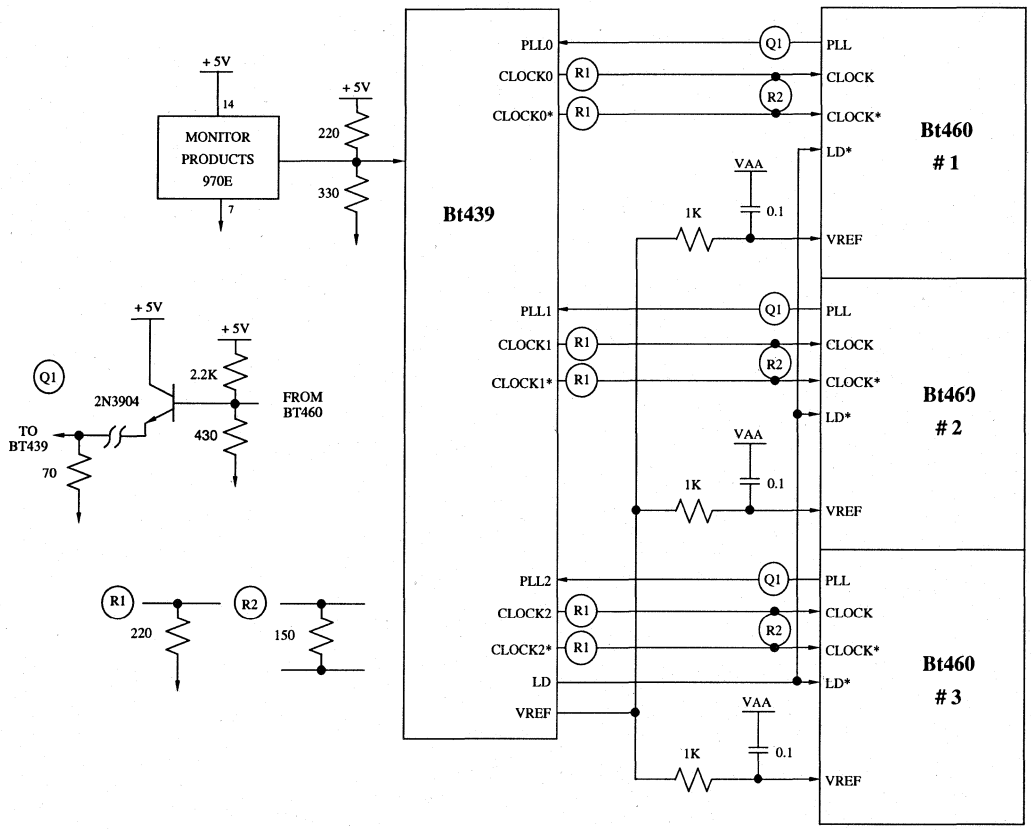


Figure 16. Generating the Clock Signals for Multiple Bt460s.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt460, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt460 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when they are used with the Bt460.

To reset the Bt460, it should be powered up, with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. The device can be held with CLOCK and CLOCK* stopped for an unlimited time.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

To ensure that the Bt460 has the proper confiuration, all the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power-up that occurs prior to initialization of the command registers cannot be used to ensure the fixed pipeline. An additional reset is required after command register writes.

The resetting of the Bt460 to an eight-clock-cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt460s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking can be software controlled by using the read mask register and overlay display enable bits.

The Bt460 must be reset to an eight-cycle pipeline delay for proper cursor pixel alignment.

Interleave Operation

To support interleaved frame buffers, the Bt460 may be configured for various interleave factors, as specified in Table 8. Table 9 is an example of interleave operation for 4:1 multiplexing, an interleave select of 3, and starting with pixel {A}. Table 10 is an example of the same operation with pixel {B} selected as the starting pixel (with the display panned down three scan lines).

Scan line number 0 corresponds to the top of the display screen and is the first displayed scan line after a vertical blanking interval. The output sequence is shown, starting at the leftmost displayed pixel.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Scan Line	Output Sequence
0	ABCDABCD...
1	DABCDABC...
2	CDABCDAB...
3	BCDABCDA...
4	ABCDABCD...
5	DABCDABC...
6	CDABCDAB...
7	BCDABCDA...
:	:

Table 9. Interleave Example.

Scan Line	Output Sequence
0	BCDABCDA...
1	ABCDABCD...
2	DABCDABC...
3	CDABCDAB...
4	BCDABCDA...
5	ABCDABCD...
6	DABCDABC...
7	CDABCDAB...
:	:

Table 10. Interleave Example.

Application Information (continued)

Test Features of the Bt460

The Bt460 contains three dedicated test registers and an analog output comparator that assist the user in evalu-ating the performance and functionality of the part. This section explains the operating use of these test features.

Signature Registers (Signature Mode)

The input signature register is 8 bits wide, capturing pixel information prior to the lookup table. Since the pixel path is 9 bits wide, the P7 or P8 pixel input, in conjunction with the P0–P6 pixel inputs, is selected for capture by command bit CR65.

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue output Signature Analysis Registers (SARs), as well as to the three on-chip DACs. The output SARs act as a 24-bit-wide linear feedback shift register on each succeeding pixel that is latched.

When the device is in either the 4:1 or 5:1 multiplexed mode, the SARs only latch 1 pixel per load group. Thus the SARs are operating on only every fourth or fifth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, or E) is latched to generate new signatures by setting bits D0–D2 in the test register.

In 1:1 mux mode, the SARs will generate signatures truly on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (test register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt460 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt460 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 8-bit or 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one line or one frame buffer of pixels, will be input to the chip. Then, at the succeeding blank state, the resultant 8-bit or 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 4:1 or 5:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, etc.—being selected.

It is not simple to specify the algorithm which specifies the linear feedback shift operations used in the Bt460. The linear feedback configurations are shown in Figures 17 and 18. Each register internally uses XORs at each input bit (D_n) with the output (result) by 1 least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can be used as the seed, for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs. Maximum frequency supported by the SARs is 135 MHz.

Signature Registers (Data-Strobe Mode)

Setting command bit CR20 to one puts the SARs into data-strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. However, each pixel value that is strobed into the SARs can be directly checked. To read values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt460. The levels of most inputs do not matter *except* that CLOCK should be high and CLOCK* should be low. Then, the user may read the pixel color by doing three successive MPU reads from the red, green, and blue output SARs, respectively. Likewise, the input SAR may be read with one MPU read.

In general, the color readout will correspond to a pixel latched on the previous load. However, because of the pipelined data path, the color may come from an earlier load cycle. To read successive pixels: LD* should be toggled, the CLOCK pins should be pulsed according to the mux state (one, four, or five periods), and all pixel-related inputs should be held and the three MPU reads performed as described. This overall process is best done on a sophisticated VLSI semiconductor tester.

Application Information (continued)

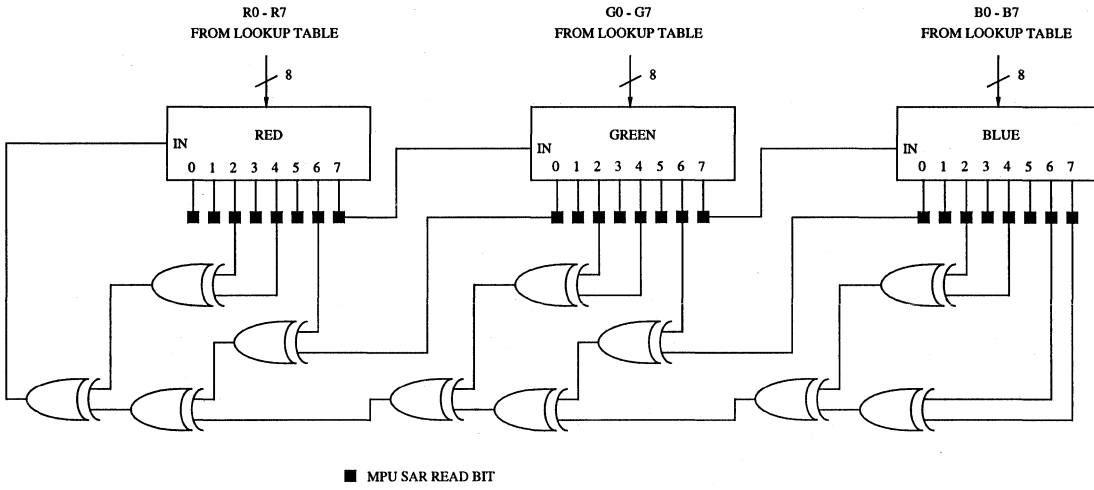


Figure 17. Output Signature Analysis Register Circuit.

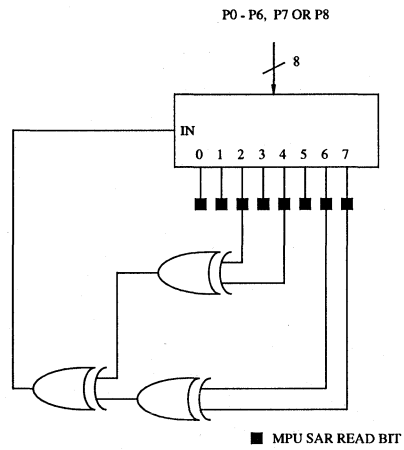


Figure 18. Input Signature Analysis Register Circuit.

Application Information (continued)

Analog Comparator

The other dedicated test structure in the Bt460 is the analog output comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected through the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register on each of the 64 scan lines of the 64 x 64 user-defined cursor block. (The 64 x 64 cursor must be enabled for display.) On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point actually occurs over the leftmost edge of the 64 x 64 cursor block.

Because of the comparator's simple design, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading test register bit D3.

Application Information (continued)

Initializing the Bt460

Following a power-on sequence, the Bt460 must be initialized. This sequence will configure the Bt460 as follows:

4:1 multiplexed operation
no overlays, no blinking, no interleave
64 x 64 block cursor, no cross hair cursor
9 bits per pixel, no panning, no zoom
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register low	10
Write $01 to pixel read mask register high	10
Write $00 to pixel blink mask register low	10
Write $00 to pixel blink mask register high	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to interleave register	10
Write $00 to test register	10
Write $0F to address register low	00
Write $14 to command register_3	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern	
Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $1FF)	11
Write green data to RAM (location $1FF)	11
Write blue data to RAM (location $1FF)	11

Overlay Color Palette Initialization	
Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization	
Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND - 0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
(except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH				
P8 {A–E}, CURDIS*				60	µA
Other Inputs				1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		4	10	pF
(f = 1 MHz, Vin = 2.4 V)					
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	0.6		6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance	CKIN		4	10	pF
(f = 1 MHz, Vin = 4.0 V)					
Digital Outputs (D0–D7, CURAC)					
Output High Voltage	VOH	2.4			V
(IOH = -400 µA)					
Output Low Voltage	VOL			0.4	V
(IOL = 3.2 mA)					
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level - Sync Enabled		6.29	7.62	8.96	mA
Blank Level - Sync Disabled		0	5	50	µA
Sync Level (If Enabled)		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance	CAOUT		13	20	pF
(f = 1 MHz, IOUT = 0 mA)					
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–1.0		+2.5	V
Output Impedance			50		kΩ
Output Capacitance			8	15	pF
(f = 1 MHz, PLL = 0 mA)					
Voltage Reference Input Current	IREF		100		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

5

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	Units
Clock Rate	Fmax	max	135	110	MHz
LD* Rate	LDmax				
1:1 multiplexing		max	50	50	MHz
4:1 multiplexing		max	33.75	27.5	MHz
5:1 multiplexing		max	27	22	MHz
R/W, C0, C1 Setup Time	1	min	0	0	ns
R/W, C0, C1 Hold Time	2	min	10	10	ns
CE* Low Time	3	min	40	40	ns
CE* High Time	4	min	20	20	ns
CE* Asserted to Data Bus Driven	5	min	10	10	ns
CE* Asserted to Data Valid	6	max	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	ns
Write Data Setup Time	8	min	15	15	ns
Write Data Hold Time	9	min	2	2	ns
Pixel and Control Setup Time	10	min	3	3	ns
Pixel and Control Hold Time	11	min	2	2	ns
Clock Cycle Time	12	min	7.4	9.09	ns
Clock Pulse Width High Time	13	min	3.2	4	ns
Clock Pulse Width Low Time	14	min	3.2	4	ns
LD* Cycle Time	15				
1:1 multiplexing		min	20	20	ns
4:1 multiplexing		min	29.63	36.36	ns
5:1 multiplexing		min	37.04	45.45	ns
LD* Pulse Width High Time	16				
1:1 multiplexing		min	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	ns
LD* Pulse Width Low Time	17				
1:1 multiplexing		min	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	ns
CURAC Output Delay	18	typ	18	18	ns
CURAC Disable Time	19	typ	tbd	tbd	ns
CURAC Enable Time	20	typ	tbd	tbd	ns

See test conditions on next page

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	Units
Analog Output Delay	21	typ	12	12	ns
Analog Output Rise/Fall Time	22	typ	1.5	1.5	ns
Analog Output Settling Time	23	max	8	8	ns
Clock and Data Feedthrough (Note 1)		typ	tbd	tbd	dB
Glitch Impulse (Note 1)		typ	50	50	pV - sec
DAC-to-DAC Crosstalk		typ	tbd	tbd	dB
Analog Output Skew		typ	0	0	ns
		max	2	2	ns
Pipeline Delay		min	6	6	Clocks
		max	10	10	Clocks
VAA Supply Current (Note 2)	IAA	typ	390	360	mA
		max	420	400	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. CURAC output load ≤ 5 pF. See timing waveforms and notes in Figures 19–21. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

5

Timing Waveforms

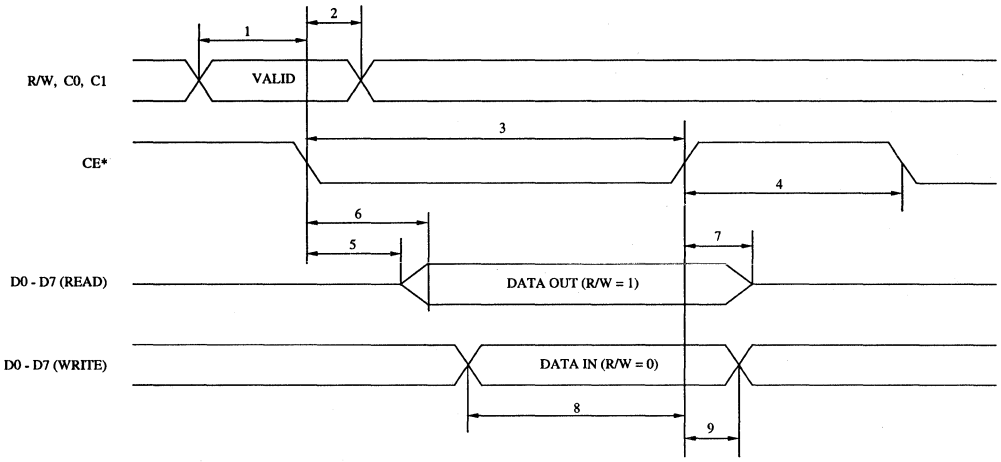
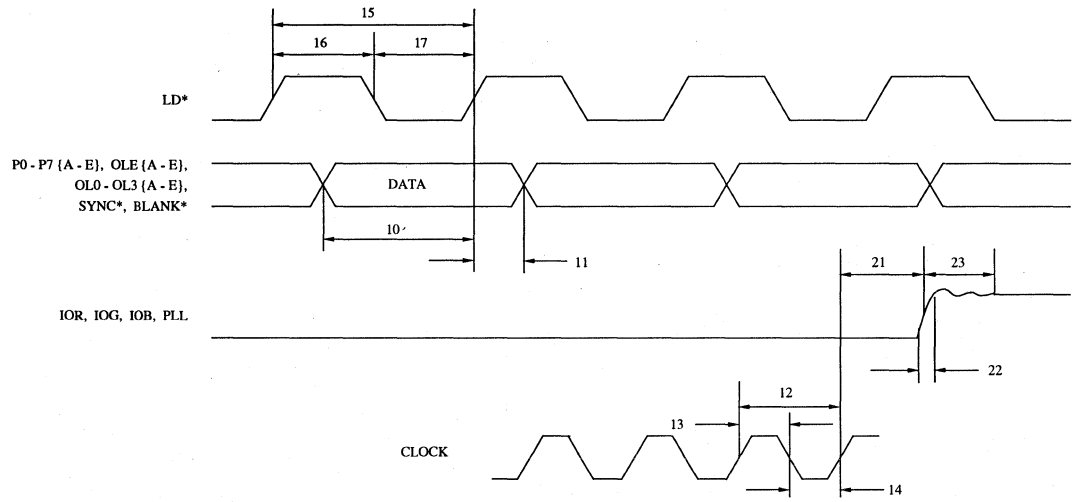


Figure 19. MPU Read/Write Timing Dimensions.



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 20. Video Input/Output Timing.

Timing Waveforms (continued)

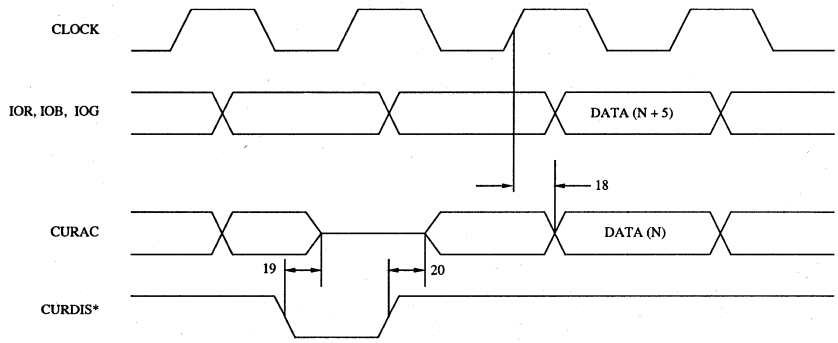


Figure 21. Cursor Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt460KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt460KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt461

Bt462

170 MHz
Monolithic CMOS
1K x 8 Color Palette
RAMDAC™

Distinguishing Features

- 170/160, 135, 110, 80 MHz Operation
- 3:1, 4:1, or 5:1 Pixel Input Muxing
- Single 8-bit D/A Converter
- 1024 x 8 Primary Color Palette RAM
- 256 x 8 Alternate Color Palette RAM
- 32 x 8 Overlay Color Palette RAM
- RS-343A-Compatible Output
- Pixel Panning Support
- Programmable Setup (0 or 7.5 IRE)
- Bit Plane Read and Blink Masks
- Two Load Color Palette Modes
- Standard MPU Interface
- 132-pin PGA or PQFP Package

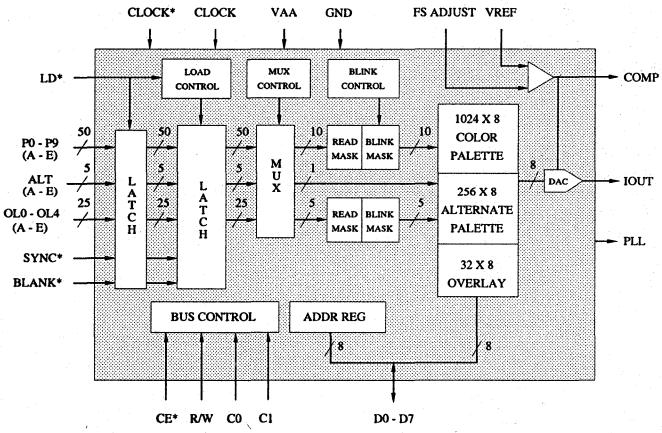
Applications

- High-Resolution Color Graphics
- True-Color Graphics Systems
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt468

Functional Block Diagram



Product Description

The Bt461/462 single-channel RAMDAC is designed specifically for high-performance, high- resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL- compatible interface (up to 45 MHz) to the frame buffer, while maintaining the 170 MHz video data rates required for sophisticated color graphics.

On-chip features include a 1024 x 8 dual-port color palette RAM; a 256 x 8 dual-port alternate color palette RAM; 32 x 8 overlay color palette RAM; programmable 3:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports; bit plane masking and blinking; programmable setup (0 or 7.5 IRE); and pixel panning support.

The Bt462 also supports an optional underlay mode. Only 15 overlays are available when the underlay is used.

Color data may be written to and read from the Bt461/462 by the MPU each cycle, or during red, green, and blue cycles. The MPU interface operates asynchronously to the pixel data, simplifying system design.

The PLL current output enables the synchronization of multiple Bt461/462s with subpixel resolution.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt461/462 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As presented in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 10-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

The two modes in which the MPU reads and writes color data to the device, as controlled by command register_0, are as follows: The first mode (normal mode), loads color data into the device each write cycle, and outputs color data from the device each read cycle. The second mode (RGB mode) loads color data into the device in red, green, and blue write cycles, and outputs data from the device using red, green, blue read cycles. The device is configured to respond only to the color cycle specified by the command register.

Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or the overlay palette RAM. The address register then increments to the next location, which the MPU may modify by writing another color. Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (8 bits each of red, green, and blue) may be read or written to three Bt461/462s in a single MPU cycle. In this application, the CE* inputs of all three Bt461/462s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, green CE* during green write cycle, and blue CE* during blue write cycle).

When accessing the primary color palette RAM, the address register resets to $0000 after a read or write cycle to location $03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each read or write cycle.

ADDR0–15	C1	C0	Addressed by MPU
$xxxx	0	0	address register low (ADDR0–7)
$xxxx	0	1	address register high (ADDR8–9)
$0000–$00FF	1	0	alternate color palette RAM
$0100	1	0	overlay color 0
:	:	:	:
$011F	1	0	overlay color 31
$0200	1	0	ID register
$0201	1	0	command register_0
$0202	1	0	command register_1
$0203	1	0	command register_2
$0204	1	0	pixel read mask register low
$0205	1	0	pixel read mask register high
$0206	1	0	pixel blink mask register low
$0207	1	0	pixel blink mask register high
$0208	1	0	overlay read mask register
$0209	1	0	overlay blink mask register
$020C	1	0	test register
$0000–$03FF	1	1	primary color palette RAM

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or overlay RAM. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt461/462 is programmed to be a red, green, or blue RAMDAC and will respond only to the assigned color read or write cycle. In this application, the Bt461/462s share a common 8-bit data bus. The CE* inputs of all three Bt461/462s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the primary color palette RAM, the address register resets to $0000 after a blue read or write cycle to location $03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits.

The other 10 bits of the address register (ADDR0–9) are accessible to the MPU.

Command register0 is used to specify whether the device loads or outputs data during the red, green, or blue cycle. This mode is useful if only an 8-bit data bus is available, and the software drivers are written for RGB operation.

CE* must be a logical zero during each of the red, green, and blue read/write cycles.

Additional Information

Although the color palette RAMs and overlay RAM are dual ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU during the write cycle, 1 or more of the pixels on the display screen can be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations. ADDR0 and ADDR8 correspond to D0. ADDR10–ADDR15 are always logical zeros.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt461/462.

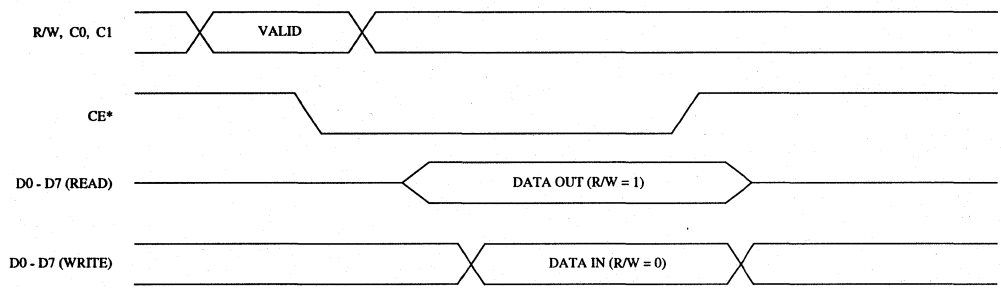

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt461/462 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information for 3, 4, or 5 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 3-, 4-, or 5-pixel resolution. Typically, the LD* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase-shifted in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 3, 4, or 5, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 3:1 multiplexing is specified, only one rising edge of LD* should occur every three clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

The 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.

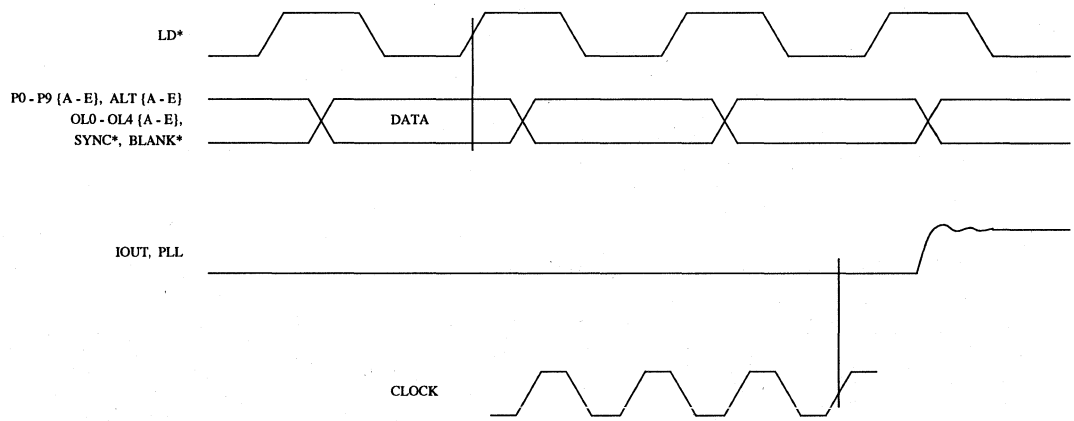

Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

Each clock cycle, 10 bits of color information (P0–P9, ALT) and 5 bits of overlay information (OL0–OL4) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that blinking does not cause a color change during the active display time (i.e., in the middle of the screen), the Bt461/462 monitors the BLANK* input to determine vertical retrace intervals, i.e., that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 illustrates the truth table used for color selection.

Alternate Color Palette RAM

The pixel read mask and blink mask registers can also be used when the pixel inputs are addressing the alternate color palette RAM.

If the ALT enable bit in command register_0 is a logical one, the alternate color palette RAM may be accessed on a pixel basis. A logical one on an ALT {A–E} input forces the P0–P7 {A–E} inputs to address the alternate color palette RAM. P8 and P9 {A–E} are ignored in this instance. If the ALT enable bit in command register_0 is a logical zero, the ALT {A–E} inputs are ignored, as specified in Tables 2 and 3.

The primary color palette RAM may be pixel bypassed with the ALT inputs. In this instance, the alternate color palette RAM should be loaded either so that each byte contains its corresponding address ($00–$FF) or with a gamma correction factor. The ALT inputs would then specify, on a pixel basis, whether to bypass the primary color palette RAM.

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CR04	ALT	CR05	OL0 - OL4	P0 - P9	Addressed by frame buffer
x	x	x	$1F	$xxx	overlay color 31
:	:	:	:	:	:
x	x	x	$01	$xxx	overlay color 1
x	x	1	$00	$xxx	overlay color 0
0	x	0	$00	$000	primary RAM location $000
0	x	x	$00	$001	primary RAM location $001
:	:	:	:	:	:
0	x	x	$00	$3FF	primary RAM location $3FF
x	0	0	$00	$000	primary RAM location $000
x	0	x	$00	$001	primary RAM location $001
:	:	:	:	:	:
x	0	x	$00	$3FF	primary RAM location $3FF
1	1	0	$00	$x00	alternate RAM location $00
:	:	x	:	$x01	alternate RAM location $01
:	:	:	:	:	:
1	1	x	$00	$xFF	alternate RAM location $FF

Table 2. Bt461—Palette and Overlay Select Truth Table.

Circuit Description (continued)

CR22	CR04	ALT	CR05	OL4	OL0–OL3	P0–P9	Addressed by Frame Buffer
x	x	x	x	1	1111	$xxx	overlay color 31
:	:	:	:	:	:	:	:
:	:	:	:	1	0000	:	overlay color 16
:	:	:	:	0	1111	:	overlay color 15
:	:	:	x	:	:	:	:
x	x	x	1	0	0000	$xxx	overlay color 0
0	0	x	0	0	0000	$000	primary RAM location $000
x	:	:	x	:	:	$001	primary RAM location $001
:	:	:	:	:	:	:	:
x	0	x	x	0	0000	$3FF	primary RAM location $3FF
0	x	0	0	0	0000	$000	primary RAM location $000
x	:	:	x	:	:	$001	primary RAM location $001
:	:	:	:	:	:	:	:
x	x	0	x	0	0000	$3FF	primary RAM location $3FF
x	1	1	x	0	0000	$x00	alternate RAM location $00
:	:	:	:	:	:	:	:
x	1	1	x	0	0000	$xFF	alternate RAM location $FF
1	x	x	x	0	1111	$xxx	overlay color 15
:	:	:	:	:	:	:	:
:	:	:	x	0	0001	$xxx	overlay color 1
1	x	x	0	1	0000	$000	overlay color 0 (underlay)

Table 3. Bt462—Palette and Overlay Select Truth Table.

Circuit Description (continued)

Pixel Panning

To support pixel panning, command register_1 specifies by what number of clock cycles to pan.

If 0-pixel panning is specified, pixel (A} is output first, followed by pixel {B}, then pixel {C}, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel (B} will be first, followed by pixel {C}, then pixel {D}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval and will not be on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval and will not be on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

When a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt461/462 during the first LD* cycle that BLANK* is a logical zero.

The pixel, overlay, and ALT inputs are all panned.

Underlay Operation (Bt462 Only)

An underlay plane can be obtained by converting overlay plane 4 (OL4) to underlay operation (command register bit CR22). In this mode of operation, only 15 overlays (OL0–OL3) are available, as specified in Table 3.

During underlay operation, the corresponding overlay plane 4 (OL4) overlay read mask register bit must be a logical zero for proper operation.

Underlays may be displayed on a pixel basis. Both overlays and the underlay may be used simultaneously. The priority of the display information is:

1. Overlays (OL0–OL3)
2. Pixel data (P0–P9)
3. Underlay (OL4)

Video Generation

Every clock cycle the selected 8 bits of color information are presented to the 8-bit D/A converter.

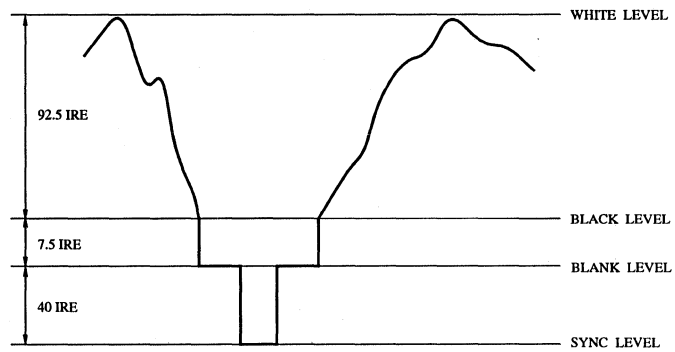
The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Command register2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converter produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converter on the Bt461/462 uses a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)

CR27 = 0		CR27 = 1	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveform (SETUP = 7.5 IRE).

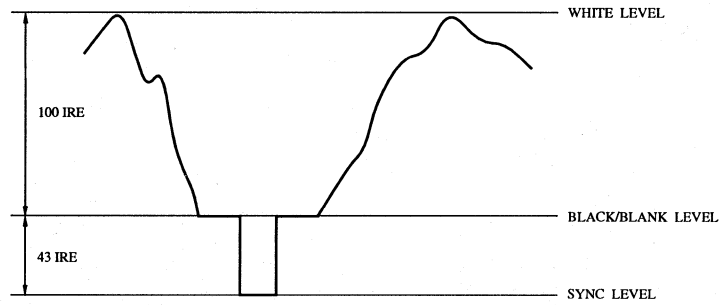
Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 523 Ω and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

CR27 = 0		CR27 = 1	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) 3:1 multiplexing
(01) 4:1 multiplexing
(10) reserved
(11) 5:1 multiplexing

These bits specify whether 3:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 3:1 is specified, the {D} and {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one third the CLOCK rate. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth the CLOCK rate.

The pipeline delay of the Bt461/462 can be reset to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt461/462 must again be reset to a fixed pipeline delay.

The 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.

CR05 Overlay 0 enable

(0) use color palette RAMs
(1) use overlay color 0

When the overlay bits are $00, this bit specifies whether to use the color palette RAMs or overlay color 0 to provide color information.

CR04 ALT enable

(0) disable alternate palette
(1) enable alternate palette

This bit specifies whether the alternate color palette RAM is enabled (logical one) or disabled (logical zero) from being addressed by the ALT {A–E} and P0–P7 {A–E} inputs.

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).

CR01 reserved (logical zero)

CR00 reserved (logical zero)

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR10 corresponds to data bus bit D0.

CR17–CR15 Pan select

(000)	0 pixels	{pixel A}
(001)	1 pixel	{pixel B}
(010)	2 pixels	{pixel C)
(011)	reserved	
(100)	3 pixels	{pixel D}
(101)	4 pixels	{pixel E}
(110)	reserved	
(111)	reserved	

These bits specify the number of pixels to be panned. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, {pixel C} indicates pixel C will be output first, etc. These bits are typically modified only during the vertical retrace interval.

The pixel, overlay, and ALT inputs are all panned.

CR14–CR10 reserved (logical zero)

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the video waveform (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video waveform. A 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt461/462 each write cycle, and color data is output each read cycle. If (01), (10), or (11) is specified, the Bt461/462 expects color data to be input and output using (red, green, and blue) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses the SYNC* or BLANK* input to generate PLL information.
CR22	Bt461—reserved (logical zero) Bt462—Underlay enable (0) overlay plane 4 (1) underlay plane 0	This bit is always a logical zero on the Bt461. On the Bt462, this bit specifies whether overlay plane 4 (OL4) should be converted to an underlay plane (logical one) or used as a normal overlay plane (logical 0).
CR21	reserved (logical zero)	
CR20	Test enable (0) disable test register (1) enable test register	A logical one enables the P9 {A–E} inputs to serve as a trigger for the test register. A logical zero enables normal operation.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt461/462, the value read by the MPU will be $4D for the Bt461 and $4C for the Bt462. Data written to this register is ignored.

Pixel Read Mask Register

The 16-bit pixel read mask register is configured as two 8-bit registers (pixel read mask low and pixel read mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM.

pixel read mask register high								pixel read mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Pixel Blink Mask Register

The 16-bit pixel blink mask register is configured as two 8-bit registers (pixel blink mask low and pixel blink mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0.

pixel blink mask register high								pixel blink mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

In order for a bit plane to blink, the corresponding bit in the pixel read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after powerup.

Internal Registers (continued)

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D4 corresponds to overlay plane 4 (OL4 {A–E}). Each register bit is logically ANDed with the corresponding overlay plane input. Bits D5–D7 are logical zeros. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

On the Bt462, the overlay read mask register for overlay plane 4 (OL4) must be a logical zero when in the underlay mode.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D4 corresponds to overlay plane 4 (OL4 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. Bits D5–D7 are logical zeros. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Test Register

The test register enables the MPU to verify that the pixel and overlay ports are addressing the color palette RAM and overlay registers correctly at full speed.

P9 (A–E} is the fast port trigger when CR20 is a logical one. P0–P8 {A–E}, ALT {A–E}, and OL0–OL4 {A–E} address the primary color palette RAM, alternate palette RAM, and overlay registers. A logical one on P9A latches the {A} color data into the test register as it is passed from the color palette to the D/A converter. A logical one on P9B latches the {B} color data into the test register as it is passed from the color palette to the D/A converter, a logical one on P9C latches the {C} color, etc.

To test the entire color palette, bit D1 in the pixel read mask register high (P9) must be a logical zero to test the lower 512 entries. Next, bit D1 in the pixel read mask register high (P9) must be a logical one to test the higher 512 entries. There should be only a single one on the P9 inputs per test read cycle.

A recommended test read cycle is four LD* cycles long. The test register may be written whenever the test mode is disabled or while in the test mode when no ones are present on the P9 inputs. The test registers are not initialized.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 4 and 5. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input typically switches off a 40 IRE current source on the IOUT output (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P9 {A–E}, OL0–OL4 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is one third, one fourth, or one fifth the CLOCK rate, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P9 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the primary or alternate color palette RAMs is to be used to provide color information (see Table 2). Through this port, 3, 4, or 5 consecutive pixels (up to 10 bits per pixel) are input. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.
OL0– OL4 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*. In conjunction with CR05 in command register_0, they specify which palette is to be used for color information, as presented in Table 2. When accessing the overlay palette RAM, the P0–P9 {A–E} and ALT {A–E} inputs are ignored. Overlay information bits (up to 5 bits per pixel) for 3, 4, or 5 consecutive pixels are input through this port. Unused inputs should be connected to GND.
ALT {A–E}	Palette select inputs (TTL compatible). These inputs are latched on the rising edge of LD*. They specify which color palette RAM is to be used for color information, as presented in Table 2. When accessing the alternate color palette RAM, the P8–P9 {A–E} inputs are ignored. Unused inputs should be connected to GND.
IOUT	Analog current output. This high-impedance current source can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 6 in the PC Board Layout Considerations section).
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt461/462s to be synchronized with subpixel resolution when used with an external PLL. A logical one on the SYNC* or BLANK* input (as specified by CR23 in command register_2) results in no output of current onto this pin, while a logical zero results in the following current output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).

5

Pin Descriptions (continued)

Pin Name	Description
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 6). When the capacitor is connected to VAA rather than to GND, the highest possible power supply noise rejection is provided. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and to maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *The PC Board Layout Considerations section contains critical layout critria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 6). The IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOUT for a 7.5 IRE blanking pedestal is: RSET (Ω) = 11,294 * VREF (V) / IOUT (mA) The relationship between RSET and the full-scale output current on IOUT for a 0 IRE blanking pedestal is: RSET (Ω) = 10,684 * VREF (V) / IOUT (mA)
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 5, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 6. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be logical zeros. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE* (see Figure 1).
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as presented in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)—132-pin PGA Package

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L1	P8A	G14	VAA	J1
SYNC*	K3	P8B	G13	VAA	J2
LD*	A5	P8C	F14	VAA	J3
CLOCK	K1	P8D	F13	VAA	C6
CLOCK*	K2	P8E	E14	VAA	F12
				VAA	M9
P0A	E3	P9A	J13		
P0B	D2	P9B	J14	GND	H1
P0C	D1	P9C	H12	GND	H2
P0D	E2	P9D	H13	GND	H3
P0E	F3	P9E	H14	GND	C7
				GND	G12
P1A	A1	ALTA	L14	GND	M8
P1B	D3	ALTB	K12		
P1C	C2	ALTC	K13	COMP	N9
P1D	B1	ALTD	K14	FS ADJUST	M10
P1E	C1	ALTE	J12	VREF	P9
P2A	A3	OL0A	E1	CE*	P13
P2B	B3	OL0B	F2	R/W	N12
P2C	A2	OL0C	F1	C1	P12
P2D	C3	OL0D	G3	C0	M11
P2E	B2	OL0E	G2		
				D0	L13
P3A	A8	OL1A	M1	D1	M14
P3B	A7	OL1B	L2	D2	L12
P3C	B7	OL1C	N1	D3	M13
P3D	A6	OL1D	L3	D4	N14
P3E	B6	OL1E	M2	D5	P14
				D6	N13
P4A	C9	OL2A	M3	D7	M12
P4B	B9	OL2B	N2		
P4C	A9	OL2C	P1	reserved	G1
P4D	C8	OL2D	P2	reserved	N11
P4E	B8	OL2E	N3	reserved	M7
				reserved	N7
P5A	B11	OL3A	M4	reserved	P7
P5B	A11	OL3B	P3	reserved	P8
P5C	C10	OL3C	N4	reserved	N8
P5D	B10	OL3D	P4		
P5E	A10	OL3E	M5	reserved	B5
				reserved	C5
P6A	A14	OL4A	N5	reserved	A4
P6B	A13	OL4B	P5	reserved	B4
P6C	B12	OL4C	M6	reserved	C4
P6D	C11	OL4D	N6		
P6E	A12	OL4E	P6	reserved	C14
				reserved	C13
P7A	E13	IOUT	P10	reserved	B14
P7B	E12	reserved	P11	reserved	C12
P7C	D14	PLL	N10	reserved	B13
P7D	D13				
P7E	D12				

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Pin Descriptions (continued)—132-pin PGA Package

Bt461/462

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	P8E	P8C	P8A	P9E	P9B	ALTD	ALTA	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	P8D	P8B	P9D	P9A	ALTC	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	P9C	ALTE	ALTB	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	N/C	N/C
10	P5E	P5D	P5C									FS ADJ	PLL	IOUT
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	N/C	N/C
7	P3B	P3C	GND									N/C	N/C	N/C
6	P3D	P3E	VAA									OL4C	OL4D	OL4E
5	LD*	N/C	N/C									OL3E	OL4A	OL4B
4	N/C	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

alignment marker (on top)

(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	ALTA	ALTD	P9B	P9E	P8A	P8C	P8E	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	ALTC	P9A	P9D	P8B	P8D	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	ALTB	ALTE	P9C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	N/C	N/C	C0									P6D	P5A	P5B
10	IOUT	PLL	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	N/C	N/C	GND									P4D	P4E	P3A
7	N/C	N/C	N/C									GND	P3C	P3B
6	OL4E	OL4D	OL4C									VAA	P3E	P3D
5	OL4B	OL4A	OL3E									N/C	N/C	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	N/C
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

Pin Descriptions (continued)—132-pin PQFP Package (Bt462 Only)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	OL0E	44	P6E	88	reserved
2	OL0D	45	P6D	89	reserved
3	OL0C	46	P6C		
4	OL0B	47	P6B	90	FS ADJUST
5	OL0A	48	P6A	91	PLL
				92	IOUT
6	P0E	49	reserved	93	VAA
7	P0D	50	reserved	94	VAA
8	P0C	51	reserved	95	COMP
9	P0B			96	VREF
10	P0A	52	P7E	97	GND
		53	P7D	98	reserved
11	P1E	54	P7C	99	reserved
12	P1D	55	P7B	100	GND
13	P1C	56	P7A	101	reserved
14	P1B				
15	P1A	57	P8E	102	OL4E
		58	VAA	103	OL4D
16	P2E	59	VAA	104	OL4C
17	P2D	60	P8D	105	OL4B
18	P2C	61	P8C	106	OL4A
19	P2B	62	GND		
20	P2A	63	GND	107	OL3E
		64	P8B	108	OL3D
21	reserved	65	P8A	109	OL3C
22	reserved			110	OL3B
23	reserved	66	P9E	111	OL3A
24	reserved	67	P9D		
25	reserved	68	P9C	112	OL2E
		69	P9B	113	OL2D
26	LD*	70	P9A	114	OL2C
27	VAA			115	OL2B
		71	ALTE	116	OL2A
28	P3E	72	ALTD		
29	P3D	73	ALTC	117	OL1E
30	GND	74	ALTB	118	OL1D
31	P3C	75	ALTA	119	OL1C
32	P3B			120	OL1B
33	P3A	76	D0	121	OL1A
		77	D1		
34	P4E	78	D2	122	SYNC*
35	P4D	79	D3	123	BLANK*
36	P4C	80	D4	124	CLOCK*
37	P4B	81	D5	125	CLOCK
38	P4A	82	D6		
		83	D7	126	VAA
39	P5E			127	VAA
40	P5D	84	CE*	128	GND
41	P5C	85	R/W	129	GND
42	P5B	86	C1		
43	P5A	87	C0	130	reserved
				131	reserved
				132	reserved

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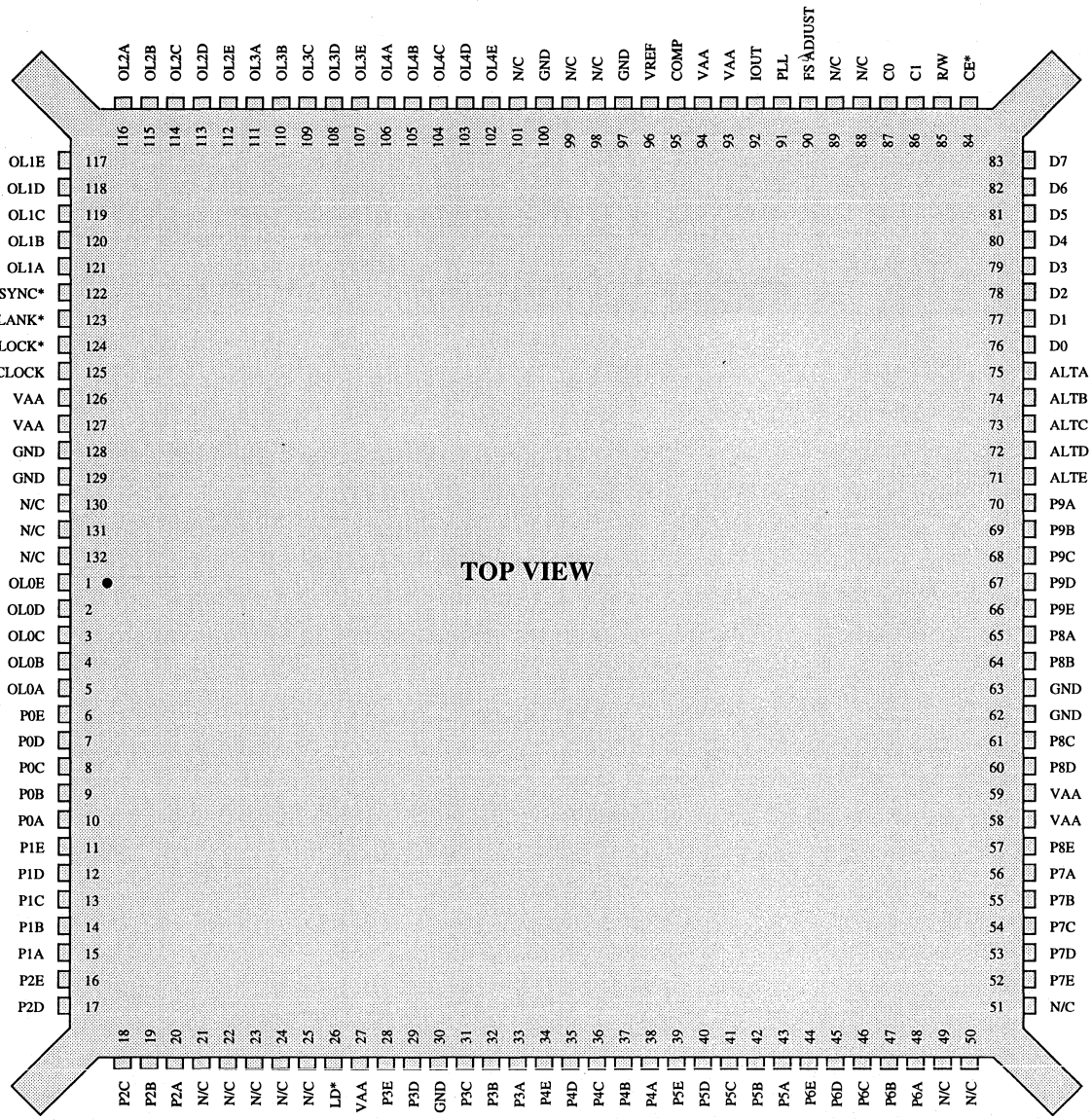
Pin Descriptions (continued)—132-pin PQFP Package (Bt462 Only)



PC Board Layout Considerations

PC Board Considerations

The Bt461 and Bt462 layout should be optimized for lowest noise on their power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt461 and Bt462 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 5.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 10 µF capacitor shown in Figure 6 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt461 and Bt462 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ring-

PC Board Layout Considerations (continued)

ing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt461 and Bt462 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt461 and Bt462 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

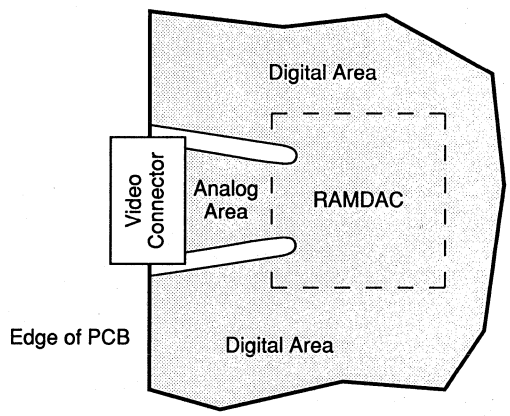
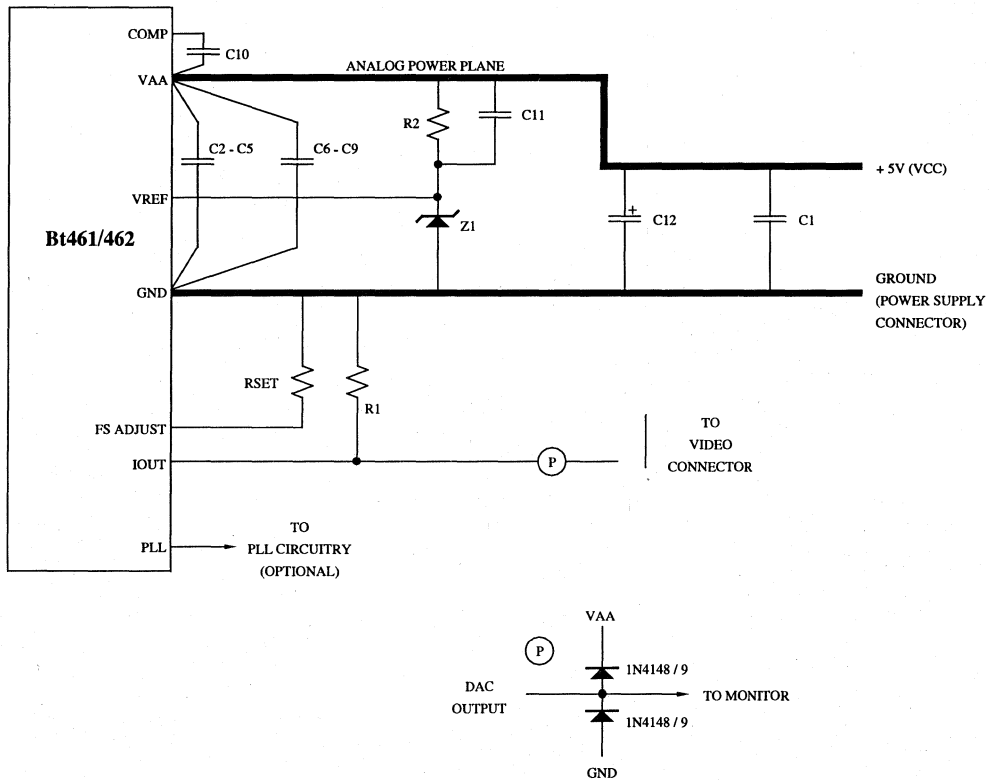


Figure 5. Sample Layout Showing Power and Ground Plane Isolation Gaps.

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt461/462.

Figure 6. Typical Connection Diagram and Parts List.

Application Information

Nonvideo Applications

The Bt461/462 may be used in nonvideo applications by disabling the video-specific control signals. Bits CR26 and CR27 in command register_2 should be set to a zero (disabling the BLANK* and SYNC* inputs). SYNC* should be a logical zero, and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}457 * VREF\ (V) / Iout\ (mA)$$

Using Multiple Devices

When multiple Bt461/462s are used, each Bt461/462 should have its own power plane ferrite bead. In addition, although a single voltage reference may drive multiple devices, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each Bt461/462 has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each Bt461/462 must have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Because of differences in pipelining and analog output delay, it is recommended that Bt461s not be mixed with Bt462s.

Clock Interfacing

Because of the high clock rates at which the Bt461 and Bt462 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 7.)

Applications of 160 MHz require robust ECL clock signals with strong pulldown (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt461/462 will not function if it uses a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by 3, 4, or 5 (depending on whether 3:1, 4:1, or 5:1 multiplexing was specified) and translating the result to TTL levels. As LD* may be phase shifted relative to CLOCK, propagation delays need not be considered when the LD* signal is derived. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC* and BLANK*).

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt461, although fixed after a power-up condition, may be anywhere from 6 to 10 clock cycles. The pipeline delay of the Bt462, although fixed after a power-up condition, may be anywhere from 8 to 12 clock cycles. The Bt461/462 contains additional circuitry enabling the pipeline delay to be fixed (8 clock cycles for the Bt461 and 10 clock cycles for the Bt462). The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt461/462.

To reset the Bt461/462, it should be powered up with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. The device can be held with CLOCK and CLOCK* stopped for an unlimited time.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

When the Bt461/462 is reset to a fixed pipeline delay, the blink counter circuitry is also reset. If the Bt461/462 is periodically reset (for example, at every vertical sync interval), the on-chip blink counter will not function correctly. In this instance, the blink mask register should be $00, and the overlay blink enable bits should be logical zeros. Software may control blinking through the read mask register and overlay display enable bits.

In standard operation, the Bt461/462 must be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

Monochrome Display Applications

For monochrome display applications where a single Bt461/462 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461/462, and sets the pipeline delay of the Bt461/462 to 8 (Bt461) or 10 (Bt462) clock cycles. The Bt438 may also be used to interface the Bt461/462 to a TTL clock. Figure 7 illustrates use of the Bt438 with the Bt461/462.

When a single Bt461/462 is used, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

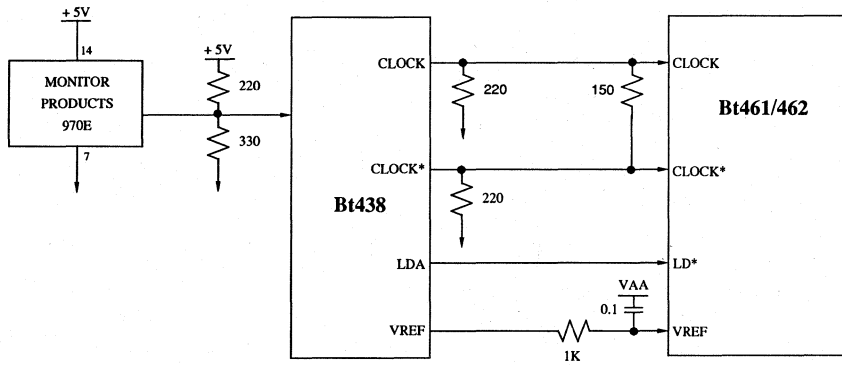


Figure 7. Generating the Bt461/462 Clock Signals (Monochrome Application).

Application Information (continued)

Color Display Applications

For color display applications where up to four Bt461/462s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461/462, synchronizes the Bt461/462s to subpixel resolution, and sets the pipeline delay of the Bt461 to 8 clock cycles and the Bt462 to 10 clock cycles. The Bt439 may also be used to interface the Bt461/462 to a TTL clock. Figure 8 illustrates use of the Bt439 with the Bt461/462.

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt461/462, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt461/462s. The Bt439 then adjusts the phase of the CLOCK and CLOCK* signals to each Bt461/462 to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

If subpixel synchronization of multiple Bt461/462s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt461/462s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). Skew must be minimized on the CLOCK and CLOCK* lines. The PLL outputs are not used and should be connected to GND (either directly or through a resistor up to 150 Ω).

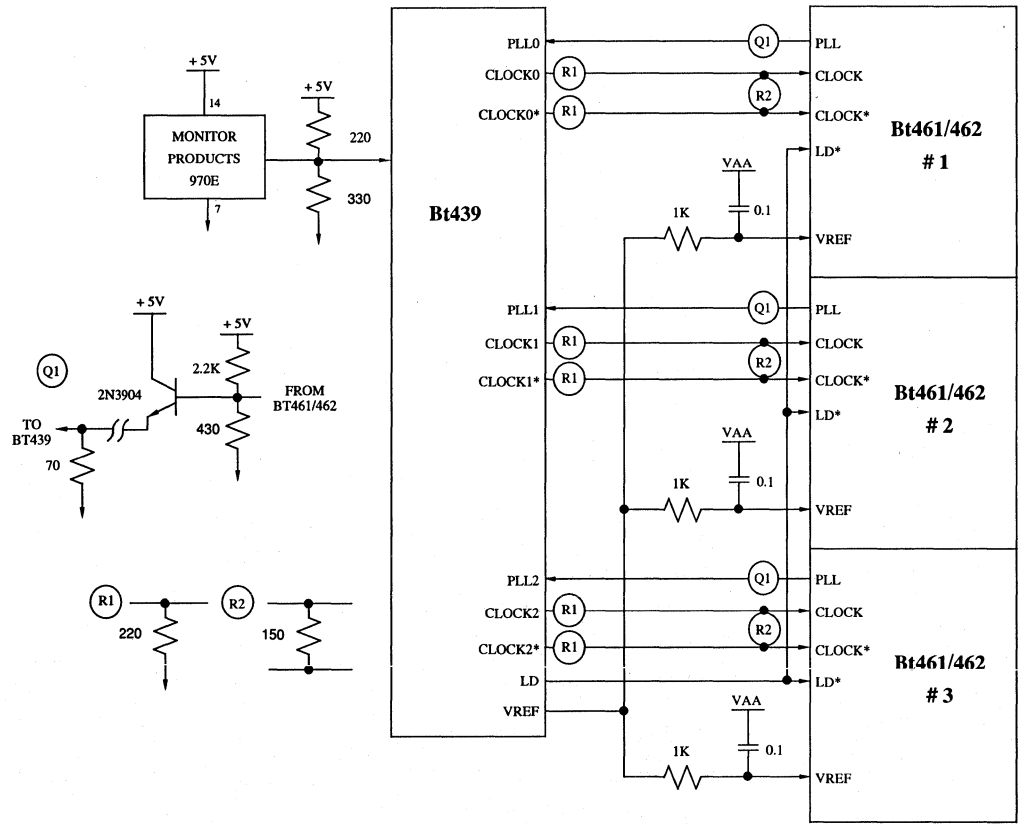


Figure 8. Generating the Bt461/462 Clock Signals (Color Application).

Application Information (continued)

Initializing the Bt461/462 (Monochrome)

Following a power-on sequence, the Bt461/462 must be initialized. This sequence will configure the Bt461/462 as follows:

4:1 multiplexed operation
no overlays
no pixel masking, no blinking, no panning
color data written/read every cycle
sync enabled on IOUT, 7.5 IRE blanking pedestal

Control Register Initialization	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $C0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Color Palette RAM Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write data to RAM (location $000)	11
Write data to RAM (location $001)	11
:	:
Write data to RAM (location $3FF)	11

Overlay Color Palette Initialization	
Write $00 to address register low	00
Write $01 to address register high	01
Write data to overlay (location $00)	10
Write data to overlay (location $01)	10
:	:
Write data to overlay (location $1F)	10

Alternate Color Palette Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write data to alternate (location $00)	10
Write data to alternate (location $01)	10
:	:
Write data to alternate (location $FF)	10

5

Application Information (continued)

Initializing the Bt461/462 (Color) 8-bit MPU Data Bus

In this example, three Bt461/462s are being used in parallel to generate true color. An 8-bit MPU data bus is available to access the Bt461/462s.

While accessing the command, read mask, blink mask, control/test, and address register, the MPU must access each Bt461/462 individually. While the MPU is accessing the color palette RAM, alternate RAM, or overlay registers, all three Bt461/462s may be accessed simultaneously.

Following a power-on sequence, the Bt461/462s must be initialized. This sequence will configure the Bt461/462s as follows:

4:1 multiplexed operation
no overlays
no blinking, no panning
initialize each one as a red, green, or blue device
sync on all outputs, 7.5 IRE blanking pedestal

Control Register Initialization

Red Bt461/462	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $D0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Green Bt461/462	
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $E0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Blue Bt461/462	
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $F0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Application Information (continued)

Color Palette RAM Initialization

Write $00 to all three address low registers	00
Write $00 to all three address high registers	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $3FF)	11
Write green data to RAM (location $3FF)	11
Write blue data to RAM (location $3FF)	11

Alternate Color Palette Initialization

Write $00 to all three address low registers	00
Write $00 to all three address high registers	01
Write red data to alternate (location $00)	10
Write green data to alternate (location $00)	10
Write blue data to alternate (location $00)	10
Write red data to alternate (location $01)	10
Write green data to alternate (location $01)	10
Write blue data to alternate (location $01)	10
:	:
Write red data to alternate (location $FF)	10
Write green data to alternate (location $FF)	10
Write blue data to alternate (location $FF)	10

Overlay Color Palette Initialization

Write $00 to all three address low registers	00
Write $01 to all three address high registers	00
Write red data to overlay (location $00)	10
Write green data to overlay (location $00)	10
Write blue data to overlay (location $00)	10
Write red data to overlay (location $01)	10
Write green data to overlay (location $01)	10
Write blue data to overlay (location $01)	10
:	:
Write red data to overlay (location $1F)	10
Write green data to overlay (location $1F)	10
Write blue data to overlay (location $1F)	10

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
PGA	TJ			+150	°C
PQFP	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow					
PGA		0			l.f.p.m.
PQFP		50			l.f.p.m.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output					
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4V)	IIH			1	µA
Input Low Current (Vin = 0.4V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	V
Input High Current (Vin = 4.0V)	IKIH			1	µA
Input Low Current (Vin = 0.4V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output	IOUT				
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	–1.0		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance	CAOUT		13	20	pF
(f = 1 MHz, IOUT = 0 mA)					
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–1.0		+2.5	V
Output Impedance			50		kΩ
Output Capacitance			15		pF
(f = 1 MHz, PLL = 0 mA)					
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Bt461 170/ Bt462 160		170/160 MHz Devices			135 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			170/160			135	MHz
LD* Rate	LDmax			42.5/40			45	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	60			60			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5.88/6.25			7.4			ns
Clock Pulse Width High Time	13	2.6/2.8			3.2			ns
Clock Pulse Width Low Time	14	2.6/2.8			3.2			ns
LD* Cycle Time	15	23.5/25			22.2			ns
LD* Pulse Width High Time	16	11			8			ns
LD* Pulse Width Low Time	17	11			8			ns
Analog Output Delay	18							
Bt461			11			11		ns
Bt462			5			5		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			6			8	ns
Clock and Data Feedthrough (Note 1)			tbd			tbd		dB
Glitch Impulse (Note 1)			50			50		pV - sec
Pipeline Delay								
Bt461		6		10	6		10	Clocks
Bt462		8		12	8		12	Clocks
VAA Supply Current (Note 2)	IAA							
Bt461			350	470		330	445	mA
Bt462			344	388		319	365	mA

See test conditions and notes at the end of this section.

DC specifications to remain unchanged.

5

AC Characteristics (continued)

		110 MHz Devices			80 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			36.7			26.7	MHz
R/W, C0, C1 Setup Time	1				0			ns
R/W, C0, C1 Hold Time	2				15			ns
CE* Low Time	3	0			60			ns
CE* High Time	4				25			ns
CE* Asserted to Data Bus Driven	5	15			7			ns
CE* Asserted to Data Valid	6			75			100	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	60			50			ns
Write Data Hold Time	9				0			ns
Pixel and Control Setup Time	10	25			4			ns
Pixel and Control Hold Time	11	7			2			ns
Clock Cycle Time	12				12.5			ns
Clock Pulse Width High Time	13				5			ns
Clock Pulse Width Low Time	14				5			ns
LD* Cycle Time	15				37.5			ns
LD* Pulse Width High Time	16				12			ns
LD* Pulse Width Low Time	17	35			12			ns
Analog Output Delay	18	0						
Bt461			11			11		ns
Bt462			5			5		ns
Analog Output Rise/Fall Time	19		2			3		ns
Analog Output Settling Time	20	3		8			12	ns
Clock and Data Feedthrough (Note 1)			tbd			tbd		dB
Glitch Impulse (Note 1)		2	50			50		pV - sec
Pipeline Delay								
Bt461				10	6		10	Clocks
Bt462		9.09		12	8		12	Clocks
VAA Supply Current (Note 2)	IAA	4						
Bt461			320	430		300	410	mA
Bt462		4	301	344		267	312	mA

See test conditions and notes on next page.

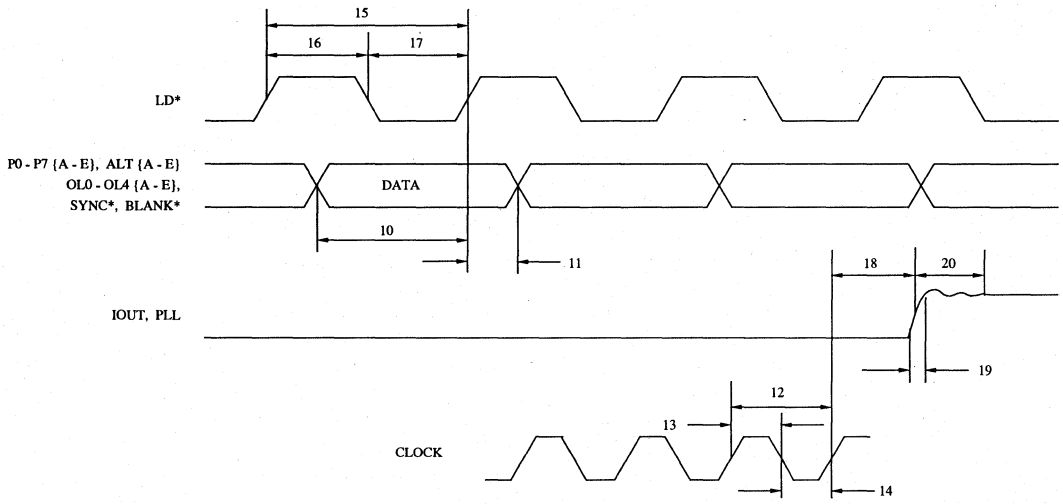
AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing waveforms and notes in Figures 9 and 10. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 9. Video Input/Output Timing.

Timing Waveforms (continued)

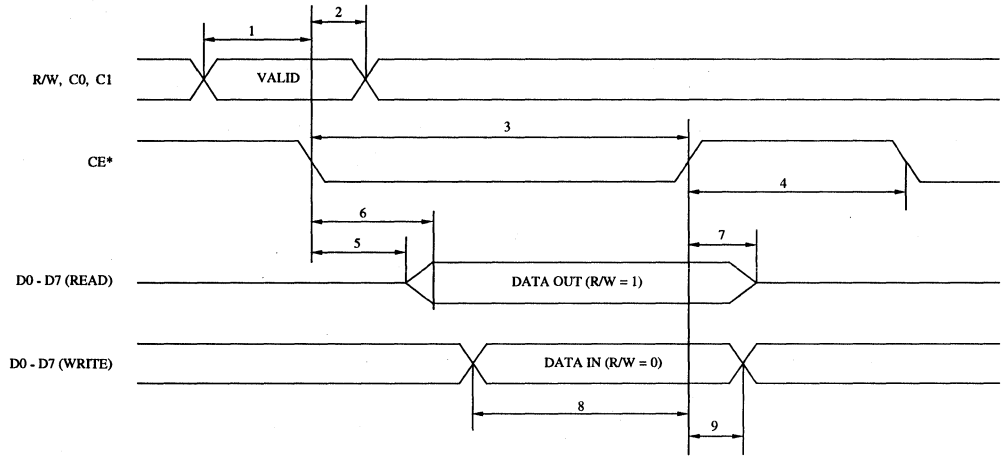


Figure 10. MPU Read/Write Timing Dimensions.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt461KG170	170 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG160	160 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KPF160	160 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF135	135 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF110	110 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF80	80 MHz	132-pin Plastic Quad Flatpack	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt463

135 MHz
Monolithic CMOS
TrueVu™ RAMDAC™

Distinguishing Features

- 135, 110 MHz Operation
- Multiple Display Modes on a Pixel Basis
- Multiple Color Maps
- Variable Palette Sizes
- Up to 8 Overlay Planes
- Reconfigurable Pixel Port
- 1:1, 2:1, or 4:1 Multiplexed Pixel Ports
- Three 528 x 8 Color Palette RAMs
- Programmable Setup (0 or 7.5 IRE)
- X-Windows Support
- Input and Output Signature Registers
- JTAG Support
- 169-pin PGA Package

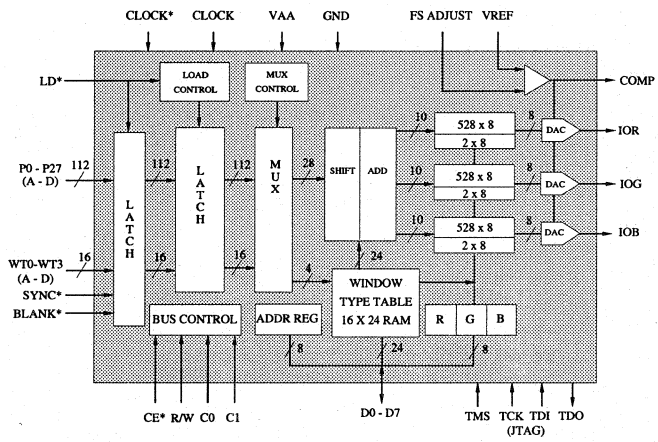
Applications

- High Resolution Color Graphics
- Medical Imaging
- Visualization
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438

Functional Block Diagram



Product Description

The Bt463 is a high-performance RAMDAC designed specifically for true-color and pseudo- color graphics addressing multiple lookup tables for different windows. It has three 528 x 8 lookup tables with triple 8-bit D/A converters to support 24-bit true-color and 9-bit pseudo-color operation.

The TrueVu™ RAMDAC allows different display modes of operation for each pixel. Using a proprietary window type scheme, each set of pixel and overlay data has 4 type bits that map the accompanying pixel data to a user-defined display mode. The type bits address a window type table that ultimately determines the description of the pixel data. With this scheme, arbitrary plane depth and unique visual display type can be achieved on a pixel basis. For example, separate windows displaying 24-plane true color, 8-plane pseudo color, and 12-plane double-buffer true color, each with a separate color map, can exist within a single frame. The size of each lookup table is user configurable and can vary from 16–512 addresses.

On-chip features include programmable 1:1, 2:1, or 4:1 input multiplexing of the pixels, bit plane masking, and a programmable setup (0 or 7.5 IRE). The Bt463 has significant testability features, including input and output signature analysis registers, and fully supports the Joint Test Action Group (JTAG) specification.

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Brooktree®

Introduction

Because X Windows is becoming the de facto standard, each window should have its unique color map and display type. Each window should be able to use its own private color map and define its own interpretation of pixel values in the frame buffer with a variety of possible visual types. In addition, since each window is independent of other windows, the hardware must be able to accommodate multiple visual types within a single frame of graphics display. Thus, the ability to switch to different color maps and visual types on a pixel-by-pixel basis is essential. The Bt463 has been designed specifically to address multiple windows and display types. The Bt463 is extremely flexible, permitting multiple visual types to be displayed simultaneously and efficiently supporting multiple virtual color maps within the physical color map.

Overview

Window type data is sent to the True-Vu™ RAMDAC with each pixel. The window type addresses a 16 x 24 window type table, which converts pixels from a virtual color map index to a physical color map index prior to sending them to the lookup table. In addition to specifying the physical color map location and display type, the window type table can determine the number of planes, location of the frame buffer data, and location of overlay data, and can select specific overlay planes for each window.

Even though the Bt463 has 24-plane true color capability, the assignment of red, green, and blue pins is not fixed to preassigned locations. The Bt463 is flexible, allowing pixel or overlay data to be in practically any location of the 28-bit pixel/overlay word and to be shifted into position to address the lookup table. With this flexibility, the Bt463 can be configured in a variety of ways. A number of possible configurations is listed in Table 1.

Pixel Pin Location	Mapped Function	Display Mode
P0–P7 P8–P15 P16–P23 P24–P27	R0–R7 G0–G7 B0–B7 OL0–OL3	24-bit true color 4-plane overlay
P0–P8 P24–P27	P0–P8 OL0–OL3	9-bit pseudo color 4-plane overlay
P8–P15 P16–P19	P0–P7 OL0–OL3	8-bit pseudo color 4-plane overlay
P0–P7 P8–P15 P16–P23 P24–P27, WT0–WT3	R0–R7 G0–G7 B0–B7 OL0–OL7	24-bit true color 8-plane overlay
P4–P7 P12–P15 P20–P23 P24–P27	R0–R3 G0–G3 B0–B3 OL0–OL3	12-bit true color 4-plane overlay
P1–P7 P9–P15 P18–P23 P16, P8, P0, P17	R1–R7 G1–G7 B2–B7 OL0, OL1, OL2, OL3	24-bit true color 4-plane overlay

Table 1. Example Pixel/Overlay Configurations and Display Modes.

MPU Interface

As illustrated in the functional block diagram, the Bt463 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers, window type table, and color palettes. The dual-port color palette RAMs allow color updating without contention with the display refresh process.

As presented in Table 2, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 12-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit. ADDR0 and ADDR8 correspond to data bus bit D0. ADDR12–ADDR15 are ignored during MPU write cycles and return logical zeros when read by the MPU.

The control registers and window type table are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 2. All control registers may be written to or read by the MPU at any time. When the MPU is accessing the control registers, the window type table, and the color palette RAM, the address register increments following a read or write cycle.

Writing/Reading Color Palette RAM

To write color data, the MPU loads the address register with the address of the color palette RAM or cursor color register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM or cursor color register. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read the color palette RAM or cursor color register, the MPU loads the address register with the address of the color palette RAM location or cursor color register to be read. Reading color data is similar to writing it, except the MPU executes read cycles.

When accessing the cursor color registers, the address register increments to $0102 following a blue read or write cycle. The color palette RAM does not have a wraparound feature after the last valid address. However, any attempt to write past $020F does not affect previous data load cycles. The address register will reset to $0000 after incrementing past $0FFF.

Writing/Reading Window Type Table

To write the window type table, the MPU writes the address register with the table location to be modified. The MPU performs three successive write cycles (B0–B7, B8–B15, then B16–B23) with B0 the least significant bit. The MPU uses C0 and C1 to select the window type table. B0, B8, and B16 correspond to data bus bit D0. After the third write cycle, the 3 bytes of the table entry are concatenated into a 24-bit word and written to the window type table address specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of 3 bytes to the window type table. To avoid irregular window displays on the screen, MPU accesses to the window type table are restricted to horizontal and vertical retrace periods.

ADDR0–16	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–11)
$0100	10	cursor color 0 (Note 1)
$0101	10	cursor color 1 (Note 1)
$0200	10	ID register ($2A)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0205	10	P0–P7 read mask register
$0206	10	P8–P15 read mask register
$0207	10	P16–P23 read mask register
$0208	10	P24–P27 read mask register
$0209	10	P0–P7 blink mask register (Note 3)
$020A	10	P8–P15 blink mask register (Note 3)
$020B	10	P16–P23 blink mask register (Note 3)
$020C	10	P24–P27 blink mask register (Note 3)
$020D	10	test register
$020E	10	input signature register (Note 2)
$020F	10	output signature register (Note 1)
$0220	10	revision register ($A)
$0300–$030F	10	window type table (Note 1)
$0000–$020F	11	color palette RAM (Note 1)

Note 1: Requires three read/write cycles.
Note 2: Two out of three valid read/write cycles.
Note 3: The blink function is nonoperational for the current revision, Revision B.

Table 2. Address Register (ADDR) Operation.

5

Circuit Description *(continued)*

To read the window type table data, the MPU loads the address register with the address of the type table to be read. Contents of the type table are copied into a 24-bit register, and the address register is incremented to the next window type table entry. The MPU performs three successive read cycles (B0–B7, B8–B15, then B16–B23) with B0 the least significant bit. The MPU uses C0 and C1 to select the window type table. B0, B8, and B16 correspond to data bus bit D0.

Additional Information

When accessing the color palette RAM, window type table, signature analysis registers, or cursor color registers, the address register increments after every third read/write cycle for each addressable location. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

For 8-bit registers, the address increments after every read/write cycle.

Figure 1 illustrates the MPU read/write timing of the Bt463.

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt463 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, window type, and overlay information for either 1, 2, or 4 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 1-, 2-, or 4-pixel resolution. Typically, the LD* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

For 1:1, 2:1, or 4:1 input multiplexing, the Bt463 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until 1, 2, or 4 pixels have been output, at which point the cycle repeats.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 2 or 4, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

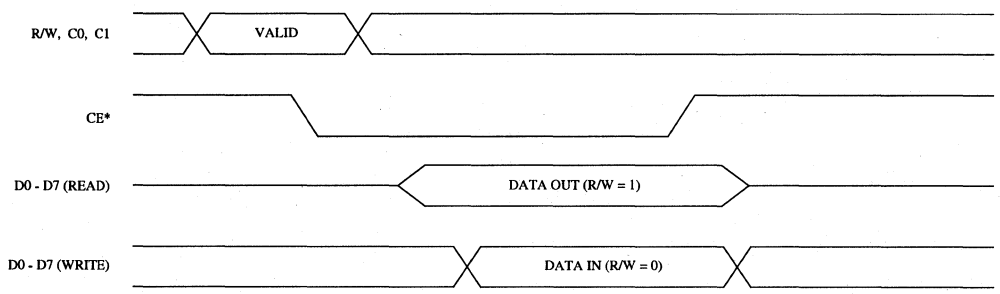


Figure 1. MPU Read/Write Timing.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 1:1 multiplexing is specified, the CLOCK and CLOCK* signals are ignored and pixel data is latched on the rising edge of LD*. If 2:1 multiplexing is specified, only one rising edge of LD* should occur every two clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

Color Palette RAM

The color lookup table consists of three independent RAMs with variable size color maps. Multiple color maps can be assigned within each of the three 528 x 8 lookup tables. The minimum color map size is 16 colors. The color map can be as large as 512 colors.

Color generated by pixel or overlay data is independent of the absolute physical address of the lookup table. Pixel, overlay, and underlay data are referenced relative to their own color maps. The start address indicating the beginning of each physical color map is added to the pixel data to generate the address for the final color. The start address is specified through the window type table.

Window Type Table

Window type data is sent to the RAMDAC with each pixel. The window type addresses a 16 x 24 window type table, selecting one of sixteen 24-bit window type words. The window type word reconfigures the mapping of the input pixels to the RAMDAC, pixel by pixel. Each color map requires a pointing index to convert pixels from a virtual color map index to a physical color map index. In addition to specifying the physical color map location and display type, the window type table can determine the number of planes, location of the frame buffer data, and location of overlay data, and can select specific overlay planes for each window.

Even though the Bt463 has 24-plane true-color capability, the assignment of red, green, and blue pins is not fixed to preassigned locations. The Bt463 is flexible, providing capabilities to have pixel or overlay data in practically any location of the 28-bit pixel/overlay word. The pixels are shifted into position where they address the lookup table. With this flexibility, the Bt463 can be configured in a variety of ways, such as those listed in Table 1.

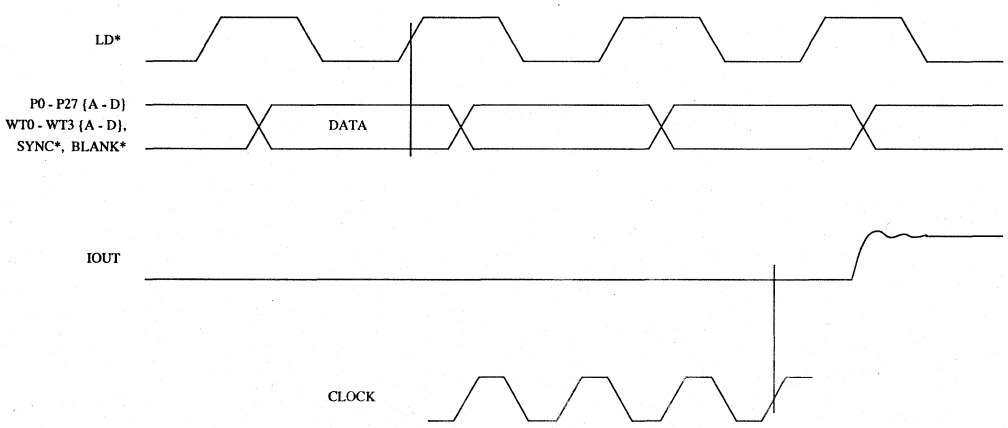


Figure 2. Video Input/Output Timing.

Circuit Description *(continued)*

Associated with each set of pixel data is a 4-bit window type word (WT0–WT3). The window type addresses 1 of 16 possible entries of the window type table. Each 24-bit window type entry is associated with a particular configuration mode that specifies the number of planes, window display type, start address of the physical color map, shift constant, overlay location, and bypass operation. Multiple windows using the same configuration mode can address the same entry of the window type table, as illustrated in Figure 3. It is recommended that the window type table be loaded by the MPU during vertical retrace to minimize disruptions during the display process.

The window type table provides the capability to switch back and forth between different display modes and individual color maps on a pixel-by-pixel basis. For example, the Bt463 can switch from 24-plane true color to 12-plane true color to 8-plane pseudo color, all within a single frame of graphic data. This allows users to personalize color maps specific to individual windows.

Users can optionally designate the fifteenth and sixteenth codes of the window type table to be used as a cursor. These two window type codes directly address the cursor palette, bypassing all pixel manipulation operations. This feature eliminates the need to use the overlay ports as an interface to a hardware cursor. Window type $E is defined as cursor color 0 and $F is cursor color 1.

The window type table words consist of seven different fields that map the function of the accompanying pixel data. The seven fields, shown in Figure 4, are: shift, number of planes, display mode, overlay location, overlay mask, start address, and lookup table bypass. These fields are described in detail in the following sections.

Window Type Table Fields

Shift <B4:B0>

This field specifies the plane position where active planes begin. If the active planes are in higher order bits, the shift field can shift these bits into the least significant position that will address the RAM. For instance, a value of 8 specifies active planes to begin at position P8. This field is particularly useful for double-buffer applications. The shift value applies to the entire 28-bit pixel/overlay input. Legal values are 0 through 27. However, the number of planes plus the shift value should not exceed 28 within one window type table entry.

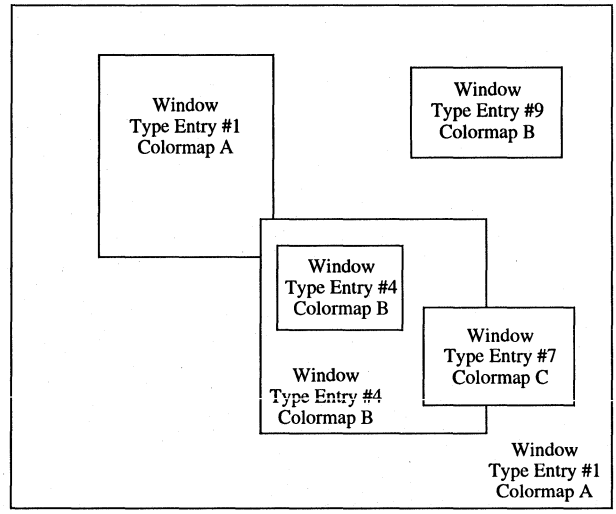


Figure 3. Multiple Windows Using Different Color Maps.

Circuit Description *(continued)*

Number of Planes <B8:B5>

This field determines the number of active planes used for pixel data. Zeros will be inserted in bit planes above the specified MSB. For true-color modes, the appropriate value in this field corresponds to the number of planes per channel. For instance, a 24-plane true-color window should specify eight as the number of planes. Legal values for this field are 0 through 8 for true-color and 0 through 9 for pseudo-color windows. Zero planes correspond to the color at the start address location regardless of pixel data, dependent on overlay and cursor data. This is useful for generating background color or flood color while the window is being changed or moved. The number of planes plus the shift value should not exceed 28 for the pseudo-color mode. The number of planes times 3 plus the shift value shound not exceed 28 for the true-color mode.

Display Mode <B11:B9>

This field determines the display mode of the pixel data. Valid display options are true color, pseudo color, bank select, 12-plane double-buffer true color, and pseudo color with load interleave. Table 3 contains full display mode descriptions.

Overlay Location <B12>

The overlay location field specifies the source location of the overlay planes. A logical zero specifies overlay data to come from P<27:24>. The overlay location is fixed to these four pixel locations, unaffected by any shift in the shift fields. A logical one in this field specifies overlay data to come from the least significant bits of the pixel data (true-color mode) or the four planes above the pixel planes (pseudo-color mode). The overlay locations for the true color mode are P<17, 0, 8, 16> with P16 the LSB of the overlay word. The overlay location is affected by the shift value and only uses these variable locations after the shift operation has been completed.

Overlay Mask <B16:B13>

The overlay mask field is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette. B13 corresponds to OL0. B13–B16 are logically ANDed with the corresponding overlay plane input. The selected overlay planes are then compacted into the LSB positions with the higher significant bits filled with zeroes. This feature allows the user to assign specific overlay planes to individual windows. Two or more separate overlay images can be generated independently and switched on a pixel-by-pixel basis with the same or different overlay palette.

Start Address <B22:B17>

The start address specifies the beginning of the physical address of each color map. Pixel data addresses the lookup table independent of the absolute physical location of the color map. The start address constitutes the 6 MSBs of the start rows of the color maps. Color address is generated by adding the pixel data with the start address in the physical color map. The maximum valid physical address resulting from this addition is $020F. Color maps start on 16 row boundaries and are allocated in blocks of 16. Thus, a binary value of 000001 corresponds to the physical address location of $0010. It is not necessary to fill the entire block with color-map colors. The resultant value from pixel data plus the start address should not exceed the 528-address space of the lookup table. Various color maps can be disjoint; they may overlap or be subsets of other color maps. Minimum color map size is 16, while the maximum contiguous color map size is 512 colors. Legal values are 000000 through 100000.

Lookup Table Bypass <B23>

Up to 24 bits of pixel information are input with P0–P27 inputs. Even in the bypass mode, pixel manipulation still occurs with the 8 lowest significant bits used for each DAC. After shifting, pixels that are in the LSB positions, P0–P7, are mapped as R0–R7, bypass the red color palette, and drive the red DAC directly. Similarly, P8–P15 pixels are mapped as G0–G7 and drive the green DAC directly. P16–P23 are mapped as B0–B7 and drive the blue DAC directly. The bypass mode can only be used in the eight-plane mode.

With the display mode set to pseudo color, the bypass bit will generate 256 shades of gray scale. Eight bits of color information are applied equally to each of the three DACs.

In the bypass mode, overlays are still effective in either the four- or eight-plane mode and address the overlay palette.

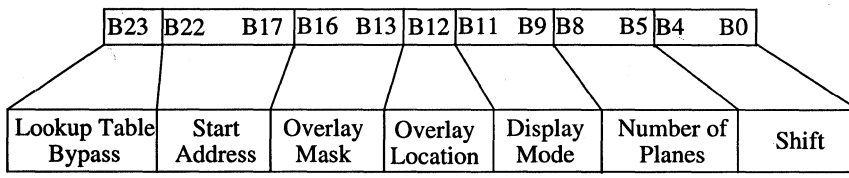


Figure 4. Window Type Table Fields.

Display Mode	Field	Description
True Color	000	An equal number of red, green, and blue pixel planes are input through the pixel port. The number of bits of true color depends on the "number of planes" field in the window type table. Eventually, pixel data must be shifted so that the least significant bit of the red pixel word is P0, green is P8, and blue is P16. The maximum number of active planes is eight for the true-color modes. Correspondingly, the number of planes for the pixel data is 3 times the value in this field for true color. For example, a value of 8 in the plane field yields 24-plane true color. A value of 4 in the plane field yields a 12-plane true-color configuration.
Pseudo Color	001	All three color palette RAMs are addressed by the same planes of pixel data. Pixel data for the pseudo color must come from a contiguous set of planes. The maximum number of active planes is nine for the pseudo-color mode. The number of available planes ranges from zero–nine.
Bank Select	010	Overlay bits are concatenated as the MSBs to the pixel data to address a different portion of the lookup table without changing pixel data. Bank select is especially useful for highlighting or color contrasting by changing overlay inputs rather than regenerating the frame buffer image. The number of planes per channel is zero–eight. The planes used for bank select also depend on the overlay mask. Refer to Figure 5 for more details on the bank-select mode.
	011	Reserved
Twelve-Plane True Color (Load Interleave) (See Figure 6.)	100	Twelve-plane true color is generated by using the lower or upper nibble (4 bits) from 8 bits each of red, green, and blue. Either the upper or lower nibble is latched on each load clock across a scan line, depending on the value of the shift field immediately after blank has been substantiated. The load cycle will begin with the lower nibble for a shift value of $00. If the shift value is $04 immediately after blank, the load cycle will begin with the upper nibble. The output sequence continues to alternate between lower nibble and upper nibble for each load sequence throughout the entire scan line. This display mode preassigns the mapped function for the pixel inputs. P0–P7 are red, P8–P15 are green, and P16–P23 are blue. Refer to Table 4 for more details.
Pseudo Color (Load Interleave) (See Figure 6.)	101	Eight-plane pseudo-color data is generated from either the lower nibble bits or upper nibble bits of red and green pixel data. The green nibble bits are concatenated with the red nibble bits to generate the 8-bit pseudo-color pixel word. The red nibble bits are the least significant bits. Either the upper or lower nibble is latched on each load clock across a scan line, depending on the value of the shift field immediately after blank has been substantiated. The load cycle will begin with the lower nibble for a shift value of $00. If the shift value is $04 immediately after blank, the load cycle will begin with the upper nibble. The output sequence continues to alternate between lower nibble and upper nibble for each load sequence throughout the entire scan line. Refer to Table 5 for more details.
	110	Reserved
	111	Reserved

Table 3. Display Mode Options.

Circuit Description *(continued)*

Pixel Location	Mapped Function	Pixel Word 12-bit True-Color Lower Nibble	Lower Nibble Output Sequence	Pixel Word 12-bit True-Color Upper Nibble	Upper Nibble Output Sequence
P0–P7 P8–P15 P16–P23	R0–R7 G0–G7 B0–B7	R0–R3 G0–G3 B0–B3	$A_LB_LC_LD_L$	R4–R7 G4–G7 B4–B7	$A_HB_HC_HD_H$

Table 4. 12-Bit True-Color (Load Interleave) Mapping and Output Sequence.

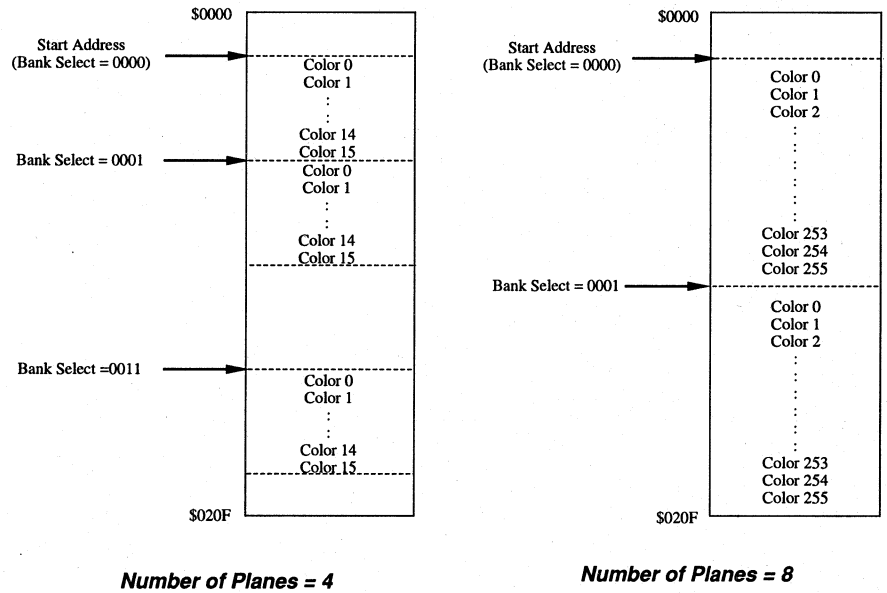


Figure 5. Color Map Allocation With Bank Select.

Pixel Location	Mapped Function	Pixel Word 8-bit Pseudo-Color Lower Nibble	Lower Nibble Output Sequence	Pixel Word 8-bit Pseudo-Color Upper Nibble	Upper Nibble Output Sequence
P0–P7 P8–P15 P16–P23	R0–R7 G0–G7 B0–B7	G0–G3, R0–R3	$A_LB_LC_LD_L$	G4–G7, R4–R7	$A_HB_HC_HD_H$

Table 5. 8-Bit Pseudo-Color (Load Interleave) Mapping and Output Sequence.

Circuit Description *(continued)*

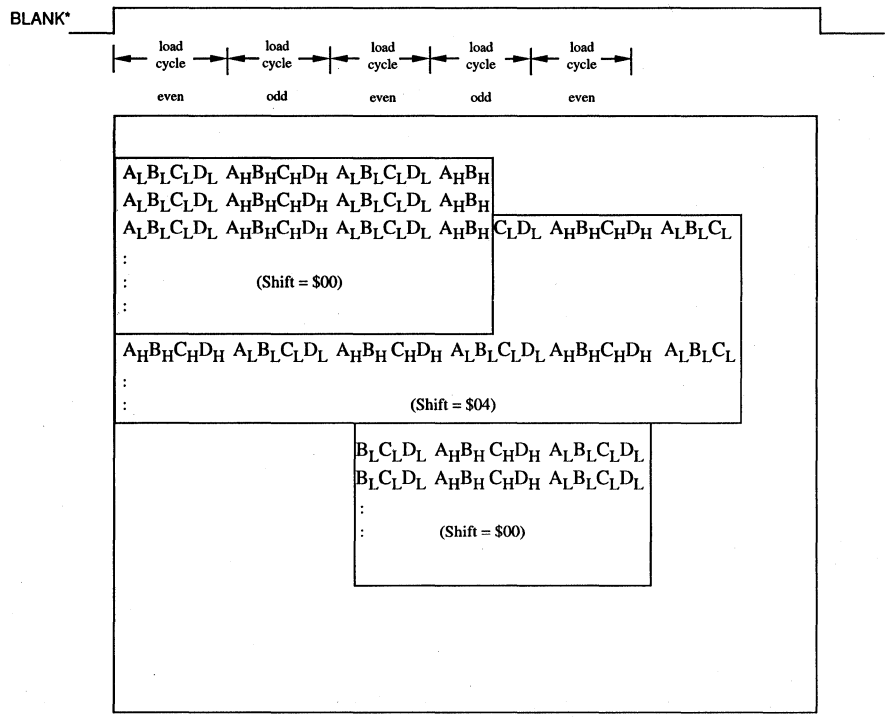


Figure 6. Load Interleave Output Sequence.

Video Generation

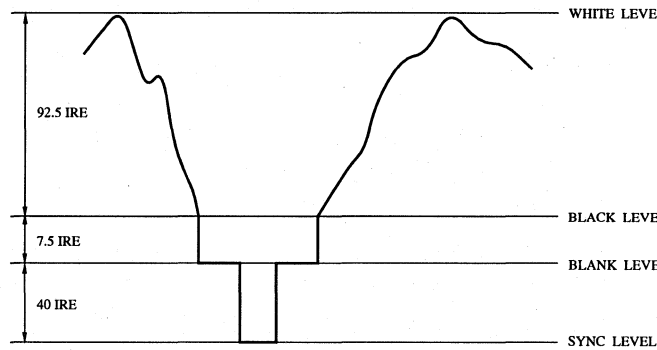
Every clock cycle, the color information (up to 24 bits) is presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 7 and 8. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt463 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 7. Composite Video Output Waveform (SETUP = 7.5 IRE).

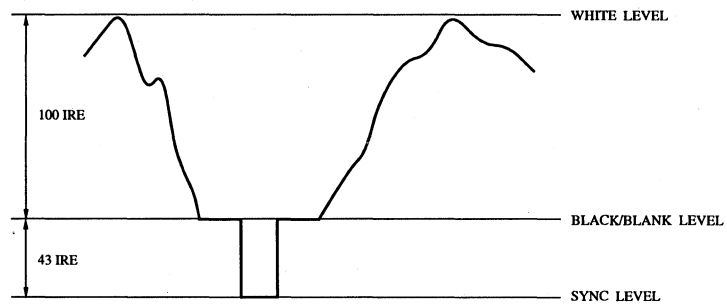
Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 8. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

Overlay and Underlay Operation

The Bt463 has capabilities for multiple plane overlay and underlay operation. The overlay palette may be indexed to each of the independent color maps as specified by the user. Overlay color is determined by subtracting $10 from the start address referenced in the window type table and adding the overlay value.

Overlay data can originate from a number of sources. The source location of the overlays is determined by the window type word and command register. All display modes can use pixel ports 24 to 27 for the overlay address. Also, in pseudo-color applications, the overlay information can originate from the four planes above the pixel planes. For instance, if pixel information is being addressed from P0 to P7, then overlay planes may come from P8 through P11 with P8 the LSB of the overlay word.

In true-color applications, overlay information can also be addressed from the least significant bits of the red, green, and blue pixel data. Two LSBs are used from the blue pixel port. The overlay word <OL3:OL0> consists of P17, P0, P8, and P16 (after shift operation) with P16 the LSB of the overlay word. The overlay enable mask bits designate whether some or all of the LSB pixel data is to be used as overlay planes.

Instead of multiple overlay palettes, a fixed overlay location can be chosen for all window type entries. The location of the common overlay palette is fixed, independent of the start address of the window type table. The common overlay palette is located at addresses $0201 to $020F.

Underlay operations with various planes can be achieved by changing command register bit CR12 to underlay operation. When this bit is set for underlay operation, OL3 determines whether the remaining overlay planes should be interpreted as overlay or underlay. If underlays are unavailable as specified in the command register, then the overlay ports are restricted to cursor and overlay operation only. To obtain overlay and underlay operation, the overlay mask must be set to $F. All other values of the overlay mask would result in a compacted overlay word, yielding only underlay operation.

In the standard mode, the Bt463 uses four overlay/underlay planes, providing a palette of 16 colors. However, the Bt463 has a special mode in which the window type bits serve as the upper nibble to the overlay port. When a command register bit is set, eight overlay planes become available. However, no window operation is available, as these window type ports are used strictly for overlay ports. Hardware cursor is still available through OL0 and OL1. Both true-color and pseudo-color operations are available in the eight-overlay-plane mode. The physical location of the overlay palette is fixed to a preassigned location.

If a color map start address is specified to be $0000, then overlay colors are located at physical address $0201–$020F. Other start addresses are shown in Figure 9, a diagram of the overlay and pixel palette color-map scheme. Tables 8 and 9 detail overlay operation for different modes.

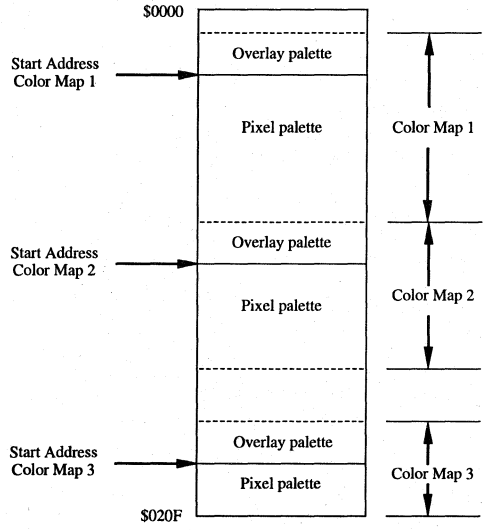


Figure 9. Example Overlay and Pixel Palette Color Map Scheme.

Circuit Description *(continued)*

Display Mode	Window Type Field <B11:B9>	Overlay Location <B12>	Overlay Location <OL3:OL0>
True Color	000 000	0 1	P <27:24> P <17, 0, 8, 16>
Pseudo Color	001 001	0 1	P <27:24> P <planes+3:planes>
Bank Select	010 010	0 1	P <27:24> P <17, 0, 8, 16>
12-Plane True Color (Load Interleave)	100 100	0 1	P <27:24> P <17, 0, 8, 16>
Pseudo Color (Load Interleave)	101 101	0 1	P <27:24> not available

Table 8. Overlay Location Truth Table.

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram Location Addressed by Frame Buffer	Operating Mode
x x : x	0000 0000 : 0000	$000 $001 : $1FF	Start Address + $000 Start Address + $001 : Start Address + $1FF	pixel data
0 : 0 0	1111 : 0010 0001	$xxx : $xxx $xxx	Start Address–$10+ $F : Start Address–$10 + $2 Start Address–$10 + $1	overlay only
1 1 1 1 1 1 1 1	1111 1110 1101 1100 1011 1010 1001 1000	$xxx $xxx $xxx $xxx $xxx $xxx $xxx $xxx	Start Address–$10 + $F Start Address–$10 + $E Start Address–$10 + $D Start Address–$10 + $C Start Address–$10 + $B Start Address–$10 + $A Start Address–$10 + $9 Start Address–$10 + $8	overlay
1 1 1 1 1 1 1	0111 0110 0101 0100 0011 0010 0001	$000 $000 $000 $000 $000 $000 $000	Start Address– $10 + $7 Start Address–$10 + $6 Start Address–$10 + $5 Start Address–$10 + $4 Start Address–$10 + $3 Start Address–$10 + $2 Start Address–$10 + $1	underlay

Table 9. Palette and Overlay Select Truth Table (No Hardware Cursor Interfacing the Overlay Port) (CR<11:10> = 00, B<16:13> = $F).

Circuit Description *(continued)*

Hardware Cursor Interface

The Bt463 has numerous configurations for interfacing with a hardware cursor. Using two entry codes of the window type table for a two-color cursor provides the best method of maximizing overlay plane availability without sacrificing a large number of window type entries.

Otherwise, the overlay ports can be used directly as cursor ports but require setting command register bits CR10 and CR11 to configure the RAMDAC for either a single-plane cursor or dual-plane cursor through the overlay port. Adding cursor planes through the overlay port reduces the available colors for overlays and underlays.

Single-Plane Cursor (Overlay Port)

In the single-plane cursor mode, OL0 directly addresses the cursor color palette and overrides all other inputs. By setting a command register, mapped function OL3 determines whether OL1 and OL2 serve as overlay or underlays. Only seven combinations of overlays/ underlays are available. Refer to Table 10 for more details.

Dual-Plane Cursor (Overlay Port)

In the dual-plane cursor mode, both mapped functions OL0 and OL1 become cursor planes with OL0 the least significant bit. With the underlay enabled, OL3 determines whether OL2 serves as an overlay or an underlay. Refer to Table 11 for more details.

Dual-Plane Cursor (Window Type Port)

In the dual-plane cursor mode, mapped functions $E and $F of the window type table are used to select Cursor 0 and Cursor 2. Refer to Table 12 for more details.

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Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram Location Addressed by Frame Buffer	Operating Mode
x	0000	$000	Start Address + $000	
x	0000	$001	Start Address + $001	pixel
:	:	:	:	data
x	0000	$1FF	Start Address + $1FF	
x	xxx1	$xxx	Cursor Color 0	cursor
0	1110	$xxx	Start Address–$10 + $E	
0	1100	$xxx	Start Address–$10 + $C	
0	1010	$xxx	Start Address–$10 + $A	overlay
0	1000	$xxx	Start Address–$10 + $8	only
0	0110	$xxx	Start Address–$10 + $6	
0	0100	$xxx	Start Address–$10 + $4	
0	0010	$xxx	Start Address–$10 + $2	
x	xxx1	$xxx	Cursor Color 0	cursor
1	1110	$xxx	Start Address–$10 + $E	
1	1100	$xxx	Start Address–$10 + $C	overlay
1	1010	$xxx	Start Address–$10 + $A	
1	1000	$xxx	Start Address–$10 + $8	
1	0110	$000	Start Address–$10 + $6	
1	0100	$000	Start Address–$10 + $4	underlay
1	0010	$000	Start Address–$10 + $2	

Table 10. Palette and Overlay Select Truth Table (Single-Plane Hardware Cursor Interfacing the Overlay Port) (CR<11:10> = 01, B<16:13> = $F).

Circuit Description *(continued)*

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram Location Addressed by Frame Buffer	Operating Mode
x	0000	$000	Start Address + $000	pixel data
x	0000	$001	Start Address + $001	
:	:	:	:	
x	0000	$1FF	Start Address + $1FF	
x	xx01	$xxx	Cursor Color 0	cursor
x	xx1x	$xxx	Cursor Color 1	
0	1100	$xxx	Start Address–$10 + $C	overlay only
0	1000	$xxx	Start Address–$10 + $8	
0	0100	$xxx	Start Address–$10 + $4	
x	xx01	$xxx	Cursor Color 0	cursor
x	xx1x	$xxx	Cursor Color 1	
1	1100	$xxx	Start Address–$10 + $C	overlay
1	1000	$xxx	Start Address–$10 + $8	
1	0100	$000	Start Address–$10 + $4	underlay

Table 11. Palette and Overlay Select Truth Table (Dual-Plane Hardware Cursor Interfacing the Overlay Port) (CR<11:10> = 10, B<16:13> = $F).

Mapped Function <WT3:WT0>	
0000	Window Type Table Field 0
0001	Window Type Table Field 1
:	:
1101	Window Type Table Field $D
1110	Cursor Color 0 $E
1111	Cursor Color 1 $F

CR11 and CR10 = 10 Two Cursor Plane
CR13 = 1 Limited Window Type Table to 14 Entries

Table 12. Cursor and Window Type Select Truth Tables.

Boundary Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt463 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the JTAG. Conforming to the IEEE P1149.1, Standard Test Access Port and Boundary Scan Architecture, the Bt463 has dedicated pins that are used for testability purposes only.

JTAG's approach to testability uses boundary scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a Boundary Scan Register (BSR) that applies or captures test data used for functional verification of the RAMDAC. The JTAG approach is particularly useful for board testers that use functional testing methods.

Circuit Description *(continued)*

The JTAG approach is with four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data Input), and TDO (Test Data Out). These four TAP pins can completely verify the RAMDAC. With boundary scan cells at each digital pin, the Bt463 can apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access to and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned on the TDO pin and externally checked. While isolating the Bt463 from the other components on the board, the user has easy access to all Bt463 digital pins through the TAP and can perform complete functionality tests without expensive bed-of-nails testers.

The bidirectional MPU port is given special attention with respect to the JTAG standards. Because JTAG requires control over each digital pin, an additional Output Enable (OE) function is included in the BSR for the MPU pins. In conjunction with the JTAG instruction, the output enable will configure the MPU port as an input or output.

With the JTAG bus, users also have access to a vital portion of the Bt463, the Output Signature Analysis Register (OSAR) (See Figure 10). With access to this register, users can easily verify expected video data serially through the JTAG port. The OSAR is located between the lookup table and the inputs to the DACs.

The Power-On Reset (POR) circuitry ensures that the Bt463 initializes each pin to operate in a RAMDAC mode instead of a JTAG test mode during power-up sequence.

A variety of verification procedures can be performed through the TAP controller. Through a set of eight instructions, the Bt463 can verify board connectivity at all digital pins, generate artificial pixel vectors on chip, check signatures on system pixel streams, and scan vectors in and out of the pixel shifter and signature analysis register. The instructions are accessible through a simple state machine.

Note: Since the boundary scan (JTAG) circuitry is intended for gross functional verification, it is tested and guaranteed operational at VAA ≥ 5.0 V and VIL on JTAG pins at 0.6 V maximum. Maximum JTAG clock speed (TCK) is 50 MHz.

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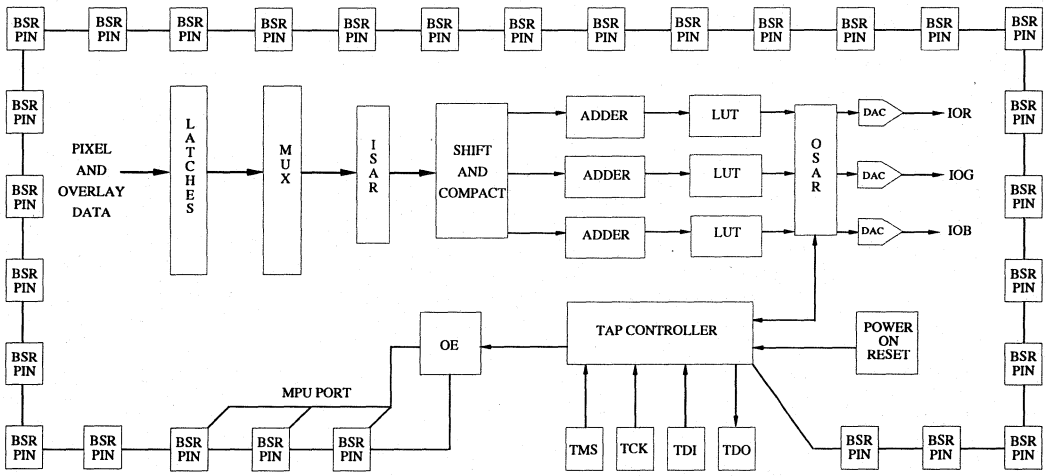

Figure 10. JTAG Block Diagram.

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 2:1 multiplexing

These bits specify whether 1:1, 2:1, or 4:1 multiplexing is to be used for the pixel and overlay inputs. If 2:1 is specified, the {C} and {D} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one half the CLOCK rate. If 4:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fourth the CLOCK rate. If 1:1 is specified, the {B}, {C}, and {D} inputs are ignored.

In the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

The pipeline delay of the Bt463 can be reset to a fixed 13 clock cycles. In this instance, each time the input multiplexing is changed, the Bt463 must again be reset to a fixed pipeline delay.

CR05, CR04 reserved (logical zero)

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off). The counters that determine the blink rate are reset when command register_0 is written to. The blink function is nonoperational for the current revision, Revision B.

CR01, CR00 reserved (logical zero)

Internal Registers *(continued)*

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR10 corresponds to data bus bit D0.

CR17 reserved (logical zero)

CR16 Overlay mapping

(0) Mapped to start address
(1) Mapped to common palette

This bit determines the physical address location of the overlay. In the standard mode, overlays are addressed with respect to the start address specified in the start address field of the window type table. The alternate mapping option addresses the same portion of the color map for overlays, regardless of the start address location. In this mode, the overlays must be located at physical address locations $0201–$020F.

CR15 Contiguous Plane Configuration

(0) 24/28 planes contiguous
(1) 12/16 planes contiguous

This bit allows the Bt463 to be used with 12- or 16-plane systems with an easy field upgrade to 24/28 planes. In the 12/16 plane configuration, up to 12 planes of true color are available. Red must be entered at P<3:0>, blue at P<4:7>, and green at P<11:8>. No shift is of use with 12-plane true color, and the shift value in the window type word should be set to 0. The standard pseudo-color mode is available, up to nine planes. In this mode, the shift value should be between 0 and either 11 (12-plane systems) or 15 (16-plane systems). In 16-plane systems, the four planes of overlay should be entered at P<15:12>. If the alternate location overlay is selected, then overlays are input at P<5,0,8,4> for the true-color mode or at P<P+3:P> for the pseudo-color mode. Unused pixel pins must be grounded.

CR14 Overlay planes select

(0) 4 overlay planes
(1) 8 overlay planes

This bit inacts a special mode that configures the Bt463 for eight overlay planes. This mode can be used for either the standard true-color or pseudo-color display modes. For true-color applications, the red pixel port corresponds to P0–P7, green corresponds to P8–P15, and blue corresponds to P16–P23. The 4 least significant overlay bits, OL0–OL3, are assigned pixel port P24–P27. The window type port is converted into the 4 most significant bits of the overlay port where WT0–WT3 correspond to OL4–OL7, respectively. All 16 window type entries must be loaded and must be set to the same value. The recommended

Command Register_1 (continued)

configuration is true color, no shift, eight planes, all overlay inputs enabled, and the standard overlay location. Although different window display modes are no longer available, pixel operation is still user defined, based on the window type word placed in all 16 type entries. The only field with a restriction is the start address, which should have a value of 010000 ($0100). Thus, the physical locations of the pixel lookup table and the overlay palette are preassigned with the pixel color palette starting from $0100 and ending at $01FF, while the overlay palette RAM is located at $0000–$00FF.

CR13 — Window type entries

(0) 16 entries
(1) 14 entries

This bit determines the number of entries available in the window type table. If 14 entries are selected, then the two window type codes, $E and $F, correspond to cursor color 0 and cursor color 1, respectively.

CR12 — Underlay enable

(0) underlays disabled
(1) underlays enabled

This bit determines the underlay availability. When this bit is set to a logical one, underlays operation is achieved when the OL3 plane is a logical zero.

CR11–CR10 — Overlay configuration

(00) no cursor
(01) one cursor plane
(10) two cursor planes
(11) reserved

These bits configure the overlay port so that overlay pins may be used as a hardware cursor port. By configuring this register, these overlay ports will directly address the cursor palette. If the overlay ports are used for cursors, they must be used on OL0 and OL1. OL0 is the least significant cursor bit. OL0 must be used for the single-cursor mode. This overlay configuration register applies to the standard four-plane mode or the eight-plane overlay option.

Internal Registers *(continued)*

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. A 0 IRE specifies that the black and blank levels are the same.
CR25–CR23	reserved (logical zero)	
CR22	Input SAR capture selection (0) lower 16 bits (1) upper 16 bits	This bit specifies whether the 16-bit input Signature Analysis Register (SAR) should capture the lower or upper 16 bits of the pixel path. The input SAR is guaranteed operational only for the 110 MHz speed grade on the current revision (B).
CR21	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all SAR clocking. Logical zero is the normal mode with pixel position (A, B, C, or D) determined by the test register. Logical one is a special mode for chip testing. (In this instance, SAR operation is not guaranteed for clock rates above 30 MHz.)
CR20	Test-mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The SARs are used to hold the test result for both test methods.

Internal Registers *(continued)*

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt463, the value read by the MPU will be $2A. Data written to this register is ignored.

Pixel Read Mask Register

The 28-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. The masking function is independent of all the operations specified by the window type entries, masking the pixel ports prior to pixel manipulation. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0, P8, P16, and P24.

Pixel Blink Mask Register

The 28-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. The blinking function is independent of all the operations specified by the window type entries, blinking the pixel ports prior to pixel manipulation. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0, P8, P16, and P24. The blink function is nonoperational for the current revision, Revision B.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt463. The 4 most significant bits signify the revision letter in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored.

Internal Registers *(continued)*

Red, Green, and Blue Output Signature Analysis Registers (OSARs)

Signature Operation

These three 8-bit signature analysis registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the OSARs while BLANK* is a logical zero to load the seed value. The OSARs use data being loaded into the output DACs to calculate the signatures. JTAG logic can access the OSAR independent of the MPU operation. MPU accesses to the OSARs require one address register load to address $020F, followed by three reads or writes to the red, green, and blue signature registers, respectively. D0 corresponds to R0, G0, and B0.

When a test display is loaded into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

Data-Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

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Input Signature Analysis Registers (ISARs)

Signature Operation

This 16-bit signature analysis register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the ISAR while BLANK* is a logical zero to load the seed value. The ISAR uses P0–P15 or P16–P27, and WT0–WT3 (selected by command bit CR22) to calculate the signatures. The 16 bits of data latched in the ISAR may be masked (forced low) by the read mask registers. MPU accesses to the ISAR require one address register load to $020E, followed by three reads or writes to, respectively, lower byte, upper byte, and dummy access. D0 corresponds to P0 and P8, or to P16 and P24.

When a test display is loaded into the frame buffer, a given value for the ISAR will be returned if all circuitry is working properly.

Note: The input signature analysis register is operational at frequencies < 120 MHz only.

Data-Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the ISAR changes. Rather than determining the signature, it captures and holds the 16 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the ISAR captures the 16 bits of pixel data addressing the color palette RAM. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Internal Registers *(continued)*

Test Register

This 8-bit register is used to test the Bt463. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 2:1 pixel multiplexing is specified, signature analysis is done on every second pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel. D0–D2 are used for 2:1 and 4:1 multiplexing to specify whether to use the A, B, C, or D pixel inputs, as follows:

D2 - D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	reserved
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables comparison of that function; the result is D3. The output levels of the DACs should be constant for 5 µs to allow enough time for detection. The capture occurs over one LD* period set by a logical one at any of the pixel pins P16A, P16B, P16C, or P16D.

For normal operation, D4–D7 must be logical zeros.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 6 and 7. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 10 and 11). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, SYNC*should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P27 {A–D}, WT0–WT3 {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is the output clock (1:1 multiplex mode) or is one half or one fourth of CLOCK, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P27 {A–D}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information. The function of each of these pixel ports is configurable depending on the entry of the window type table. Overlay data may exist from various locations of this pixel port. If data exists in the assigned overlay input port, then pixel data inputs are ignored. Overlay information (up to 4 bits per pixel) for 1, 2, or 4 consecutive pixels is input through this port. One, two, or four consecutive pixels (up to 24 bits per pixel) are input through this port. All 4 pixels (112 bits) are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 1, 2, or 4 pixels have been output, at which point the cycle repeats.
WT0–WT3 {A–D}	Window type inputs (TTL compatible). These inputs are latched on the rising edge of LD*. The window type references a location within the window type table, which configures the corresponding pixel data or overlay data into user-defined display modes. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 14 in the Application Information section). All outputs, whether used or not, should have the same output load.
TCK	Test Clock (TTL compatible). This pin is used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When JTAG operations are not being performed, this pin is pulled low by internal circuitry.
TMS	Test Mode Select (TTL compatible). This is a JTAG input pin whose transitions drive the JTAG state machine through its sequences. When JTAG operations are not being performed, this pin is pulled high by internal circuitry.
TDI	Test Data Input (TTL compatible). This is a JTAG input pin used to load instructions to the TAP controller or to load test vector data for boundary scan operation. When JTAG operations are not being performed, this pin is pulled high by internal circuitry.
TDO	Test Data Output (TTL compatible). This is a JTAG output used to verify test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences and will be three-stated at all other times. When JTAG operations are not being performed, this pin should be left floating.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>COMP</td><td>Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 12 in the PC Board Layout Considerations section). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. The PC Board Layout Considerations section contains critical layout criteria.</td></tr>
<tr><td>FS ADJUST</td><td>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 12). The IRE relationships in Figures 9 and 10 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

RSET (Ω) = K1 * VREF (V) / IOG (mA)

The full-scale output current on IOR and IOB for a given RSET is:

IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)

where K1 and K2 are defined as:

<table><tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr><tr><td>7.5 IRE</td><td>K1 = 11,294</td><td>K2 = 8,067</td></tr><tr><td>0 IRE</td><td>K1 = 10,684</td><td>K2 = 7,457</td></tr></table></td></tr>
<tr><td>VREF</td><td>Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 12, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 12. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CLOCK,
CLOCK*</td><td>Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CE*</td><td>Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.</td></tr>
<tr><td>R/W</td><td>Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be logical zeros. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.</td></tr>
<tr><td>C0, C1</td><td>Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as presented in Table 1. They are latched on the falling edge of CE*.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
</table>

Pin Descriptions *(continued)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	J1	P9A	A10	P19A	T13
SYNC*	H1	P9B	B10	P19B	U13
LD*	H3	P9C	B9	P19C	R13
CLOCK*	J3	P9D	C10	P19D	U14
CLOCK	J2				
		P10A	A12	P20A	R12
P0A	F2	P10B	C11	P20B	U11
P0B	G3	P10C	A11	P20C	T12
P0C	F1	P10D	B11	P20D	U12
P0D	G1				
		P11A	A14	P21A	T11
P1A	F3	P11B	B12	P21B	U9
P1B	D1	P11C	A13	P21C	R11
P1C	E2	P11D	C12	P21D	U10
P1D	E1				
		P12A	A16	P22A	R10
P2A	C2	P12B	C13	P22B	U8
P2B	B1	P12C	A15	P22C	T10
P2C	D2	P12D	B13	P22D	T9
P2D	C1				
		P13A	C14	P23A	T7
P3A	C3	P13B	B15	P23B	U6
P3B	D3	P13C	A17	P23C	T8
P3C	E3	P13D	B14	P23D	U7
P3D	B2				
		P14A	D15	P24A	R6
P4A	A1	P14B	B16	P24B	U4
P4B	B3	P14C	E15	P24C	R7
P4C	C4	P14D	C15	P24D	U5
P4D	D4				
		P15A	D16	P25A	T5
P5A	A3	P15B	C17	P25B	U2
P5B	C5	P15C	C16	P25C	T6
P5C	A2	P15D	B17	P25D	U3
P5D	B4				
		P16A	T16	P26A	T4
P6A	A5	P16B	T17	P26B	R4
P6B	B6	P16C	R16	P26C	R5
P6C	A4	P16D	R17	P26D	U1
P6D	B5				
		P17A	R15	P27A	R3
P7A	A7	P17B	R14	P27B	N3
P7B	C7	P17C	P15	P27C	T3
P7C	A6	P17D	U17	P27D	T1
P7D	C6				
		P18A	T14	TMS	D17
P8A	A9	P18B	U15	TCK	E16
P8B	B8	P18C	T15	TDI	E17
P8C	A8	P18D	U16	TDO	F17
P8D	B7				

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Pin Descriptions *(continued)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
WT0A	P1	IOR	F16	VAA	C8
WT0B	P3	IOG	H15	VAA	G17
WT0C	R1	IOB	F15	VAA	H17
WT0D	T2			VAA	J15
		COMP	K15	VAA	K2
WT1A	M1	FS ADJUST	H16	VAA	R8
WT1B	P2	VREF	G16	VAA	M16
WT1C	N1				
WT1D	R2	CE*	N15	GND	C9
		R/W	N16	GND	G2
WT2A	L1	C1	P17	GND	G15
WT2B	N2	C0	P16	GND	H2
WT2C	L3			GND	L15
WT2D	M3			GND	M15
				GND	R9
WT3A	K1				
WT3B	L2				
WT3C	K3				
WT3D	M2				
D0	N17				
D1	L16				
D2	M17				
D3	K16				
D4	L17				
D5	J16				
D6	K17				
D7	J17				

Pin Descriptions *(continued)*

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
17	P13C	P15D	P15B	TMS	TDI	TD0	VAA	VAA	D7	D6	D4	D2	D0	C1	P16D	P16B	P17D
16	P12A	P14B	P15C	P15A	TCK	IOR	VREF	FSADJ	D5	D3	D1	VAA	R/W	C0	P16C	P16A	P18D
15	P12C	P13B	P14D	P14A	P14C	IOB	GND	IOG	VAA	COMP	GND	GND	CE*	P17C	P17A	P18C	P18B
14	P11A	P13D	P13A												P17B	P18A	P19D
13	P11C	P12D	P12B												P19C	P19A	P19B
12	P10A	P11B	P11D												P20A	P20C	P20D
11	P10C	P10D	P10B												P21C	P21A	P20B
10	P9A	P9B	P9D												P22A	P22C	P21D
9	P8A	P9C	GND												GND	P22D	P21B
8	P8C	P8B	VAA												VAA	P23C	P22B
7	P7A	P8D	P7B												P24C	P23A	P23D
6	P7C	P6B	P7D												P24A	P25C	P23B
5	P6A	P6D	P5B												P26C	P25A	P24D
4	P6C	P5D	P4C	P4D											P26B	P26A	P24B
3	P5A	P4B	P3A	P3B	P3C	P1A	P0B	LD*	CLK*	WT3C	WT2C	WT2D	P27B	WT0B	P27A	P27C	P25D
2	P5C	P3D	P2A	P2C	P1C	P0A	GND	GND	CLK	VAA	WT3B	WT3D	WT2B	WT1B	WT1D	WT0D	P25B
1	P4A	P2B	P2D	P1B	P1D	P0C	P0D	SYNC*	BLK*	WT3A	WT2A	WT1A	WT1C	WT0A	WT0C	P27D	P26D

Bt463

(TOP VIEW)

alignment marker (on top)

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Pin Descriptions *(continued)*—169-pin PGA Package

	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
17	P17D	P16B	P16D	C1	D0	D2	D4	D6	D7	VAA	VAA	TD0	TDI	TMS	P15B	P15D	P13C
16	P18D	P16A	P16C	C0	R/W	VAA	D1	D3	D5	FSADJ	VREF	IOR	TCK	P15A	P15C	P14B	P12A
15	P18B	P18C	P17A	P17C	CE*	GND	GND	COMP	VAA	IOG	GND	IOB	P14C	P14A	P14D	P13B	P12C
14	P19D	P18A	P17B												P13A	P13D	P11A
13	P19B	P19A	P19C												P12B	P12D	P11C
12	P20D	P20C	P20A												P11D	P11B	P10A
11	P20B	P21A	P21C												P10B	P10D	P10C
10	P21D	P22C	P22A					(BOTTOM VIEW)							P9D	P9B	P9A
9	P21B	P22D	GND												GND	P9C	P8A
8	P22B	P23C	VAA												VAA	P8B	P8C
7	P23D	P23A	P24C												P7B	P8D	P7A
6	P23B	P25C	P24A												P7D	P6B	P7C
5	P24D	P25A	P26C												P5B	P6D	P6A
4	P24B	P26A	P26B											P4D	P4C	P5D	P6C
3	P25D	P27C	P27A	WT0B	P27B	WT2D	WT2C	WT3C	CLK*	LD*	P0B	P1A	P3C	P3B	P3A	P4B	P5A
2	P25B	WT0D	WT1D	WT1B	WT2B	WT3D	WT3B	VAA	CLK	GND	GND	P0A	P1C	P2C	P2A	P3D	P5C
1	P26D	P27D	WT0C	WT0A	WT1C	WT1A	WT2A	WT3A	BLK*	SYNC*	P0D	P0C	P1D	P1B	P2D	P2B	P4A

PC Board Layout Considerations

PC Board Considerations

The Bt463 layout should be optimized for lowest noise on the Bt463 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt463 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 11.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 12 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt463 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

PC Board Layout Considerations *(continued)*

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt463 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt463 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 12 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

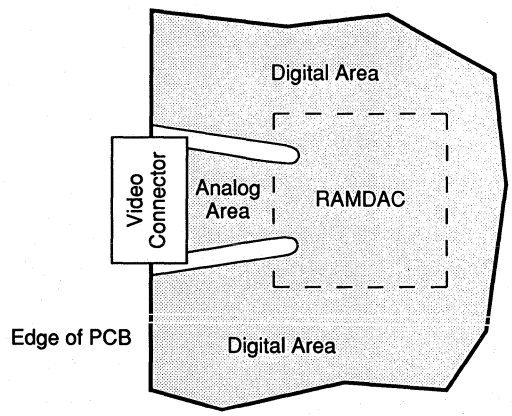
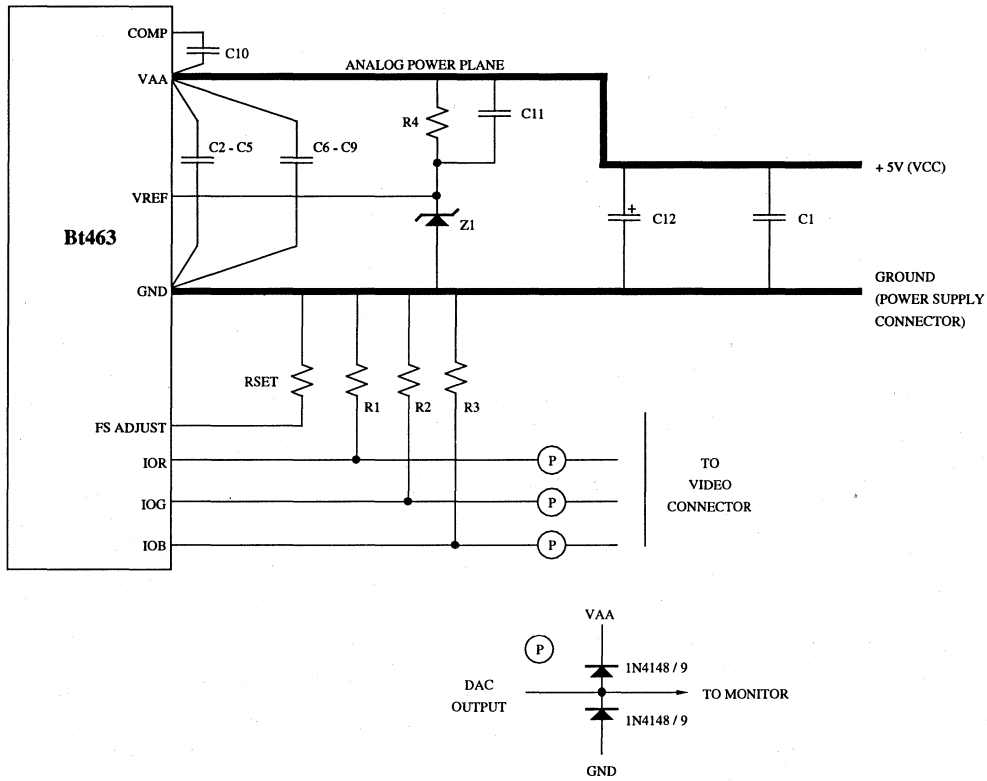


Figure 11. Sample Layout Showing Power and Ground Plane Isolation Gaps.

PC Board Layout Considerations *(continued)*



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors. EMI may be compromised with ferrite bead in circuit.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt463.

Figure 12. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt463 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt463 will not function if a single-ended clock is used with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by 2 or 4 (depending on whether 2:1 or 4:1 multiplexing was specified) and translating the result to TTL levels. As LD* may be phase shifted relative to CLOCK, propagation delays need not be a concern when the LD* signal is derived. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC* and BLANK*).

For display applications in which a single Bt463 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 input multiplexing of the Bt463 and will also set the pipeline delay of the Bt463 to 13 clock cycles. The Bt438 may also be used to interface the Bt463 to a TTL clock. Figure 13 illustrates use of the Bt438 with the Bt463.

Setting the Pipeline Delay

The pipeline delay of the Bt463, although fixed after a power-up condition, may be anywhere from 11–15 clock cycles. The Bt463 contains additional circuitry enabling the pipeline delay to be fixed at 13 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt463.

To reset the Bt463, it should be powered up, with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for at least three rising edges of LD*. The device can be held with CLOCK and CLOCK* stopped for an unlimited time.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

When the Bt463 is reset to a 13-clock-cycle pipeline delay, the blink counter circuitry is not reset. Therefore, if multiple Bt463s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00, and the overlay blink enable bits should be logical zeros. Software may control blinking through the read mask register and overlay display enable bits.

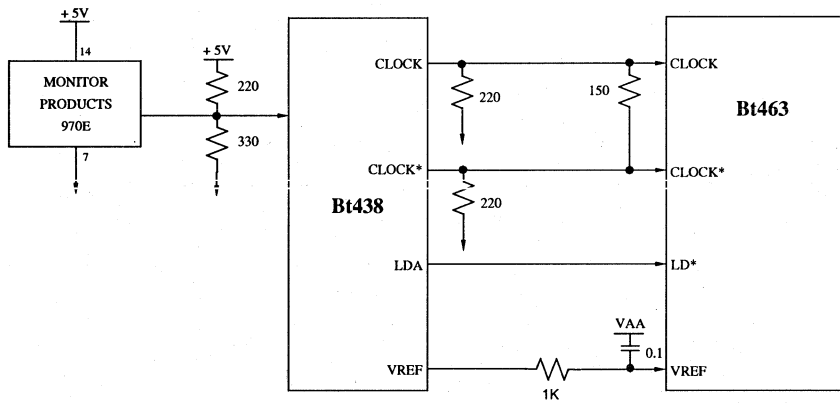


Figure 13. Generating the Bt463 Clock Signals.

Application Information *(continued)*

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt463

The Bt463 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating use of these test features.

Signature Registers (Signature Mode)

The input signature register is 16 bits wide, capturing pixel information prior to the lookup tables. Since the pixel path is 28 bits wide, the lower or upper 16 bits are selected for capture by command bit CR22. The input signature analysis register (SAR) is operational at frequencies <120 MHz

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color and are presented as inputs simultaneously to the red, green, and blue SARs, as well as to the three on-chip DACs.

The SARs act as a 16-bit- or 24-bit-wide linear feedback shift register on each succeeding pixel that is latched. In either the 2:1 or 4:1 multiplexed mode, the SARs latch only 1 pixel per load group. Thus, the SARs are operating on only every second or fourth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, or D) is latched to generate new signatures by setting bits D0–D2 in the test register.

In 1:1 mux mode, the SARs will generate signatures on each succeeding pixel in the input stream. In this case, the user should select pixel "A" (test register D0, D1, and D2 = 000) when the Bt463 is in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt463 will generate signatures only while it is in "active-display" (BLANK* negated). The SARs are available for reading and writing through the MPU port when the Bt463 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 16-bit or 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan line or one frame buffer of pixels, will be input to the chip. At the succeeding blank state, the resultant 16-bit or 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested with the signature registers.

Assuming the chip is running 2:1 or 4:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, or D—selected. The linear feedback configurations are shown in Figures 14 and 15.

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can by used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Signature Registers (Data-Strobe Mode)

When command bit CR20 is set to a logical one, the SARs are put in data-strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the generation of signatures by the SARs. Instead, the SARs capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt463. The levels of most inputs are insignificant except that CLOCK should be high and CLOCK* should be low. Then, the user may read the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively. Likewise, the input SAR may be read with two MPU reads.

Application Information *(continued)*

In general, the color readout will correspond to a pixel latched on the previous load. However, because the data path is pipelined, the color may come from an earlier load cycle. To read successive pixels, LD* should be toggled, the CLOCK pins should be pulsed according to the mux state (one, two, or four periods), and all pixel-related inputs should be held and the three MPU reads performed as described. This process is best done on a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt463 is the analog comparator. It allows the user to measure the DACs against each other as well as against a specific reference voltage.

Four combinations of tests are selected through the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register. The capture occurs over one LD* period set by a logical one at pixel port P16 (A–D).

Because the comparator's design is simple, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. The color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

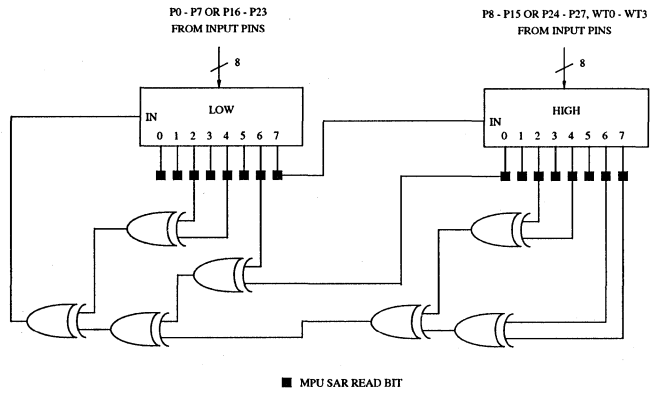


Figure 14. Input Signature Analysis Register Circuit.

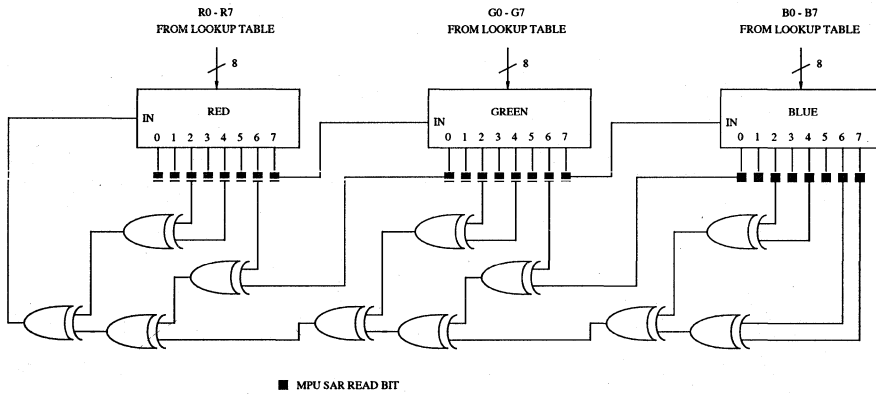


Figure 15. Output Signature Analysis Register Circuit.

Application Information *(continued)*

Initializing the Bt463

Following a power-on sequence, the Bt463 must be initialized. This sequence will configure the Bt463 as follows:

4:1 multiplexed operation
4 overlay planes on P<27:23>
sync enabled on IOG, 7.5 IRE blanking pedestal
no cursor interface
24-plane true color
start address at $0001
16 window entries

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $00 to command register 1	10
Write $C0 to command register 2	10
Write $00 to reserved location	10
Write $FF to pixel read mask register P0- P7	10
Write $FF to pixel read mask register P8- P15	10
Write $FF to pixel read mask register P16- P23	10
Write $FF to pixel read mask register P24- P27	10
Write $00 to pixel blink mask register P0- P7	10
Write $00 to pixel blink mask register P8-P15	10
Write $00 to pixel blink mask register P16- P23	10
Write $00 to pixel blink mask register P24- P27	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $00 to B0-B7 register (location $0)	10
Write $E1 to B8-B15 register (location $0)	10
Write $03 to B16-B23 register (location $0)	10
Write $00 to B0-B7 register (location $1)	10
Write $E1 to B8-B15 register (location $1)	10
Write $03 to B16-B23 register (location $1)	10
:	:
Write $00 to B0-B7 register (location $F)	10
Write $E1 to B8-B15 register (location $F)	10
Write $03 to B16-B23 register (location $F)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $20F)	11
Write green data to RAM (location $20F)	11
Write blue data to RAM (location $20F)	11

Cursor Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2) (Note 1)	10
Write green data to cursor (location $2) (Note 1)	10
Write blue data to cursor (location $2) (Note 1)	10
Write red data to cursor (location $3) (Note 1)	10
Write green data to cursor (location $3) (Note 1)	10
Write blue data to cursor (location $3) (Note 1)	10

5

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short-Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
PGA	TJ			+170	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (Each DAC)		8	8	8	Bits
Accuracy (Each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			80	µA
Input Low Current (Vin = 0.4 V)	IIL			–80	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	15	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	0.6		6	V
Input High Current (Vin = 4.0V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0V)	CKIN		4	15	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = 400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		90		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

All JTAG DC parameters are tested to a minimum VAA = 5.0 V with VIL on JTAG pins at 0.6 V maximum.

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	Units
Clock Rate	Fmax	max	135	110	MHz
LD* Rate	LDmax				
1:1 multiplexing		max	67.5	55	MHz
2:1 multiplexing		max	67.5	55	MHz
4:1 multiplexing		max	33.75	27.5	MHz
R/W, C0, C1 Setup Time	1	min	0	0	ns
R/W, C0, C1 Hold Time	2	min	15	15	ns
CE* Low Time	3	min	50	50	ns
CE* High Time	4	min	25	25	ns
CE* Asserted to Data Bus Driven	5	min	7	7	ns
CE* Asserted to Data Valid	6	max	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	20	20	ns
Write Data Setup Time	8	min	35	35	ns
Write Data Hold Time	9	min	3	3	ns
TMS, TDI Setup Time	10	min	8	8	ns
TMS, TDI Hold Time	11	min	6	6	ns
TCK Low Time	12	min	10	10	ns
TCK High Time	13	min	10	10	ns
TCK Asserted to TDO Driven	14	min	5	5	ns
TCK Asserted to TDO Valid	15	max	20	20	ns
TCK Negated to TDO 3-Stated	16	max	20	20	ns
Pixel and Control Setup Time	17	min	3	3	ns
Pixel and Control Hold Time	18	min	2	2	ns
Clock Cycle Time	19	min	7.4	9.09	ns
Clock Pulse Width High Time	20	min	3.2	4	ns
Clock Pulse Width Low Time	21	min	3.2	4	ns
LD* Cycle Time	22				
1:1 multiplexing		min	14.81	18.18	ns
2:1 multiplexing		min	14.81	18.18	ns
4:1 multiplexing		min	29.63	36.36	ns
LD* Pulse Width High Time	23				
1:1 multiplexing		min	6	7	ns
2:1 multiplexing		min	6	8	ns
4:1 multiplexing		min	12	15	ns
LD* Pulse Width Low Time	24				
1:1 multiplexing		min	6	7	ns
2:1 multiplexing		min	6	8	ns
4:1 multiplexing		min	12	15	ns

See test conditions on next page.

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AC Characteristics *(continued)*

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	Units
Analog Output Delay	25	typ	35	35	ns
Analog Output Rise/Fall Time	26	typ	1.5	1.5	ns
Analog Output Settling Time	27	max	8	8	ns
Clock and Data Feedthrough (Note 1)		typ	tbd	tbd	dB
Glitch Impulse (Note 1)		typ	50	50	pV - sec
DAC-to-DAC Crosstalk		typ	tbd	tbd	dB
Analog Output Skew		typ	0	0	ns
		max	2	2	ns
Pipeline Delay		min	11	11	Clocks
		max	15	15	Clocks
VAA Supply Current (Note 2)	IAA	typ	500	450	mA
		max	tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF, and D0–D7 output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

All JTAG AC parameters are tested to a minimum VAA = 5.0 V with VIL on JTAG pins at 0.6 V maximum.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V, and TA = 20° C. IAA (max) at VAA = 5.25 V, and TA = 0° C.

See timing waveforms and notes in Figures 16–18.

Timing Waveforms

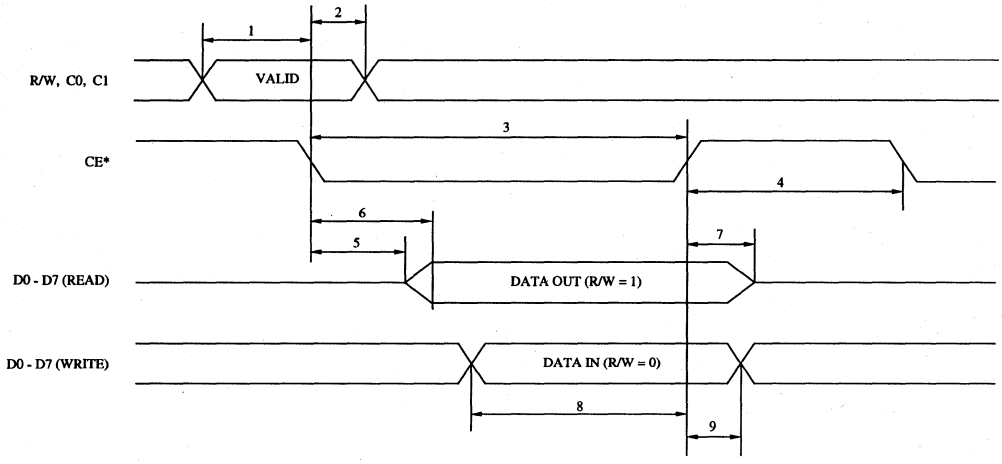
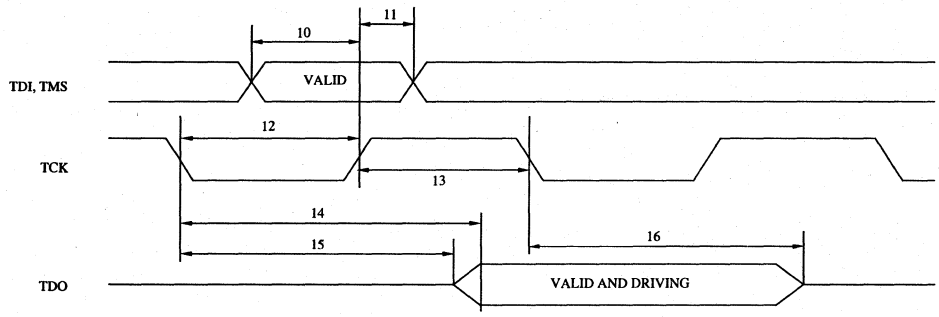
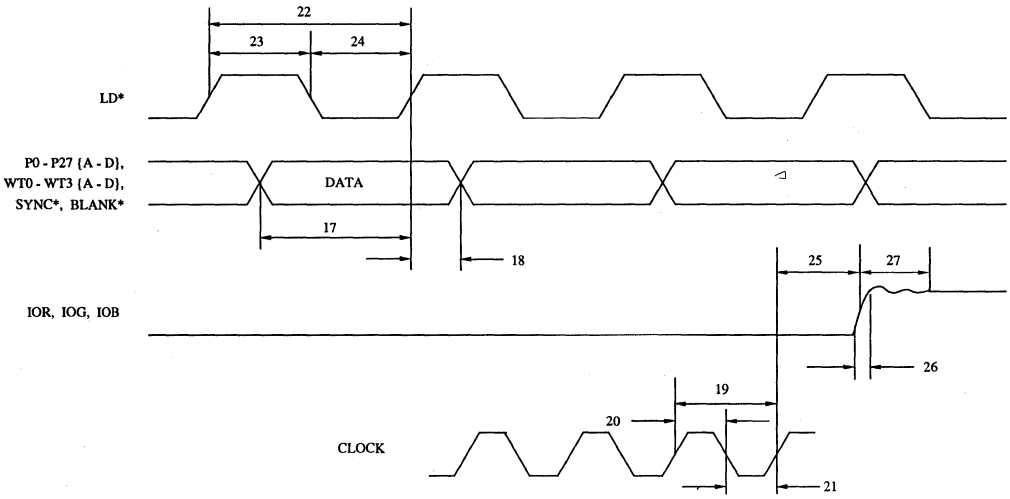


Figure 16. MPU Read/Write Timing Dimensions.



Note 1: TMS and TDI are sampled on the rising edge of TCK.
Note 2: TDO changes after the falling edge of TCK.

Figure 17. JTAG Timing.



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 18. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt463KG135	135 MHz	169-pin Ceramic PGA	0° to +70° C
Bt463KG110	110 MHz	169-pin Ceramic PGA	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice. Please consult Brooktree regarding the most updated datasheet before design.

Bt467

230 MHz
Monolithic CMOS
256-Color Palette
RAMDAC™

Distinguishing Features

- 230, 170, 135 MHz Operation
- 8:1 Multiplexed TTL Pixel Ports
- Register Compatibility with Bt458
- 256-Word Dual-Port Color Palette
- 4-Word Dual-Port Overlay Palette
- RS-343A-Compatible Outputs
- Bit Plane Read and Blink Masks
- Programmable Offset
- Standard MPU Interface
- 145-pin PGA Package
- +5 V CMOS Monolithic Construction

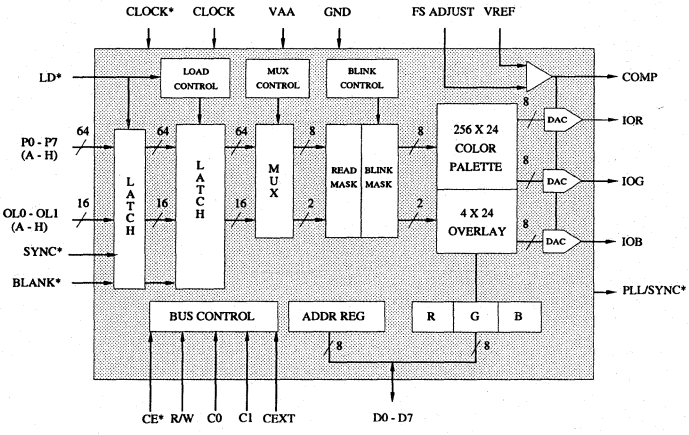
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439, Bt458

Functional Block Diagram



Product Description

The Bt467 is designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1600 x 1280 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information). This minimizes the requirements for costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The 8:1 multiple pixel ports and internal multiplexing enable TTL-compatible interface (up to 29 MHz) to the frame buffer, while maintaining the 230-MHz video data rates required for 76 Hz systems.

The Bt467 contains a 256 x 24 color lookup table with triple 8-bit video D/A converters. The Bt467 is also register-compatible with the Bt458, providing Bt458 software/device driver compatibility. In addition, extended registers are optional, providing such features as testability enhancements, sync output, and pedestal option. The Bt467 has 0 IRE setup with no composite sync on the green channel. An output is provided for either separate sync or PLL for synchronization.

On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt467 generates RS-343A-compatible red, green, and blue and can drive doubly-terminated 75 Ω coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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L467001 Rev. A

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt467 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay RAM allow color updating without contention with the display refresh process.

As shown in Table 1, the C0, C1, and CEXT control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay RAM will be accessed by the MPU. CEXT is used to specify Bt458 register compatibility or access to the extended register set.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Bt467 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay RAM to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay RAM to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay RAM. Following the blue read cycle, the address register increments to the next location, which the MPU may read by reading another sequence of red, green, and blue data.

ADDR0–7	CEXT	C1	C0	Addressed by MPU
$xx	X	0	0	address register
$00–$FF	X	0	1	color palette RAM
$00	X	1	1	overlay color 0
$01	X	1	1	overlay color 1
$02	X	1	1	overlay color 2
$03	X	1	1	overlay color 3
$00	X	1	0	ID Register ($80)
$01	X	1	0	Revision Register
$02	X	1	0	reserved ($00)
$03	X	1	0	reserved ($00)
$04	X	1	0	read mask register
$05	X	1	0	blink mask register
$06	X	1	0	command register
$07	X	1	0	test register
$08	1	1	0	command register 1
$09	1	1	0	command register 2
$0A	1	1	0	reserved ($00)
$0B	1	1	0	test register 1
$0C	1	1	0	red signature
$0D	1	1	0	green signature
$0E	1	1	0	blue signature
$0F	1	1	0	reserved ($00)

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay Register 3. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. In the Bt458 register-compatibility mode, the MPU does not have access to these bits. However, in the extended register mode, the modulus three is accessible as read-only register bits through Command Register 1. This provides the state of these 2 bits after the last color was loaded. These 2 bits provide the state of the read/write cycle after the last color is loaded.

Additional Information

Although the color palette RAM and overlay registers are dual ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU during the write cycle, 1 or more of the pixels on the display screen may be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers can also be accessed through the address register in conjunction with the C0, C1, and CEXT inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU. Figure 1 illustrates the MPU read/write timing of the Bt467.

5

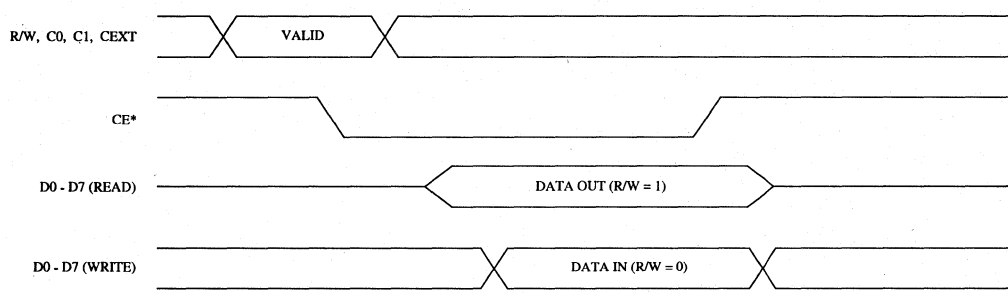


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable the transfer of pixel data from the frame buffer at TTL data rates, the Bt467 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color information (up to 8 bits per pixel), and overlay information (up to 2 bits per pixel), for 8 consecutive pixels, are latched into the device. With this configuration, the sync and blank timing will be recognized only with 8-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

At each clock cycle, the Bt467 outputs color information based on the {A} inputs, followed by the {B} inputs, followed by the {C} inputs, etc., until all 8 pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis. Or, they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK.

This enables the LD* signal to be derived by externally dividing CLOCK by eight, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than eight clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

Only one rising edge of LD* should occur every eight clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

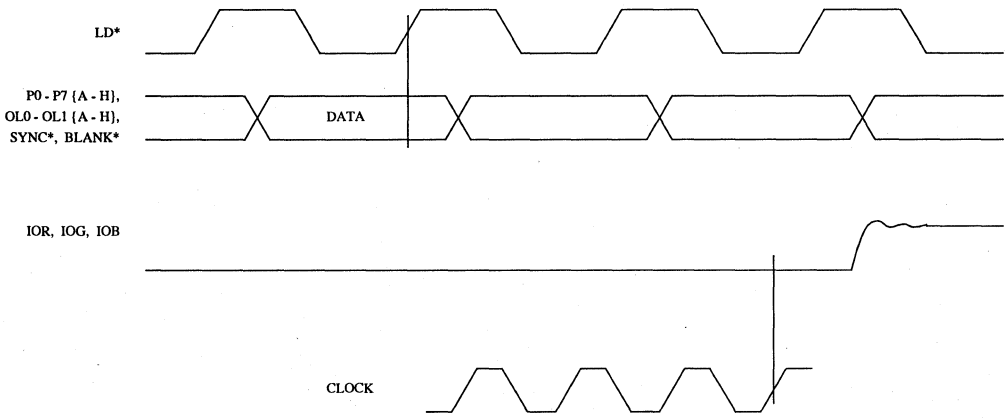


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

At each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. These registers are not initialized. They must be initialized by the user after power up for proper operation. Through the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change caused by blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt467 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval occurs when BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAM. Table 2 is the truth table used for color selection.

Video Generation

At every clock cycle, the selected color information from the color palette RAMs or overlay registers is presented to the D/A converters.

The BLANK* input, pipelined to maintain synchronization with the pixel data, adds an appropriately-weighted current to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Tables 3–6 detail how the BLANK* input modifies the output levels.

The D/A converters on the Bt467 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

The Bt467 does not have a sync current source on the green channel (IOG) as does the Bt458. However, to generate a sync on green (IOG), the PLL/sync signal can be programmed to generate sync current. Sync on green can be generated by tying the IOG and PLL/Sync output signals together. This combination will supply the appropriate sync current (see Figures 5 and 6). This output signal combination should be properly terminated to ground through a 75 Ω resistor.

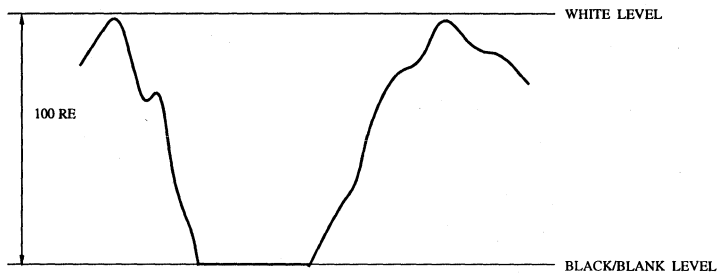
5

CR06	OL1	OL0	P0–P7	Addressed by frame
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

IOR, IOG, IOB	
MA	V
19.05	0.714
0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Figure 3. Composite Video Output Waveform (SETUP = 0 IRE).

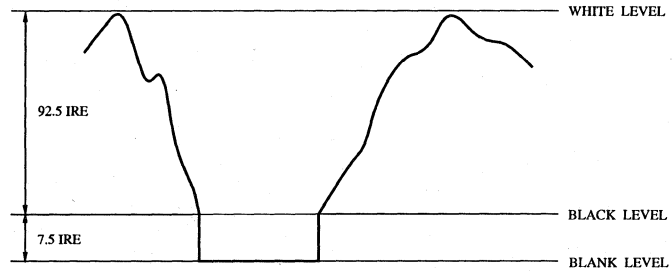
Description	IOR, IOG, IOB (mA)	BLANK*	DAC Input Data
WHITE	19.05	1	$FF
DATA	data	1	data
BLACK	0	1	$00
BLANK	0	0	$xx

Note: Typical with full-scale IOG = 19.05 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Table 3. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

IOR, IOG, IOB	
MA	V
19.05	0.714
1.44	0.054
0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Figure 4. Composite Video Output Waveform (SETUP = 7.5 IRE).

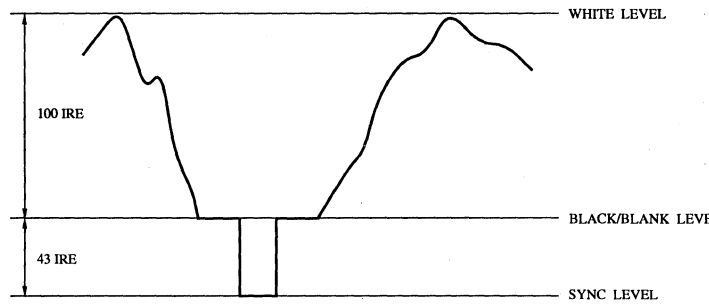
Description	IOR, IOG, IOB (mA)	BLANK*	DAC Input Data
WHITE	19.05	1	$FF
DATA	data + 1.44	1	data
BLACK	1.44	1	$00
BLANK	0	0	$xx

Note: Typical with full-scale IOG = 19.05 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 5. Composite Video Output Waveform (SETUP = 0 IRE) PLL/SYNC Externally Tied To IOG.

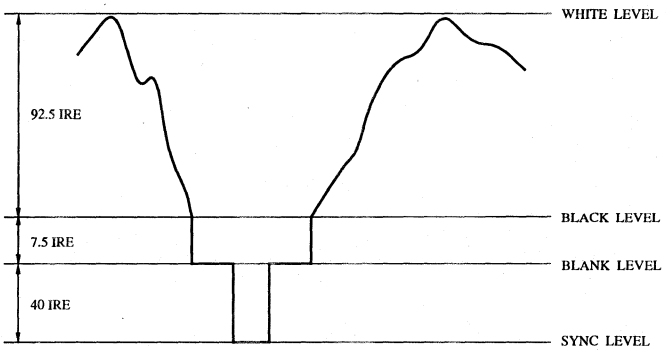
Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. RS-343A levels and tolerances are assumed on all levels.

Figure 6. Composite Video Output Waveform (SETUP = 7.5 IRE) PLL/SYNC Externally Tied To IOG.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. This register is not initialized. It must be initialized by the user after power up for proper operation. CR0 corresponds to data bus bit D0.

CR07 Multiplex select

(0) 8:1 multiplexing
(1) 8:1 multiplexing

It is only possible to set the pipeline delay of the Bt467 to a fixed 8-clock cycle.

CR06 RAM enable

(0) use overlay color 0
(1) use color palette RAM

When the overlay display bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.

CR05, CR04 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).

CR03 OL1 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL1 {A–H} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the values of the OL1 {A–H} inputs. In order for overlay 1 bit plane to blink, bit CR01 must be set to a logical one.

CR02 OL0 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL0 {A–H} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the values of the OL0 {A–H} inputs. In order for overlay 0 bit plane to blink, bit CR00 must be set to a logical one.

CR01 OL1 display enable

(0) disable
(1) enable

If a logical zero, this bit forces the OL1 {A–H} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the values of the OL1 {A–H} inputs.

CR00 OL0 display enable

(0) disable
(1) enable

If a logical zero, this bit forces the OL0 {A–H} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the values of the OL0 {A–H} inputs.

Internal Registers (continued)

Command Register 1

The command register may be written to or read by the MPU at any time and is not initialized. This register is not initialized. It must be initialized by the user after power up for proper operation. CR10 corresponds to data bus bit D0.

CR17, CR16	Address counters (0,0) red (0,1) green (1,0) blue (1,1) undefined	This is a read-only register bit that specifies the location of the modulus a,b addresses. This is useful to determine the last location written to during the load of the palette RAM. These bits are read only.
CR15	reserved (logical zero)	
CR14	reserved (logical zero)	
CR13	reserved (logical zero)	
CR12	reserved (logical zero)	
CR11	reserved (logical zero)	
CR10	reserved (logical zero)	

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Internal Registers (continued)

Command Register 2

The command register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power up for proper operation. CR20 corresponds to data bus bit D0.

CR27 reserved (logical zero)

CR26 Pedestal enable

(0) 0 IRE pedestal
(1) 7.5 IRE pedestal

This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.

CR25, CR24 Load palette RAM select

(00) normal
(01) red RAMDAC
(10) green RAMDAC
(11) blue RAMDAC

If (00) is specified, color data is loaded into the Bt467 using three write cycles (red, green, and blue). Color data is output using three read cycles (red, green, and blue).

Modes (01), (10), and (11) enable the Bt467 to emulate a single-channel RAMDAC using only the green channel. The Bt467 expects color data to be input and output using (red, green, blue) cycles. The exact value indicates during which one of the three color cycles the Bt467 is to load or output color information. The value is loaded into or read from the green color palette RAM.

CR23 PLL generate

(0) SYNC*
(1) BLANK*

This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.

CR22 PLL/SYNC

(0) disable
(1) enable

If (0) is specified, the PLL/SYNC output is disabled. If (1) is specified, the PLL/SYNC output is enabled, and CR21 should be used to select PLL or SYNC.

CR21 PLL/SYNC select

(0) PLL
(1) SYNC

If (0) is specified, PLL/SYNC outputs PLL current. CR23 should be used to select SYNC or BLANK to generate the PLL information. If (1) is specified, PLL/SYNC outputs SYNC current.

CR20 Test mode select

(0) signature analysis test
(1) data strobe test

This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–H}), and D7 correspond to bit plane 7 (P7 {A–H}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power up for proper operation.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A–H}), and D7 corresponds to bit plane 7 (P7 {A–H}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power up for proper operation.

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt467, the value read by the MPU will be $80. Data written to this register is ignored. If this location is read from the Bt458, the value returned will be $00.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt467. If this location is read from the Bt458, the value returned will be $01. The 4 most significant bits signify the revision letter in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored. For the Bt467, the value read by the MPU will be $B2.

Reserved Register ($02 and $03)

These registers are not identically compatible with the Bt458. For the Bt467, if these registers are read, they will return a value of ($00) to the data bus. For the Bt458, if these same locations are read, the data present on the data bus will be returned.

Internal Registers (continued)

Bt467 Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	Color Information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting *only one* of the (red, green, blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the (red, green, blue, low, or high nibble) enable information previously written. Either the CLOCK must be slowed to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits and D0–D3 containing (red, green, blue, low, or high nibble) enable information, as listed below.

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Internal Registers (continued)

Signature Registers (Signature Mode)

In the active mode, the signature register operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs.

The SARs act as a 24-bit-wide linear feedback shift register on each succeeding pixel that is latched. *In 8:1 multiplexed mode, the SARs only latch 1 pixel per load group.* Thus, the SARs are operating only on every eighth pixel in the multiplexed mode. The user determines which pixel phase (A, B, C, D, E, F, G, or H) is latched to generate new signatures by setting bits D0–D2 in Test Register 1.

The Bt467 will generate signatures only while it is in "active-display" (BLANK* negated). The SARs are available for reading and writing by the MPU port when the Bt467 is in a blanking state (BLANK* asserted). It is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan-line or one frame buffer's worth of pixels, will be input to the chip. Then, at the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay data validity is also tested with the signature registers.

The Bt467 linear feedback configuration is shown in Figure 7.

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Signature Registers (Data-Strobe Mode)

Setting command bit CR20 to a logic one puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt467. The levels of most inputs do not matter *except* that CLOCK should be high and CLOCK* should be low. Then, the user can read the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

In general, the color read-out will correspond to a pixel latched on the previous load. However, because the data path is pipelined, the color may come from an earlier load cycle. To read successive pixels, LD* should be toggled, the CLOCK pins should be pulsed according to the mux state, and all pixel-related inputs should then be held and the three MPU reads should be performed as described. This process is best done on a sophisticated VLSI semiconductor tester.

Internal Registers (continued)

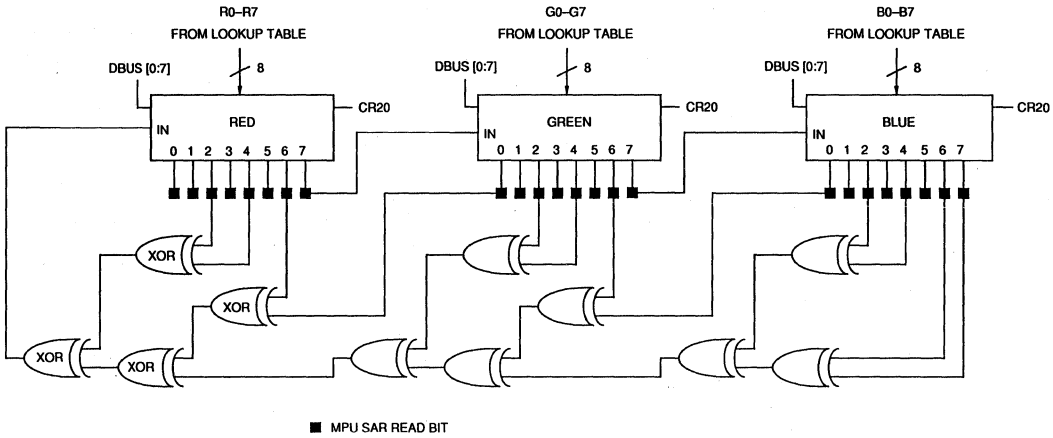


Figure 7. Signature Analysis Register Circuit.

Internal Registers (continued)

Test Register 1

This 8-bit register is used to test the Bt467. Signature analysis is performed on every eighth pixel. D0–D2 are used for 8:1 multiplexing to specify whether the A, B, C, D, E, F, G, or H pixel inputs are to be used, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	pixel F
110	pixel G
111	pixel H

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	–	–
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The output levels of the DACs should be constant for 5 µS to allow enough time for detection. The capture occurs over one LD* period set by a logical one at any of the pixel pins.

For normal operation, D3–D7 must be logical zeros.

Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>BLANK*</td><td>Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.</td></tr>
<tr><td>SYNC*</td><td>Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the PLL/SYNC output (see Figures 5 and 6). SYNC* does not override any other control or data input, as shown in Tables 5 and 6; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.</td></tr>
<tr><td>LD*</td><td>Load control input (TTL compatible). The P0–P7 {A–H}, OL0–OL1 {A–H}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD* may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.</td></tr>
<tr><td>P0–P7
{A–H}</td><td>Pixel select inputs (TTL compatible). These inputs are used to specify on a pixel basis which one of the 256 entries in the color palette RAM is to be used to provide color information. Eight consecutive pixels are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.

The {A} pixel is output first, followed by the {B} pixel, followed by the {C} pixel, etc., until all 8 pixels have been output, at which point the cycle repeats.</td></tr>
<tr><td>OL0–OL1
{A–H}</td><td>Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD* and, in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:
<table>
<tr><th>OL1</th><th>OL0</th><th>CR06 = 1</th><th>CR06 = 0</th></tr>
<tr><td>0</td><td>0</td><td>color palette RAM</td><td>overlay color 0</td></tr>
<tr><td>0</td><td>1</td><td>overlay color 1</td><td>overlay color 1</td></tr>
<tr><td>1</td><td>0</td><td>overlay color 2</td><td>overlay color 2</td></tr>
<tr><td>1</td><td>1</td><td>overlay color 3</td><td>overlay color 3</td></tr>
</table>
When accessing the overlay palette, the P0–P7 {A–H} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for 8 consecutive pixels are input through this port. Unused inputs should be connected to GND.</td></tr>
<tr><td>IOR, IOG, IOB</td><td>Red, green, and blue video current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figure 5).</td></tr>
<tr><td>PLL/SYNC*</td><td>Phase lock loop current output. This high-impedance current source is used to enable synchronization of multiple Bt467s with subpixel resolution when used with an external PLL. This function is accessible through the extended command registers. A logical one on the BLANK* input results in no current output onto this pin, while a logical zero results in the following current output:

PLL (mA) = 3,227 * VREF (V) / RSET (Ω)

If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor of up to 150 Ω). The Bt467 does not have a SYNC current source on the green channel (IOG) as does the Bt458. However, to generate a SYNC on green (IOG), the PLL/SYNC signal can be programmed to generate SYNC current. SYNC can be generated by tying the IOG and PLL/SYNC output signals together. This combination will supply the appropriate SYNC current (see Figures 5 and 6). This output signal combination should be properly terminated to ground through a 75 Ω resistor.</td></tr>
</table>

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (see Figure 8 in the PC Board Layout Considerations section). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and to maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to PC board layout considerations for critical layout criteria.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (see Figure 8). The IRE relationships in Figures 3–6 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = 10,684* VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOG, IOB, (mA) = 7,457* VREF (V) / RSET (Ω)
VREF	Voltage reference input. An external voltage reference circuit must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum (see Figure 8.)
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1, CEXT	Command control inputs (TTL compatible). C0, C1, and CEXT specify the type of read or write operation being performed, as shown in Table 1. CEXT provides the control input for Bt458 register compatibility or access to the extended register set. These Inputs are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	K1	P5A	K15	D0	B9
SYNC*	J2	P5B	J15	D1	B8
LD*	K3	P5C	K13	D2	A10
CLOCK	J1	P5D	K14	D3	A9
CLOCK*	K2	P5E	L14	D4	C10
		P5F	L15	D5	B10
P0A	P1	P5G	M15	D6	B11
P0B	P2	P5H	L13	D7	A11
P0C	N2				
P0D	N1	P6A	D15	VAA	C3
P0E	M1	P6B	E15	VAA	C7
P0F	L3	P6C	F15	VAA	C8
P0G	L2	P6D	F14	VAA	C13
P0H	M2	P6E	G14	VAA	D4
		P6F	G15	VAA	G13
P1A	R4	P6G	J14	VAA	H3
P1B	N5	P6H	H15	VAA	H13
P1C	N4			VAA	J3
P1D	P4	P7A	B15	VAA	N3
P1E	R2	P7B	B14	VAA	N13
P1F	R3	P7C	C14		
P1G	P3	P7D	C15	GND	A5
P1H	R1	P7E	E14	GND	A7
		P7F	E13	GND	C4
P2A	P7	P7G	F13	GND	C9
P2B	R7	P7H	D14	GND	D13
P2C	R6			GND	G3
P2D	N7	OL0A	D1	GND	H2
P2E	N6	OL0B	E3	GND	H14
P2F	P6	OL0C	D3	GND	J13
P2G	P5	OL0D	D2	GND	M3
P2H	R5	OL0E	B1	GND	N12
		OL0F	C1		
P3A	R10	OL0G	C2	reserved	A2
P3B	P10	OL0H	A1	reserved	L1
P3C	P9			reserved	A12
P3D	N9	OL1A	G2	reserved	C12
P3E	R8	OL1B	H1	reserved	A14
P3F	R9	OL1C	F1	reserved	B13
P3G	N8	OL1D	G1	reserved	C11
P3H	P8	OL1E	F3	reserved	B12
		OL1F	F2	reserved	A13
P4A	M13	OL1G	E2	reserved	A15
P4B	M14	OL1H	E1	reserved	P13
P4C	P15			reserved	R12
P4D	N15	IOR	A8	reserved	P11
P4E	N14	IOG	B7	reserved	N10
P4F	R15	IOB	A6	reserved	R13
P4G	R14	PLL/SYNC*	A4	reserved	P12
P4H	P14			reserved	N11
		CE*	B2	reserved	R11
COMP	C6	R/W	B3		
FS ADJUST	A3	C0	B5		
VREF	B6	C1	C5		
		CEXT	B4		

Pin Descriptions (continued)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	N/C	P7A	P7D	P6A	P6B	P6C	P6F	P6H	P5B	P5A	P5F	P5G	P4D	P4C	P4F
14	N/C	P7B	P7C	P7H	P7E	P6D	P6E	GND	P6G	P5D	P5E	P4B	P4E	P4H	P4G
13	N/C	N/C	VAA	GND	P7F	P7G	VAA	VAA	GND	P5C	P5H	P4A	VAA	N/C	N/C
12	N/C	N/C	N/C										GND	N/C	N/C
11	D7	D6	N/C										N/C	N/C	N/C
10	D2	D5	D4										N/C	P3B	P3A
9	D3	D0	GND										P3D	P3C	P3F
8	IOR	D1	VAA										P3G	P3H	P3E
7	GND	IOG	VAA										P2D	P2A	P2B
6	IOB	VREF	COMP										P2E	P2F	P2C
5	GND	C0	C1										P1B	P2G	P2H
4	PLL/ SYNC*	CEXT	GND	VAA									P1C	P1D	P1A
3	FS ADJ	R/W	VAA	OL0C	OL0B	OL1E	GND	VAA	VAA	LD*	P0F	GND	VAA	P1G	P1F
2	N/C	CE*	OL0G	OL0D	OL1G	OL1F	OL1A	GND	SYNC*	CLK*	P0G	P0H	P0C	P0B	P1E
1	OL0H	OL0E	OL0F	OL0A	OL1H	OL1C	OL1D	OL1B	CLK	BLK*	N/C	P0E	P0D	P0A	P1H

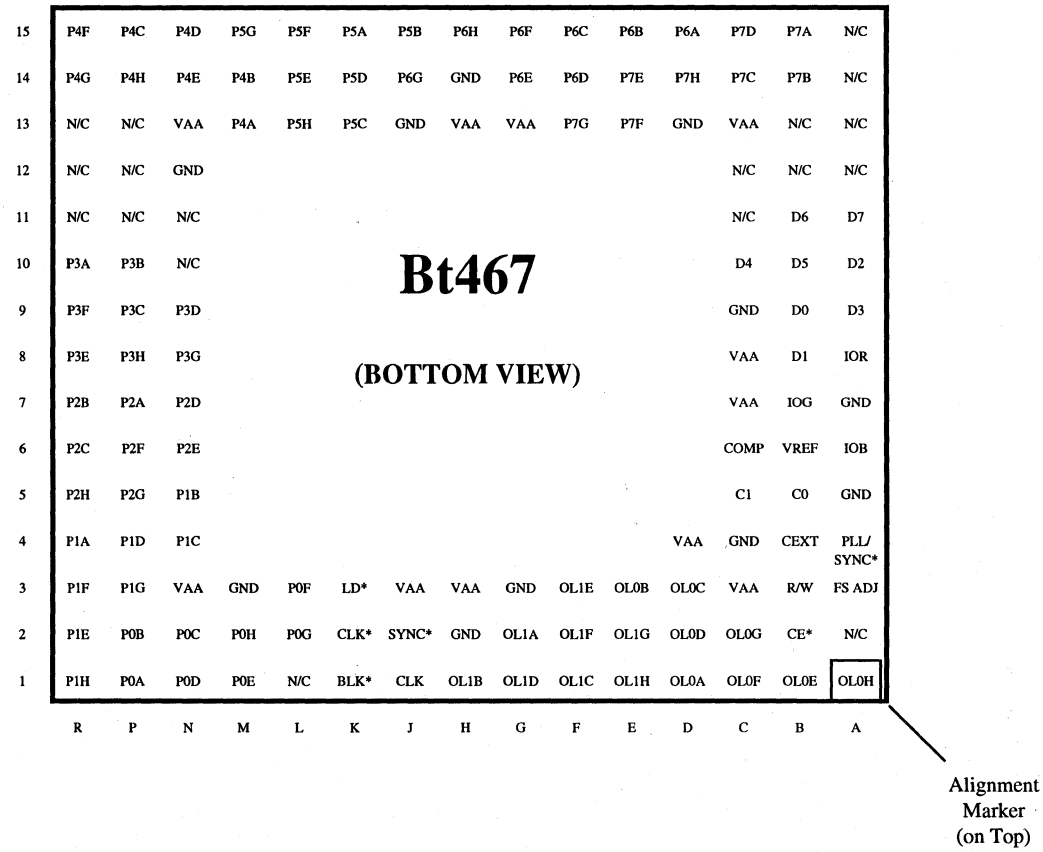
Bt467

(TOP VIEW)

Alignment Marker (on Top)

5

Pin Descriptions (continued)



	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
15	P4F	P4C	P4D	P5G	P5F	P5A	P5B	P6H	P6F	P6C	P6B	P6A	P7D	P7A	N/C
14	P4G	P4H	P4E	P4B	P5E	P5D	P6G	GND	P6E	P6D	P7E	P7H	P7C	P7B	N/C
13	N/C	N/C	VAA	P4A	P5H	P5C	GND	VAA	VAA	P7G	P7F	GND	VAA	N/C	N/C
12	N/C	N/C	GND										N/C	N/C	N/C
11	N/C	N/C	N/C										N/C	D6	D7
10	P3A	P3B	N/C										D4	D5	D2
9	P3F	P3C	P3D										GND	D0	D3
8	P3E	P3H	P3G										VAA	D1	IOR
7	P2B	P2A	P2D										VAA	IOG	GND
6	P2C	P2F	P2E										COMP	VREF	IOB
5	P2H	P2G	P1B										C1	C0	GND
4	P1A	P1D	P1C									VAA	GND	CEXT	PLL/ SYNC*
3	P1F	P1G	VAA	GND	P0F	LD*	VAA	VAA	GND	OL1E	OL0B	OL0C	VAA	R/W	FS ADJ
2	P1E	P0B	P0C	P0H	P0G	CLK*	SYNC*	GND	OL1A	OL1F	OL1G	OL0D	OL0G	CE*	N/C
1	P1H	P0A	P0D	P0E	N/C	BLK*	CLK	OL1B	OL1D	OL1C	OL1H	OL0A	OL0F	OL0E	OL0H

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt467, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16). This application note can be found in Brooktree's *Applications Handbook.*

The layout should be optimized for lowest noise on the Bt467 power and ground lplanes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Ccomponents should be placed as close as possible to the associated RAMDAC pin. Whenever possiple, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt467 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt467 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located within 3 inches of the Bt467. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 33 µF capacitor shown in Figure 8 is for low-frequency power supply ripple; the 0.1 µF and 0.01-µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

PC Board Layout Considerations (continued)

Digital Signal Interconnect

The digital inputs to the Bt467 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt467 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt467 to minimize reflections. Unused analog outputs should be connected to GND.

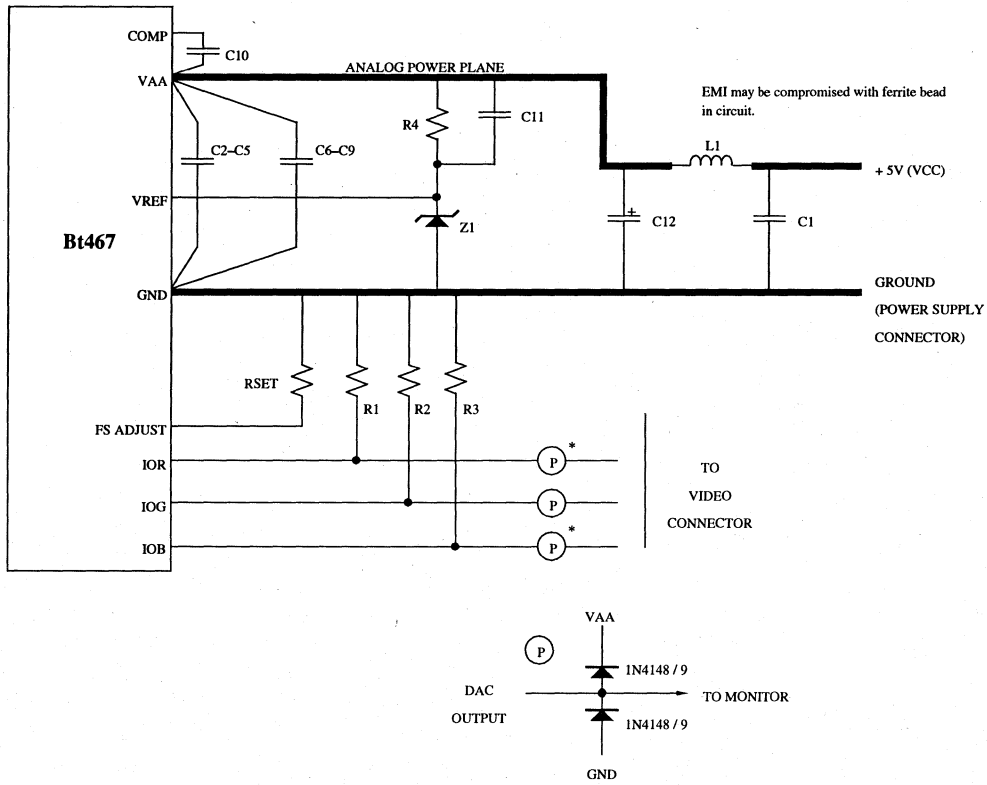
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt467 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 8 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111 *
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

* Or equivalent only.

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt467.

Figure 8. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt467 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 9.)

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt467 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by eight and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal only if fixed pipeline is not required. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt467 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt467, and will also optionally set the pipeline delay of the Bt467 to 8 clock cycles. The Bt438 may also be used to interface the Bt467 to a TTL clock. Figure 9 illustrates use of the Bt438 with the Bt467.

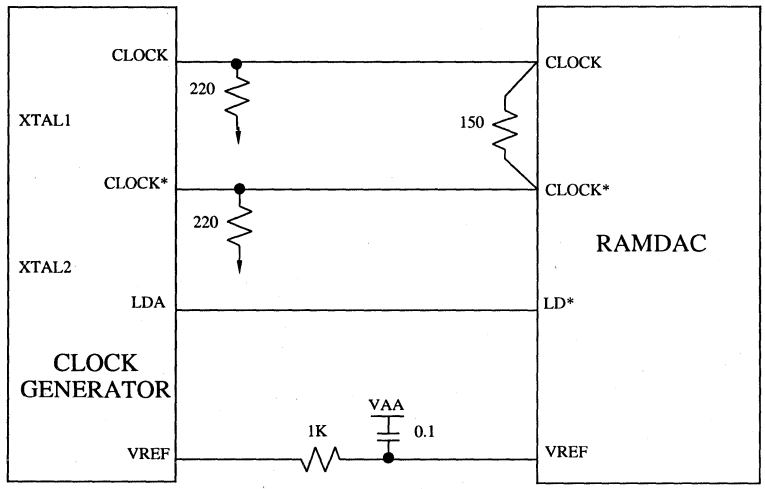


Figure 9. Generating the Bt467 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt467, although fixed after a power-up condition, may be anywhere from 6 to 13 clock cycles. The Bt467 contains additional circuitry enabling the pipeline delay to be fixed at 8 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt467.

To reset the Bt467, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

Resetting the Bt467 to an 8 clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt467s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask registers should be $00. Blinking may be done under software control via the read mask registers.

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Bt467 Color Display Applications

For color display applications when 1–4 Bt467s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt467, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt467 to eight clock cycles. The Bt439 may also be used to interface the Bt467 to a TTL clock. Figure 10 illustrates use of the Bt439 with the Bt467.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt467, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by 1–4 Bt467s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt467s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

If sub-pixel synchronization of multiple Bt467s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of 1–4 Bt467s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt467s must still have a 0.1 µF bypass capacitor to VAA.

Application Information (continued)

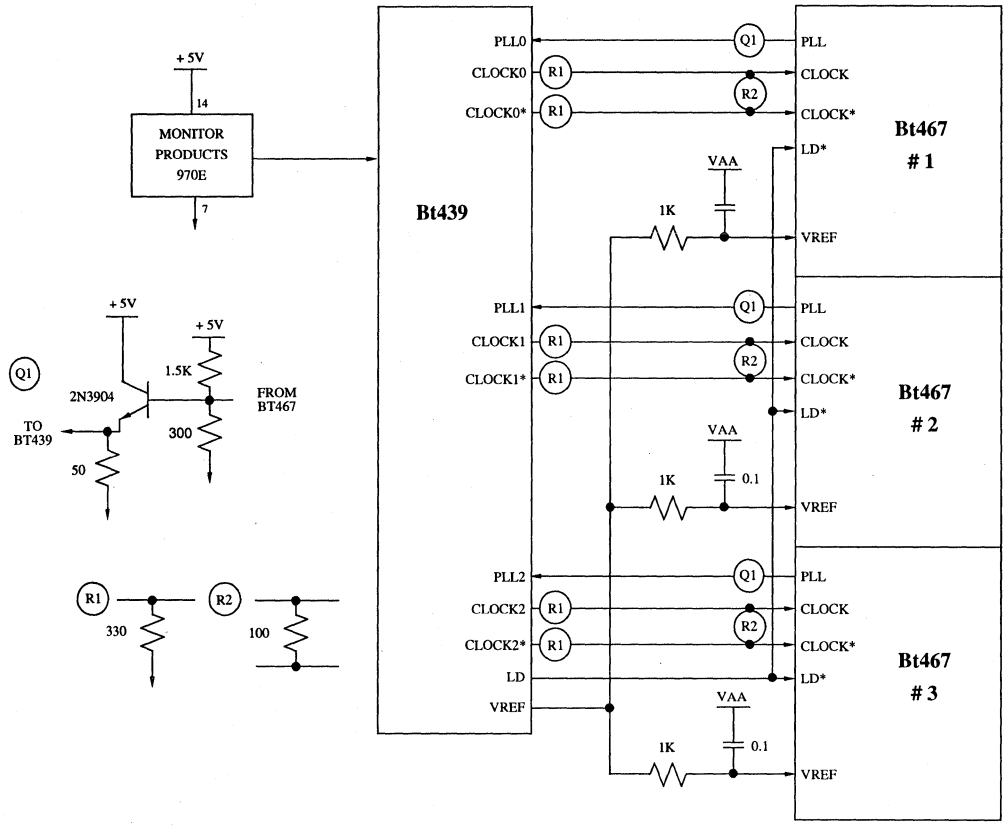


Figure 10. Generating the Bt467 Clock Signals (True-Color Application).

Application Information (continued)

Using Multiple Devices

When multiple RAMDACs are used, each RAMDAC should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each RAMDAC has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Bt467 Nonvideo Applications

The Bt467 may be used in nonvideo applications by disabling the video-specific control signals. BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}457 * VREF\ (V) / Iout\ (mA)$$

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 610 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

Initializing the Bt467 (Bt458 Register-Compatible Mode)

Following a power-on sequence, the Bt467 must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt467 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. CEXT is held low.

This sequence will configure the Bt467 as follows:

- 8:1 multiplexed operation
- 0 IRE pedestal
- no overlays
- no blinking
- sync output enabled

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10
Write $09 to address register	00
Write $06 to command register 2	10
Write $0B to address register	00
Write $00 to test register 1	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		487		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Clock Inputs	ΔVIN	.6			V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

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DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 0 IRE		0	5	50	µA
SETUP = 7.5 IRE		.95	1.44	1.90	mA
Blank Level on IOR, IOG, IOB		0	5	50	µA
LSB Size			75		µA
DAC-to-DAC Matching (Note 1)			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6	7.62	9	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–1.0		+2.5	V
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)			10		pF
Voltage Reference Input Current	IREF		10	100	µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 487 Ω and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

AC Characteristics

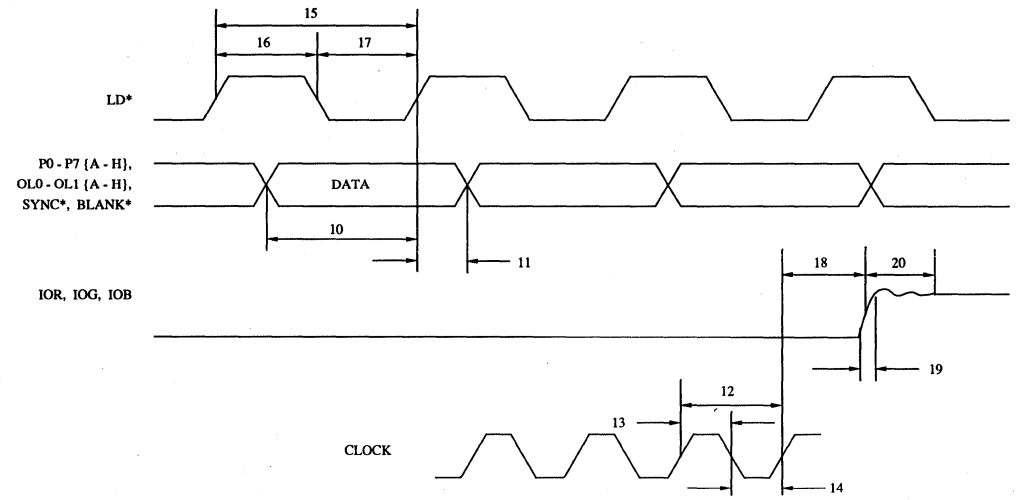
Parameter	Symbol	Min/Typ/ Max	230 MHz	170 MHz	135 MHz	Units
Clock Rate	Fmax	max	230	170	135	MHz
LD* Rate	LDmax		28.75	21.25	16.9	MHz
R/W, C0, C1, EXT Setup Time	1	min	0	0	0	ns
R/W, C0, C1, EXT Hold Time	2	min	10	10	10	ns
CE* Low Time	3	min	45	45	45	ns
CE* High Time	4	min	25	25	25	ns
CE* Asserted to Data Bus Driven	5	min	7	7	7	ns
CE* Asserted to Data Valid	6	max	45	45	45	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	15	ns
Write Data Setup Time	8	min	20	20	20	ns
Write Data Hold Time	9	min	0	0	0	ns
Pixel and Control Setup Time	10	min	3	3	3	ns
Pixel and Control Hold Time	11	min	2	2	2	ns
Clock Cycle Time	12	min	4.34	5.88	7.4	ns
Clock Pulse Width High Time	13	min	1.9	2.5	3.2	ns
Clock Pulse Width Low Time	14	min	1.9	2.5	3.2	ns
LD* Cycle Time	15	min	34.8	47	59	ns
LD* Pulse Width High Time	16	min	14	20	24	ns
LD* Pulse Width Low Time	17	min	14	20	24	ns
Analog Ouput Delay	18	typ	12	12	12	ns
Analog Ouput Rise/Fall Time	19	typ	2	2	2	ns
Analog Output Settling Time	20	max	tbd	tbd	tbd	ns
Clock and Data Feedthrough		typ	tbd	tbd	tbd	dB
Glitch Impulse (Note 1)		typ	50	50	50	pV-sec
Analog Output Skew		max	1	1	1	ns
Pipeline Delay		min	6	6	6	Clocks
		max	13	13	13	Clocks
VAA Supply Current (Note 2)	IAA	typ	450	380	360	mA
		max	tbd	tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 487 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. (See Figures 11 and 12 in the Timing Waveforms section.) As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2 x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 25° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms (continued)



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB for the Bt467.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 11. Video Input/Output Timing.

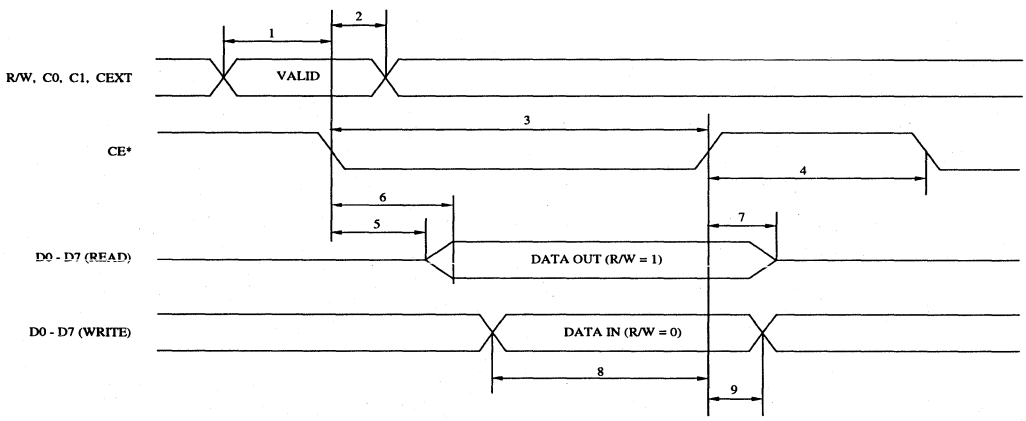


Figure 12. MPU Read/Write Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt467KG230	230 MHz	145 PGA	0° to +70° C
Bt467KG170	170 MHz	145 PGA	0° to +70° C
Bt467KG135	135 MHz	145 PGA	0° to +70° C

Preliminary Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt468

220 MHz
Monolithic CMOS
256 x 24 Color Palette
RAMDAC™

Distinguishing Features

- 220, 200, 170 MHz Operation
- 8:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- Pixel Panning Support
- On-Chip User-Definable Cursor
- RS-343A-Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X-Windows Support for Cursor
- Standard MPU Interface
- 145-pin PGA Package
- +5 V CMOS Monolithic

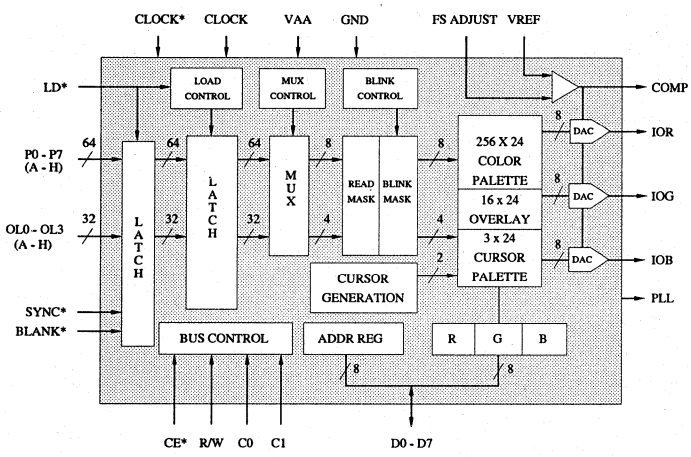
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439

Functional Block Diagram



Product Description

The Bt468 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL-compatible interface to the frame buffer, while maintaining the 220 MHz video data rates required for sophisticated color graphics.

On-chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), and pixel panning support.

The Bt468 has an on-chip three-color 64 x 64 pixel cursor and a three-color full-screen (or full-window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with subpixel resolution.

The Bt468 generates RS-343A-compatible red, green, and blue video signals. It can drive doubly-terminated 50 Ω or 75 Ω coax directly without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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L468001 Rev. E

Brooktree®

MPU Interface

As illustrated in the functional block diagram, the Bt468 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As presented in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

When the MPU is accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always logical zeros. ADDR0 and ADDR8 correspond to D0.

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0 (Note 1)
:	10	:
$010F	10	overlay color 15 (Note 1)
$0181	10	cursor color register 1 (Note 1)
:	:	cursor color register 2 (Note 1)
$0183	10	cursor color register 3 (Note 1)
$0200	10	ID register ($4F)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	reserved ($00)
$020B	10	test register
$020C	10	red output signature register
$020D	10	green output signature register
$020E	10	blue output signature register
$0220	10	revision register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$00FF	11	color palette RAM (Note 1)

Note 1: Requires three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

Although the color palette RAM, overlay RAM, and cursor color registers are dual ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, 1 or more of the pixels on the display screen can be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers and cursor RAM are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When the control registers and cursor RAM are accessed, the address register increments following a read or write cycle.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt468.

Single-Channel RAMDAC Operation

The Bt468 may be configured (through command register_2) to be a single-channel RAMDAC, enabling three Bt468s to be used in parallel for a 24-bit true-color system. The Bt468s share a common 8-bit data bus (D0–D7).

Each Bt468 must be configured to be either a red, green, or blue RAMDAC through command register_2. Only the green channel (IOG) of each RAMDAC is used; the IOR and IOB outputs should be connected to GND either directly or through a resistor up to 75 Ω.

To load the color palettes, the MPU performs the normal (red, green, and blue) write cycles to all three RAMDACs simultaneously. The red Bt468 loads color data only during the the red write cycle, the green Bt468 loads color data only during the green write cycle, and the blue Bt468 loads color data only during the blue write cycle.

To read the color palettes, the MPU performs the normal (red, green, and blue) read cycles from all three RAMDACs simultaneously. The red Bt468 outputs color data only during the the red read cycle, the green Bt468 outputs color data only during the green read cycle, and the blue Bt468 outputs color data only during the blue read cycle.

External circuitry must decode when the MPU is reading or writing to the color palettes and assert CE* to all three Bt468s simultaneously.

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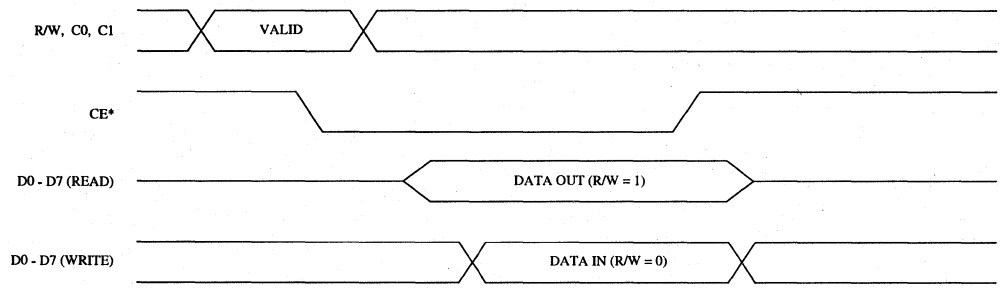

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt468 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for 8 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 8-pixel resolution. Typically, the LD* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

Typically, the Bt468 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until all 8 pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis. Or, the overlay inputs may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 8 , independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than six, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

Only one rising edge of LD* should occur every eight clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

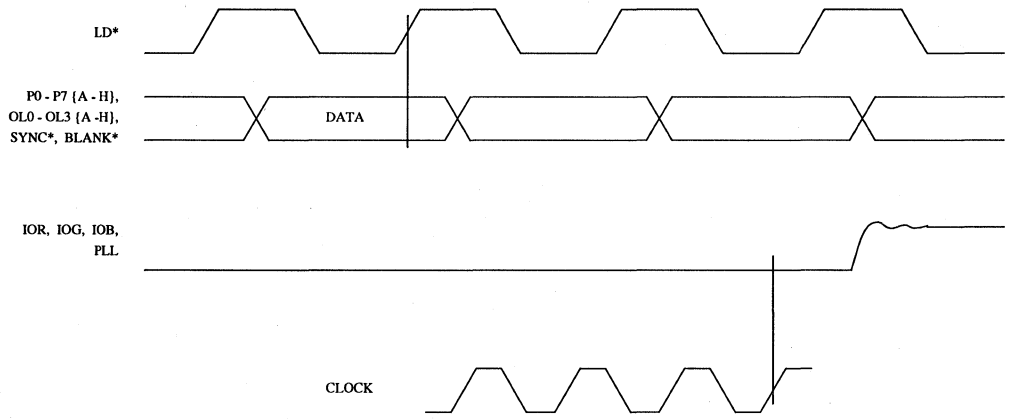

Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that blinking does not cause a color change to occur during the active display time (i.e., in the middle of the screen), the Bt468 monitors the SYNC* and BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 is the truth table used for color selection.

Pixel Panning

To support pixel panning, command register_1 specifies by what number of clock cycles to pan.

If 0-pixel panning is specified, pixel {A} is output first, followed by pixel {B}, then pixel {C}, etc., until all 8 pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, then pixel {D}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval and will not be on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B} through {H} will be output during the blanking interval and will not be on the display screen.

The process is similar for panning by 2–7 pixels.

When a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt468 during the first LD* cycle that BLANK* is a logical zero.

The P0–P7 and OL0–OL3 inputs are all panned. Cursor position is also panned. If the user desires to keep the cursor position the same relative to the edge of the display, the X register of the cursor position should be updated when the pixel panning register is updated.

Panning is done by delaying the SYNC* and BLANK* signals an additional one to seven clock cycles.

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Cursor1, Cursor0	CR05	OL0–OL3	P0–P7	Addressed by frame buffer
11	x	$x	$xx	cursor color 3
10	x	$x	$xx	cursor color 2
01	x	$x	$xx	cursor color 1
00	x	$F	$xx	overlay color 15
:	:	:	:	:
00	x	$1	$xx	overlay color 1
00	1	$0	$xx	overlay color 0
00	0	$0	$00	RAM location $00
00	0	$0	$01	RAM location $01
:	:	:	:	:
00	0	$0	$FF	RAM location $FF

Note: Refer to Figure 6 for generation of Cursor1 and Cursor0 control bits.

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

On-Chip Cursor Operation

The Bt468 has an on-chip, three-color, 64 x 64 pixel, user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor (x,y) register. The Bt468 expects (x) to increase to the right and (y) to increase down, as shown on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the first falling edge of SYNC* that is after a vertical sync has been detected. Vertical sync is detected as the second falling edge during blank.

The Bt468 must be reset to an eight-cycle pipeline delay for proper cursor pixel alignment.

Three-Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

A (0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each plane of cursor information may also be independently enabled or disabled for display through the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM. The cursor color registers, color palette RAM, or overlay RAM provides 24 bits of color information during the appropriate clock cycle, depending on the cursor pattern values.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the thirty-first column of the 64 x 64 array (assuming the columns start with 0 for the leftmost pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the thirty-first row of the 64 x 64 array (assuming the rows start with 0 for the topmost pixel and increment to 63). (See Figure 3.)

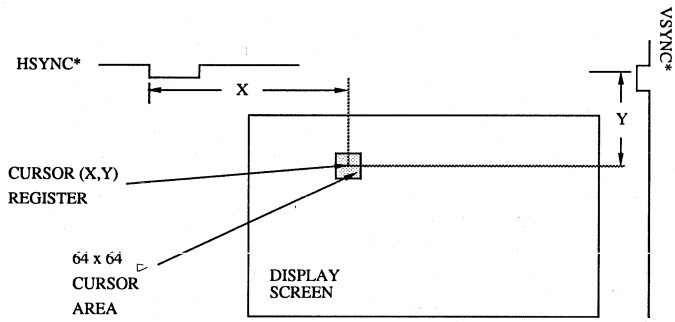

Figure 3. Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor

The cursor for the three-color cross hair cursor is also positioned through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than 1 pixel, the center of the intersection is the reference position.

When cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is displayed only within the cross hair window, which is specified by the window (x,y), window-width, and window-height registers. Since the cursor (x,y) register must specify a point within the window boundaries, *the software must ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.*

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000, and the window-width and -height registers should contain $0FFF. (See Figure 4.)

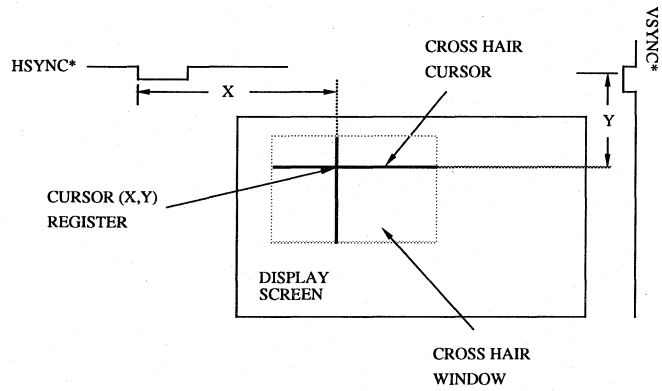

Figure 4. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual-Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors. Both cursor planes use the same cursor (x,y) registers.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical directions, it will be 1 pixel from true center about the cross hair cursor.

Figure 5 illustrates dual-cursor display.

In the 64 x 64 pixel area in which the user-definable cursor is displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will depend on the cursor pattern, whether they are logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 6 shows the equivalent cursor generation circuitry.

The Bt468 must be reset to an eight-cycle pipeline delay for proper cursor pixel alignment.

X-Windows Cursor Mode

In the X-Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Figure 9 in the Internal Registers section shows the organization of the cursor RAM while in the X-Windows mode.

If the cursor is configured for X-Windows mode, the cross hair cursor will not be displayed.

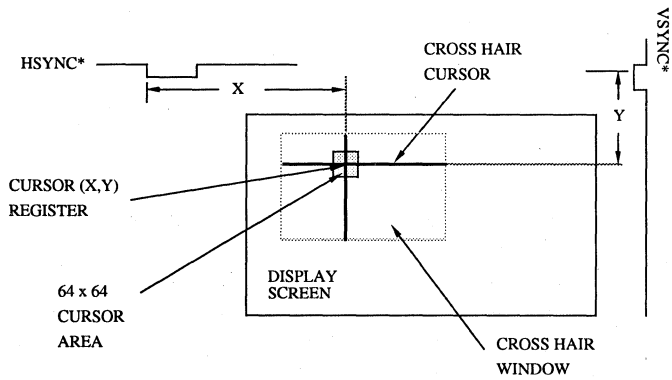

Figure 5. Dual-Cursor Positioning.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 7 and 8. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The Bt468 can drive either doubly-terminated 50 Ω or 75 Ω coax directly. If a 50 Ω double termination is used, then a typical RSET value is 348 Ω for a 7.5 IRE blanking pedestal and 332 Ω for a 0 IRE blanking pedestal. For a 75 Ω double termination, a typical RSET is 523 Ω for a 7.5 IRE blanking pedestal and 495 Ω for a 0 IRE blanking pedestal.

The varying output current from the D/A converters produces a corresponding voltage level that is used to drive the CRT monitor. Tables 3 and 4 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt468 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

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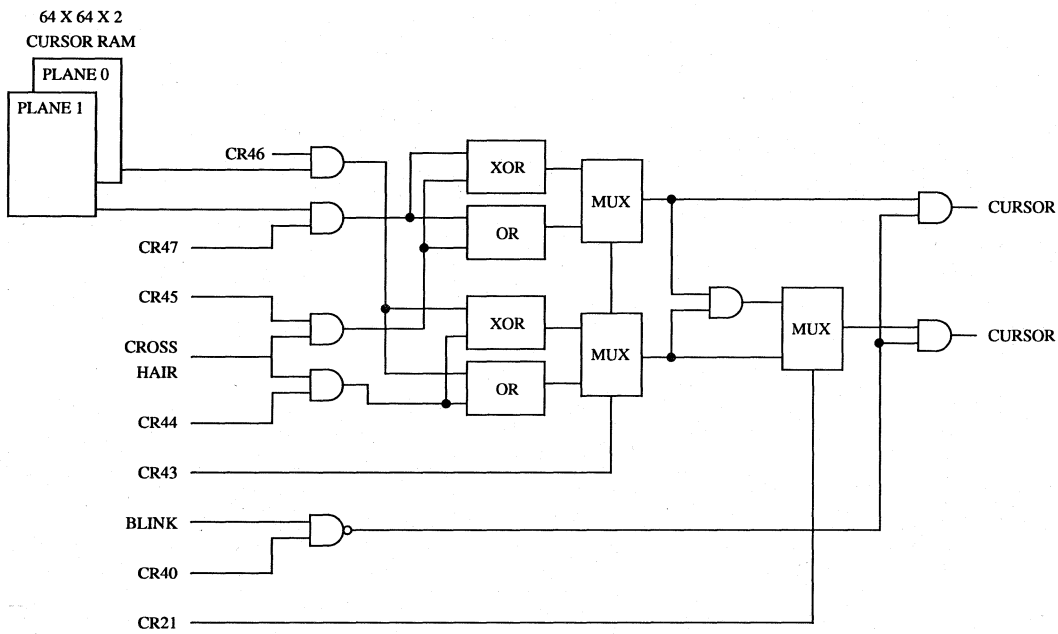
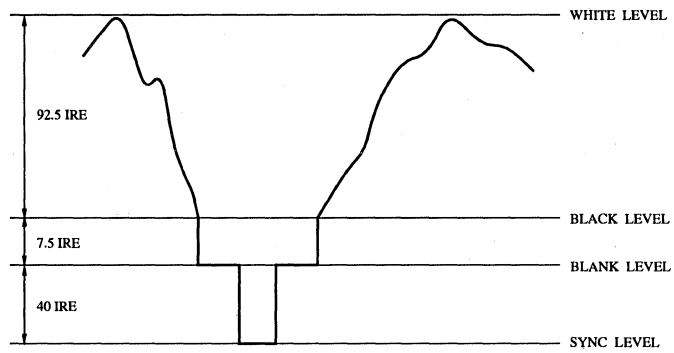


Figure 6. Cursor Control Circuitry.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
28.56	0.714	40.00	1.000
2.16	0.054	13.6	0.340
0.00	0.000	11.44	0.286
		0.00	0.000



Note: 50 Ω doubly-terminated load, RSET = 348 Ω, and VREF = 1.235 V. RS-343A levels and tolerances are assumed on all levels.

Figure 7. Composite Video Output Waveform (SETUP = 7.5 IRE).

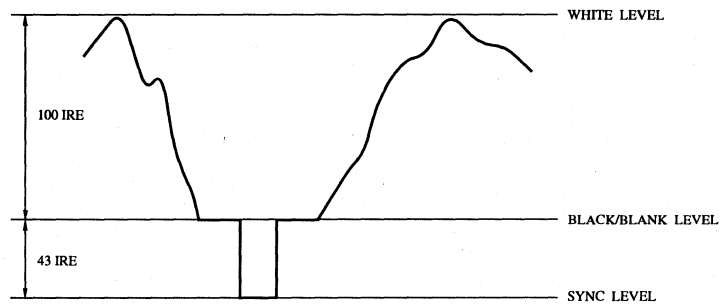
Description	IOG (mA)	IOR, IOB (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	40	28.56	1	1	$FF
DATA	data + 13.6	data + 2.16	1	1	data
DATA - SYNC	data + 2.16	data + 2.16	0	1	data
BLACK	13.6	2.16	1	1	$00
BLACK - SYNC	2.16	2.16	0	1	$00
BLANK	11.44	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 40 mA. RSET = 348 Ω and VREF = 1.235 V.

Table 3. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
27.90	0.698	40.00	1.000
0.00	0.000	12.08	0.302
		0.00	0.000



Note: 50 Ω doubly-terminated load, RSET = 332 Ω, and VREF = 1.235 V. RS-343A levels and tolerances are assumed on all levels.

Figure 8. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	40	27.9	1	1	$FF
DATA	data + 12.1	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	12.1	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	12.1	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 40 mA. RSET = 332 Ω and VREF = 1.235 V.

Table 4. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR00 corresponds to data bus bit D0.

CR07	reserved (logical one)	
CR06	reserved (logical zero)	
CR05	Overlay 0 enable (0) use color palette RAM (1) use overlay color 0	When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. (See Table 2.)
CR04	reserved (logical zero)	
CR03, CR02	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).
CR01, CR00	reserved (logical zero)	

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR10 corresponds to data bus bit D0.

CR17–CR15 Pan select

(000)	0 pixels	{pixel A}
(001)	1 pixel	{pixel B}
(010)	2 pixels	{pixel C}
(011)	3 pixels	{pixel D}
(100)	4 pixels	{pixel E}
(101)	5 pixels	{pixel F}
(110)	6 pixels	{pixel G}
(111)	7 pixels	{pixel H}

These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, then pixel {C}, etc.

CR14–CR10 reserved (logical zero)

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR20 corresponds to data bus bit D0.

CR27	Sync Enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt468 in three write cycles (red, green, and blue), and color data is output in three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt468 to emulate a single-channel RAMDAC with only the green channel (IOG).
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* to generate PLL information.
CR22	reserved (logical zero)	
CR21	X-Windows cursor select (0) normal cursor (1) X-Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X-Windows-compatible mode (logical one).
CR20	Test-mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt468, the value read by the MPU will be $4F. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–H}), and D3 corresponds to overlay plane 3 (OL3 {A–H}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always logical zeros.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–H}), and D3 corresponds to overlay plane 3 (OL3 {A–H}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always logical zeros.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Revision Register (Revision B only)

This 8-bit register is read-only, specifying the revision of the Bt468. The 4 most significant bits signify the revision letter B, in hexidecimal form. The 4 least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Internal Registers (continued)

Red, Green, and Blue Output Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. Test Features of the Bt468 in the the Application Information section contains more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

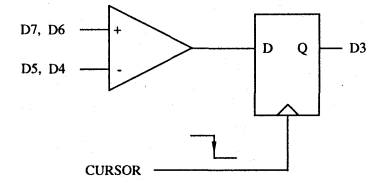
Test Register

This 8-bit register is used to test the Bt468. D0–D2 are used to specify which pixel input to use, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	pixel F
110	pixel G
111	pixel H

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be logical zeros.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt468. It is not initialized and may be written to or read by the MPU at any time. For proper operation, it must be initialized by the user after power-up. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is 1, 3, 5, or 7 pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window or the intersection of the cross hair cursor. The cursor (x) register is made up of the Cursor (x) Low Register (CXLR) and the Cursor (x) High Register (CXHR); the cursor (y) register is made up of the Cursor (y) Low Register (CYLR) and the Cursor (y) High Register (CYHR). They are not initialized and may be written to or read by the MPU at any time. For proper operation, they must be initialized by the user after power-up. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–72

where H = number of pixels between the first rising edge of CLOCK following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where V = number of scan lines from the first falling edge of SYNC* that is two or more clock cycles after vertical sync to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used when V < 32 and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the Window (x) Low Register (WXLR) and the Window (x) High Register (WXHR); the window (y) register is made up of the Window (y) Low Register (WYLR) and the Window (y) High Register (WYHR). They are not initialized and may be written to or read by the MPU at any time. For proper operation, they must be initialized by the user after power-up. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always logical zeros.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–40

where H = number of pixels between the first rising edge of CLOCK following the falling edge of SYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where V = number of scan lines from the first falling edge of SYNC* that is two or more clock cycles after vertical sync to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000, and the window-width and -height registers with $0FFF.

Internal Registers (continued)

Window-Width and -Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window-width register is made up of the Window-Width Low Register (WWLR) and the Window-Width High Register (WWHR); the window-height register is made up of the Window-Height Low Register (WHLR) and the Window-Height High Register (WHHR). They are not initialized and may be written to or read by the MPU at any time. For proper operation, they must be initialized by the user after power-up. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window-width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window-height register. Bits D4–D7 of WWHR and WHHR are always logical zeros.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 16 pixels more than the value specified by the window-width register. The actual window height is 16 pixels more than the value specified by the window-height register. Therefore, the minimum window width is 16 pixels, and the minimum window height is 16 pixels.

Values from $0000 to $0FFF may be written to the window-width and -height registers.

Internal Registers (continued)

Cursor RAM

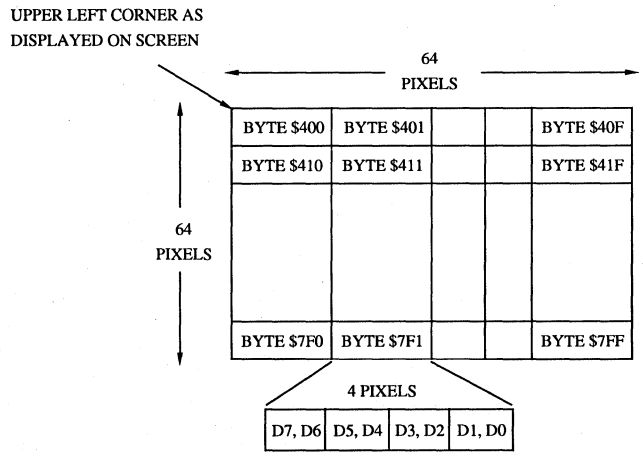
This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window and is not initialized. The cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention.

If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the cursor be positioned off-screen in the Y direction (write to the cursor (y) registers and wait for the vertical sync interval to move the cursor off-screen), write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write-then-read sequence, and if the correct cursor RAM data was not written, perform another write-then-read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 9 illustrates the internal format of the cursor RAM as it appears on the display screen. Addressing starts at location $400 as specified in Table 1.

When the Bt468 is in the X-Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: In both modes of operation, plane1 = D7, D5, D3, D1; and plane0 = D6, D4, D2, D0.



Normal Mode:

00 = color palette or overlay RAM
01 = cursor color 1
10 = cursor color 2
11 = cursor color 3

X-Windows Mode:

00 = color palette or overlay RAM
01 = color palette or overlay RAM
10 = cursor color 2
11 = cursor color 3

Figure 9. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 3 and 4. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 7 and 8). SYNC* does not override any other control or data input, as shown in Tables 3 and 4; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–H}, OL0–OL3 {A–H}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is one eighth of CLOCK, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P7 {A–H}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 2). Eight consecutive pixels (8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 8 pixels have been output, at which point the cycle repeats.
OL0– OL3 {A–H}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as shown in Table 2. When accessing the overlay palette RAM, the P0–P7 {A–H} inputs are ignored. Overlay information (up to 4 bits per pixel) for 8 consecutive pixels are input through this port. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 50 Ω coaxial cable (Figure 11 in the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt468s to be synchronized with subpixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 11). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. The PC Board Layout Considerations section contains critical layout criteria.

Pin Descriptions (continued)

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>VAA</td><td>Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>GND</td><td>Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>FS ADJUST</td><td>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 11). The IRE relationships in Figures 7 and 8 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

RSET (Ω) = K1 * VREF (V) / IOG (mA)

The full-scale output current on IOR and IOB for a given RSET is:

IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)

where K1 and K2 are defined as:

<table><tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr><tr><td>7.5 IRE</td><td>K1 = 11,294</td><td>K2 = 8,067</td></tr><tr><td>0 IRE</td><td>K1 = 10,684</td><td>K2 = 7,457</td></tr></table></td></tr>
<tr><td>VREF</td><td>Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 10, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 11. IF VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CLOCK,
CLOCK*</td><td>Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CE*</td><td>Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Glitches should be avoided on this edge-triggered input.</td></tr>
<tr><td>R/W</td><td>Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be logical zeros. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. (See Figure 1.)</td></tr>
<tr><td>C0, C1</td><td>Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as shown in Table 1. They are latched on the falling edge of CE*.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
</table>

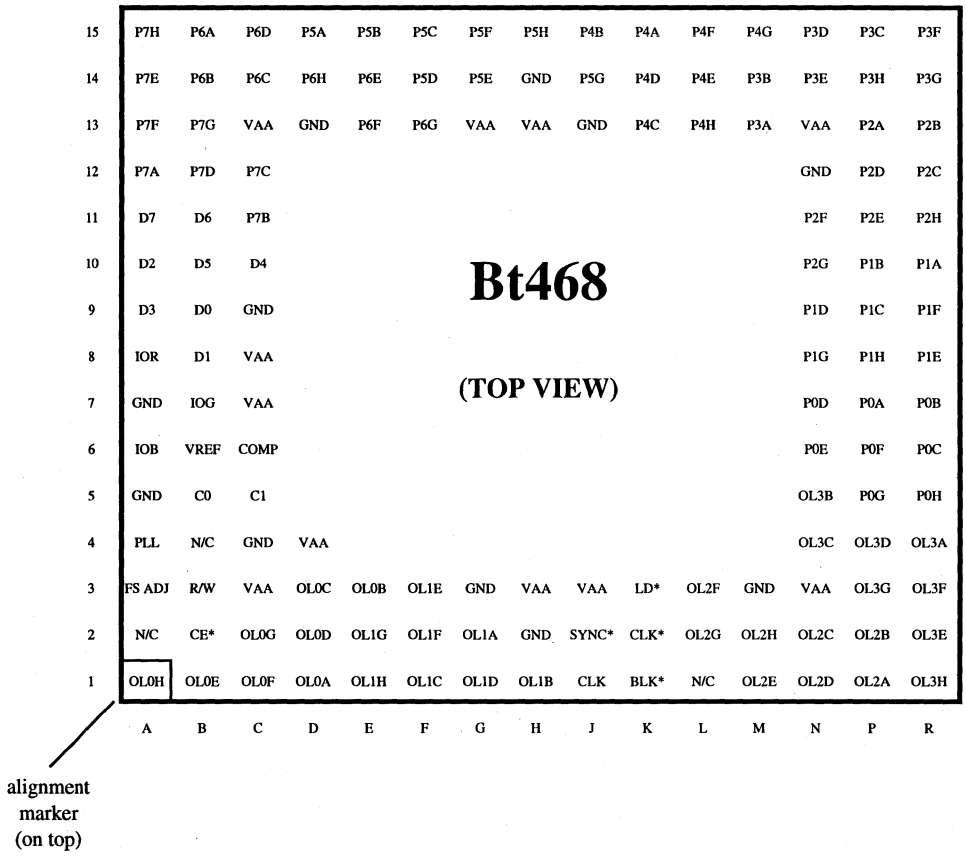
Pin Descriptions (continued)

Signal	Pin Number
BLANK*	K1
SYNC*	J2
LD*	K3
CLOCK	J1
CLOCK*	K2
P0A	P7
P0B	R7
P0C	R6
P0D	N7
P0E	N6
P0F	P6
P0G	P5
P0H	R5
P1A	R10
P1B	P10
P1C	P9
P1D	N9
P1E	R8
P1F	R9
P1G	N8
P1H	P8
P2A	P13
P2B	R13
P2C	R12
P2D	P12
P2E	P11
P2F	N11
P2G	N10
P2H	R11
P3A	M13
P3B	M14
P3C	P15
P3D	N15
P3E	N14
P3F	R15
P3G	R14
P3H	P14
P4A	K15
P4B	J15
P4C	K13
P4D	K14
P4E	L14
P4F	L15
P4G	M15
P4H	L13
COMP	C6
FS ADJUST	A3
VREF	B6

Signal	Pin Number
P5A	D15
P5B	E15
P5C	F15
P5D	F14
P5E	G14
P5F	G15
P5G	J14
P5H	H15
P6A	B15
P6B	B14
P6C	C14
P6D	C15
P6E	E14
P6F	E13
P6G	F13
P6H	D14
P7A	A12
P7B	C11
P7C	C12
P7D	B12
P7E	A14
P7F	A13
P7G	B13
P7H	A15
OL0A	D1
OL0B	E3
OL0C	D3
OL0D	D2
OL0E	B1
OL0F	C1
OL0G	C2
OL0H	A1
OL1A	G2
OL1B	H1
OL1C	F1
OL1D	G1
OL1E	F3
OL1F	F2
OL1G	E2
OL1H	E1
IOR	A8
IOG	B7
IOB	A6
PLL	A4
CE*	B2
R/W	B3
C0	B5
C1	C5

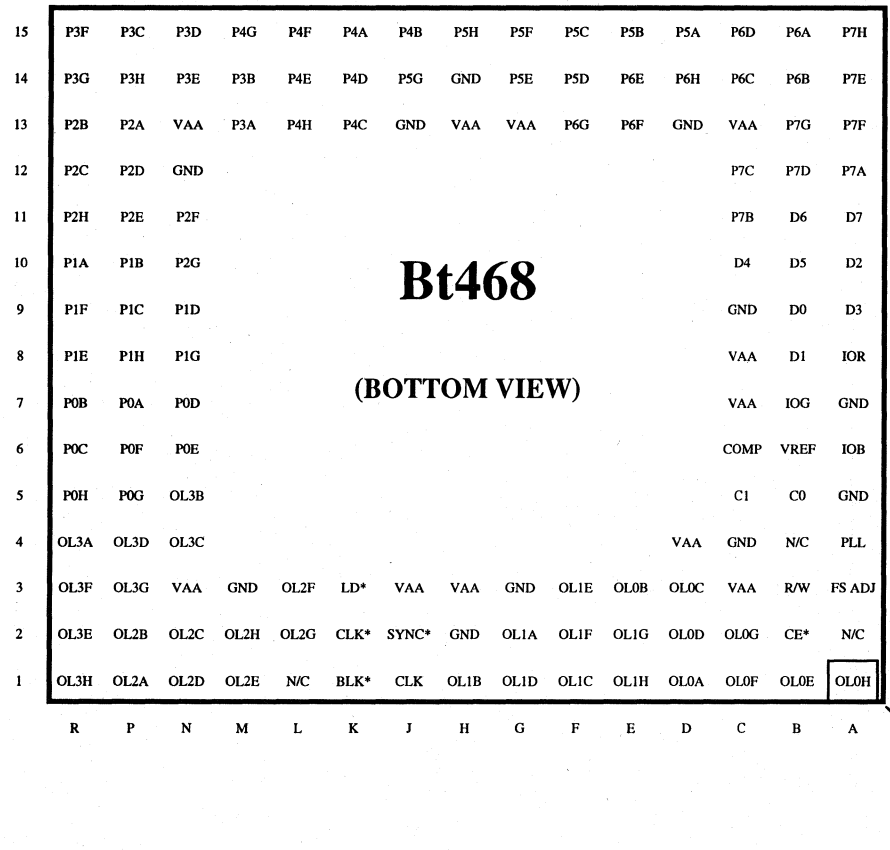
Signal	Pin Number
OL2A	P1
OL2B	P2
OL2C	N2
OL2D	N1
OL2E	M1
OL2F	L3
OL2G	L2
OL2H	M2
OL3A	R4
OL3B	N5
OL3C	N4
OL3D	P4
OL3E	R2
OL3F	R3
OL3G	P3
OL3H	R1
D0	B9
D1	B8
D2	A10
D3	A9
D4	C10
D5	B10
D6	B11
D7	A11
VAA	C3
VAA	C7
VAA	C8
VAA	C13
VAA	D4
VAA	G13
VAA	H3
VAA	H13
VAA	J3
VAA	N3
VAA	N13
GND	A5
GND	A7
GND	C4
GND	C9
GND	D13
GND	G3
GND	H2
GND	H14
GND	J13
GND	M3
GND	N12
reserved	A2
reserved	B4
reserved	L1

Pin Descriptions (continued)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	P7H	P6A	P6D	P5A	P5B	P5C	P5F	P5H	P4B	P4A	P4F	P4G	P3D	P3C	P3F
14	P7E	P6B	P6C	P6H	P6E	P5D	P5E	GND	P5G	P4D	P4E	P3B	P3E	P3H	P3G
13	P7F	P7G	VAA	GND	P6F	P6G	VAA	VAA	GND	P4C	P4H	P3A	VAA	P2A	P2B
12	P7A	P7D	P7C										GND	P2D	P2C
11	D7	D6	P7B										P2F	P2E	P2H
10	D2	D5	D4										P2G	P1B	P1A
9	D3	D0	GND										P1D	P1C	P1F
8	IOR	D1	VAA										P1G	P1H	P1E
7	GND	IOG	VAA										P0D	P0A	P0B
6	IOB	VREF	COMP										P0E	P0F	P0C
5	GND	C0	C1										OL3B	P0G	P0H
4	PLL	N/C	GND	VAA									OL3C	OL3D	OL3A
3	FS ADJ	R/W	VAA	OL0C	OL0B	OL1E	GND	VAA	VAA	LD*	OL2F	GND	VAA	OL3G	OL3F
2	N/C	CE*	OL0G	OL0D	OL1G	OL1F	OL1A	GND	SYNC*	CLK*	OL2G	OL2H	OL2C	OL2B	OL3E
1	OL0H	OL0E	OL0F	OL0A	OL1H	OL1C	OL1D	OL1B	CLK	BLK*	N/C	OL2E	OL2D	OL2A	OL3H

Pin Descriptions (continued)



	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
15	P3F	P3C	P3D	P4G	P4F	P4A	P4B	P5H	P5F	P5C	P5B	P5A	P6D	P6A	P7H
14	P3G	P3H	P3E	P3B	P4E	P4D	P5G	GND	P5E	P5D	P6E	P6H	P6C	P6B	P7E
13	P2B	P2A	VAA	P3A	P4H	P4C	GND	VAA	VAA	P6G	P6F	GND	VAA	P7G	P7F
12	P2C	P2D	GND										P7C	P7D	P7A
11	P2H	P2E	P2F										P7B	D6	D7
10	P1A	P1B	P2G										D4	D5	D2
9	P1F	P1C	P1D										GND	D0	D3
8	P1E	P1H	P1G										VAA	D1	IOR
7	P0B	P0A	P0D										VAA	IOG	GND
6	P0C	P0F	P0E										COMP	VREF	IOB
5	P0H	P0G	OL3B										C1	C0	GND
4	OL3A	OL3D	OL3C									VAA	GND	N/C	PLL
3	OL3F	OL3G	VAA	GND	OL2F	LD*	VAA	VAA	GND	OL1E	OL0B	OL0C	VAA	R/W	FS ADJ
2	OL3E	OL2B	OL2C	OL2H	OL2G	CLK*	SYNC*	GND	OL1A	OL1F	OL1G	OL0D	OL0G	CE*	N/C
1	OL3H	OL2A	OL2D	OL2E	N/C	BLK*	CLK	OL1B	OL1D	OL1C	OL1H	OL0A	OL0F	OL0E	OL0H

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PC Board Layout Considerations

PC Board Considerations

The Bt468 layout should be optimized for lowest noise on the Bt468 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt468 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 10.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 10 µF capacitor shown in Figure 11 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt468 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

PC Board Layout Considerations (continued)

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt468 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt468 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 11 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

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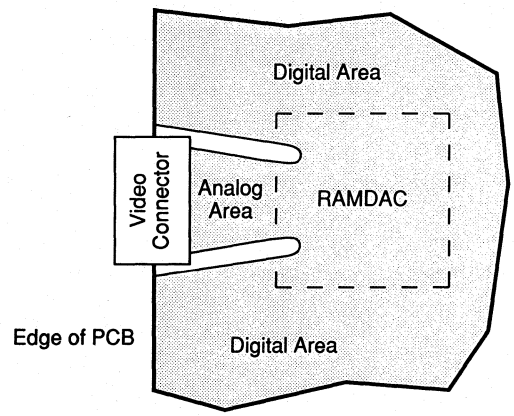
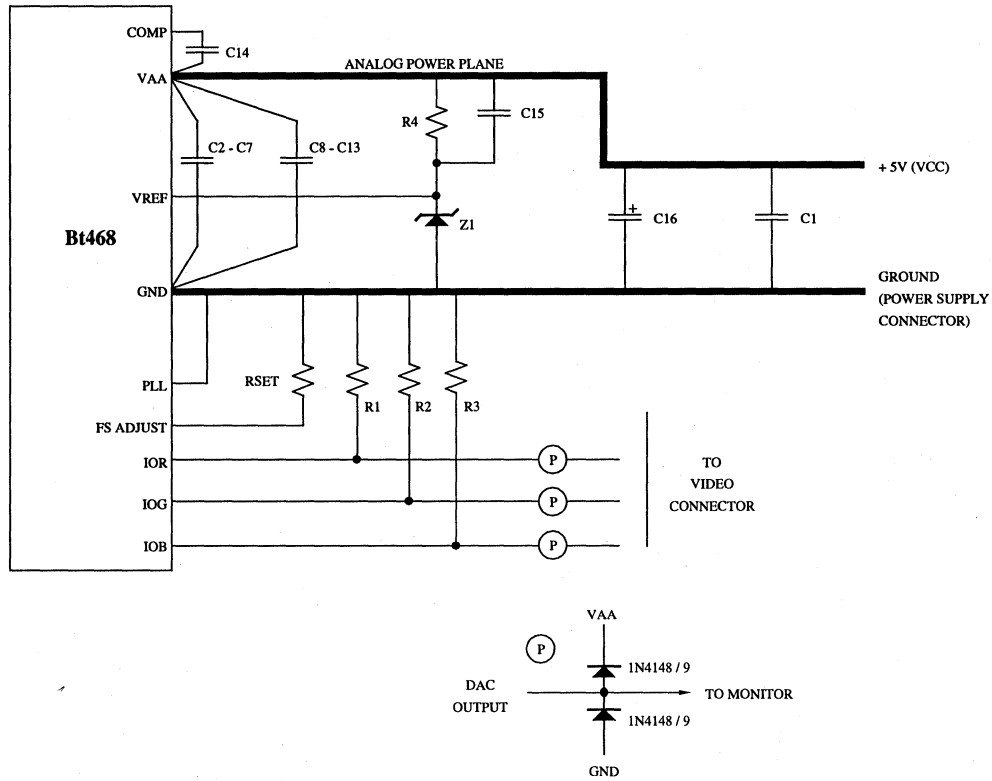


Figure 10. Sample Layout Showing Power and Ground Plane Isolation Gaps.

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C7, C14, C15	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C8–C13	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C16	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	50 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	348 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt468.

Figure 11. Typical Connection Diagram and Parts List.

Clock Interfacing

Because of the high clock rates at which the Bt468 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt468 will not function if a single-ended clock is used with CLOCK* connected to ground.

For 170 MHz and greater applications, robust ECL clock signals with strong pulldown (~20 mA at VOH) and double termination are required if clock trace lengths are greater than 2 inches.

Typically, LD* is generated by dividing CLOCK by 8 and translating the result to TTL levels. As LD* may be phase shifted relative to CLOCK, propagation delays need not be considered when the LD* signal is being derived. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC* and BLANK*).

For display applications in which a single Bt468 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt468 and sets the pipeline delay of the Bt468 to eight clock cycles. Figure 12 illustrates use of the Bt438 with the Bt468.

When a single Bt468 is used, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Using Multiple Bt468s

For display applications in which up to four Bt468s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt468, synchronizes the signals to subpixel resolution, and sets the pipeline delay of the Bt468 to eight clock cycles. Figure 13 illustrates use of the Bt439 with the Bt468.

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt468, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt468s and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt468s, minimizing the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

If subpixel synchronization of multiple Bt468s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt468s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). Skew must be minimized on the CLOCK and CLOCK* lines. The PLL outputs are not used and should be connected to GND (either directly or through a resistor up to 150 Ω).

When multiple Bt468s are used, each Bt468 should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Each Bt468 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

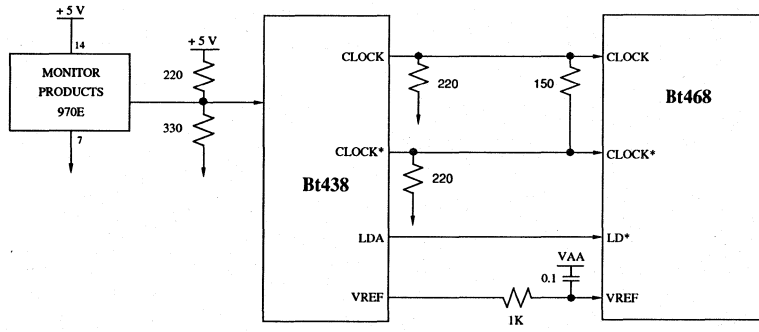


Figure 12. Generating the Bt468 Clock Signals.

Application Information (continued)

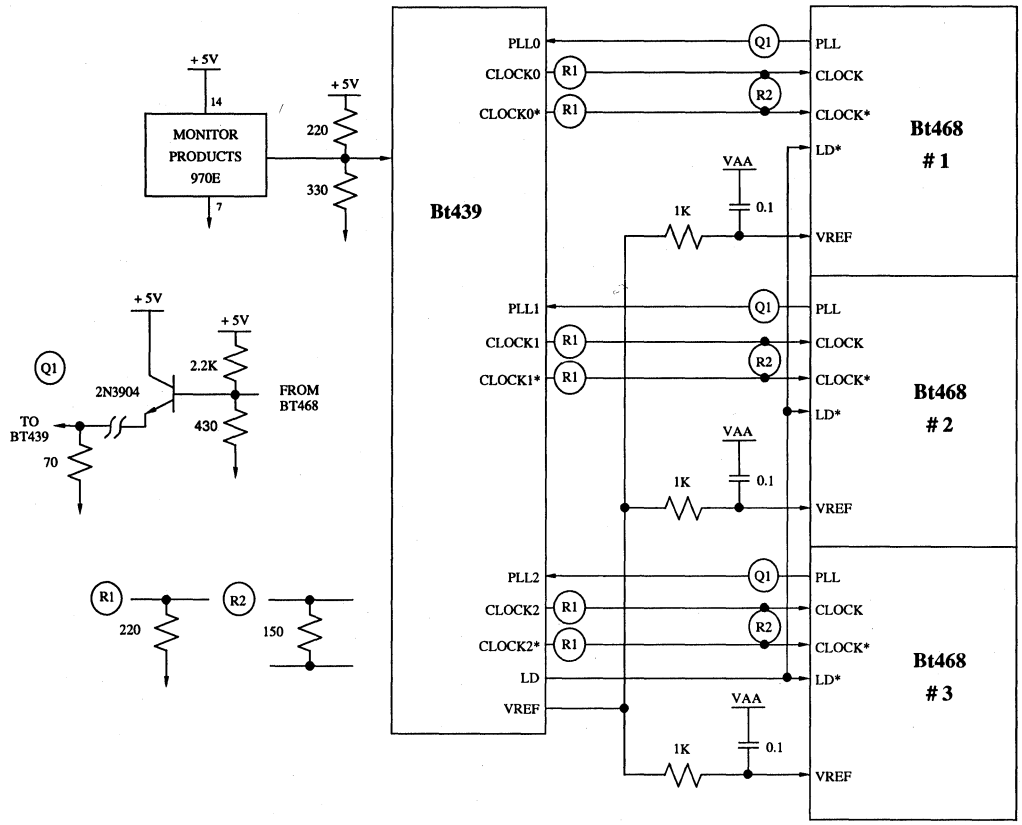


Figure 13. Generating the Clock Signals for Multiple Bt468s.

Setting the Pipeline Delay

The pipeline delay of the Bt468, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt468 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt468.

To reset the Bt468, it should be powered up with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. The device can be held with CLOCK and CLOCK* stopped for an unlimited time.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

In order to ensure that the Bt468 has the proper configuration, all of the command registers must be initialized prior to a fixed-pipeline reset. Because of this requirement, the power-up that occurs prior to initialization of the command registers cannot be used to ensure the fixed pipeline. An additional reset is required after command register writes.

When the Bt468 is reset to an eight-clock-cycle pipeline delay, the blink counter circuitry is not reset. Therefore, if the multiple Bt468s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits logical zeros. Software may control blinking through the read mask register and overlay display enable bits.

The Bt468 must be reset to an eight-clock-cycle pipeline delay for proper cursor pixel alignment.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt468

The Bt468 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section explains the operating use of these test features.

Signature Register (Signature Mode)

The signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs.

The SARs act as a 24-bit-wide linear feedback shift register on each succeeding pixel that is latched. The SARs latch only 1 pixel per load group. Thus the SARs are operating on only every eighth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, E, F, G, or H) is latched for generating new signatures by setting bits D0–D2 in the test register.

The Bt468 will only generate signatures while in active-display (BLANK* negated). The SARs are available for reading and writing through the MPU port when the Bt468 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan line or one frame buffer of pixels, will be input to the chip. Then, at the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested with the signature registers.

The above process is repeated with all different pixel phases—A, B, C, etc.,—selected.

The linear feedback configuration is shown in Figure 14. Each register internally uses XORs at each input bit (D_n) with the output (result) by 1 least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can be used as the seed, for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

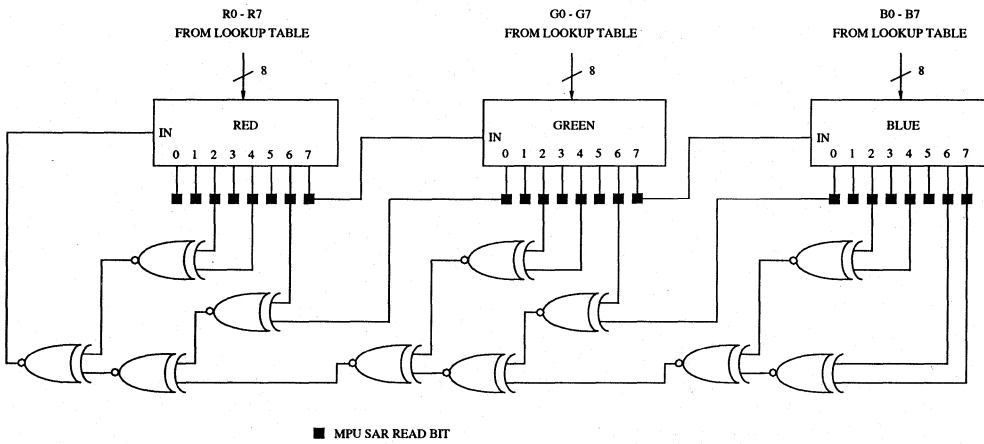


Figure 14. Signature Analysis Register Circuit.

Application Information (continued)

Signature Register (Data-Strobe Mode)

Setting command bit CR20 to one puts the SARs into data-strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the generation signatures by the SARs. Instead, the SARs capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt468. The levels of most inputs are insignificant *except* that CLOCK should be high and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

In general, the color readout will correspond to a pixel latched on the previous load. However, because the data path is pipelined, the color may come from an earlier load cycle. To read successive pixels, LD* should be toggled, the CLOCK pins should be pulsed according to the mux state (eight periods), and all pixel-related inputs should be held and the three MPU reads performed as described. This overall process is best done on a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt468 is the analog output comparator. It allows the user to measure the DACs against each other as well as against a specific reference voltage.

Four combinations of tests are selected through the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register on each of the 64 scan lines of the 64 x 64 user-defined cursor block. (The 64 x 64 cursor must be enabled for display.) On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point actually occurs over the leftmost edge of the 64 x 64 cursor block.

Because of the comparator's simple design, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading test register bit D3.

Application Information (continued)

Initializing the Bt468

Following a power-on sequence, the Bt468 must be initialized. This sequence will configure the Bt468 as follows:

8:1 multiplexed operation
no overlays, no blinking, no panning
64 x 64 block cursor, no cross hair cursor
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to reserved location	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern

Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization

Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		25		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		348		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short-Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND – 0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input Differntial Voltage	ΔVIN	.6		6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		26.56	28.56	30.56	mA
White Level Relative to Black		25.08	26.40	27.72	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.48	2.16	2.84	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		9.44	11.44	13.44	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			103.5		µA
DAC-to-DAC Matching				5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		9	11.44	14	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–1.0		+2.5	V
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, PLL = 0 mA)			10		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 348 Ω and VREF = 1.235 V. SETUP = 7.5 IRE with 50 Ω double termination. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	220/200 MHz Devices Min	220/200 MHz Devices Typ	220/200 MHz Devices Max	170 MHz Devices Min	170 MHz Devices Typ	170 MHz Devices Max	Units
Clock Rate	Fmax			220/200			170	MHz
LD* Rate	LDmax			27.5/25			21.25	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	10			10			ns
CE* Low Time	3	45			45			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			45			45	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	20			20			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	4.5/5			5.88			ns
Clock Pulse Width High Time	13	2/2.2			2.5			ns
Clock Pulse Width Low Time	14	2/2.2			2.5			ns
LD* Cycle Time	15	36/40			47			ns
LD* Pulse Width High Time	16	13.5/15			20			ns
LD* Pulse Width Low Time	17	13.5/15			20			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		1			1		ns
Analog Output Settling Time	20			tbd			tbd	ns
Clock and Data Feedthrough (Note 1)			tbd			tbd		dB
Glitch Impulse (Note 1)			50			50		pV - sec
DAC-to-DAC Crosstalk			tbd			tbd		dB
Analog Output Skew			0	1		0	1	ns
Pipeline Delay		6		13	6		13	Clocks
VAA Supply Current (Note 2)	IAA		450	tbd		430	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 348 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing waveforms and notes in Figures 15 and 16. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 25° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms

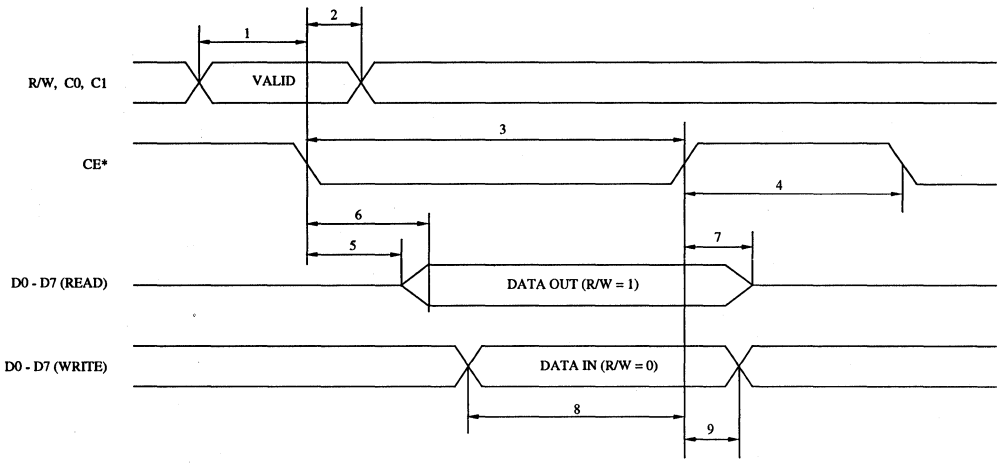
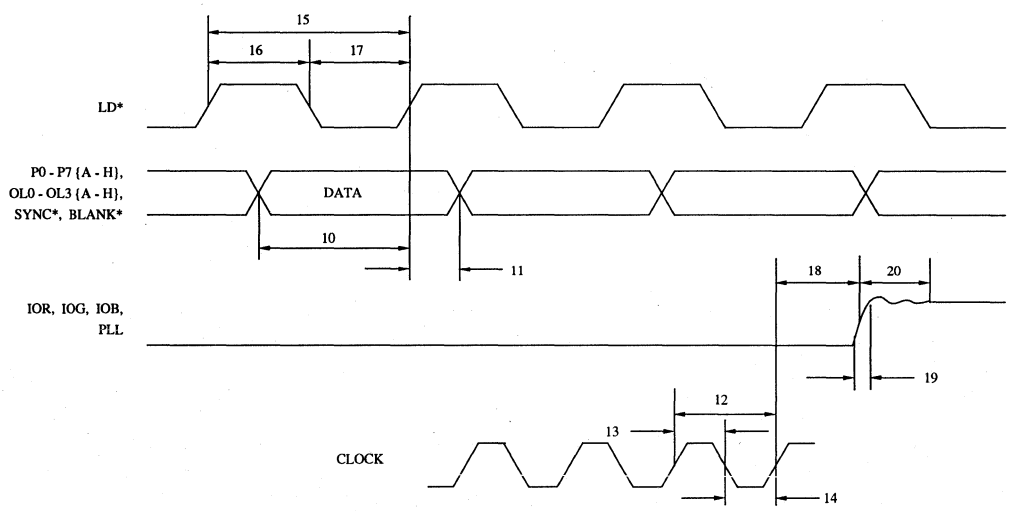


Figure 15. MPU Read/Write Timing Dimensions.



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale

Figure 16. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt468KG220	220 MHz	145-pin Ceramic PGA	0° to +70° C
Bt468KG200	200 MHz	145-pin Ceramic PGA	0° to +70° C
Bt468KG170	170 MHz	145-pin Ceramic PGA	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt492

360 MHz
100K ECL-Compatible
256 x 8 Color Palette
RAMDAC™

Distinguishing Features

- 360 MHz Pipelined Operation
- 256 x 8 Color Palette RAM
- 16 x 8 Overlay RAM
- 500 ps Typical Rise/Fall Time
- RS-343A Compatible Output
- 0 or 7.5 IRE Blanking Pedestal
- 1 V Drive Into 25 Ω Output Loads
- 100K ECL-Compatible Pixel Inputs
- Divide-by-2 of Clock for Load Generation
- TTL-Compatible MPU Interface
- 68-pin Ceramic PGA Package with Heatsink and Alignment Pin
- Typical Power Dissipation: 3.5 W

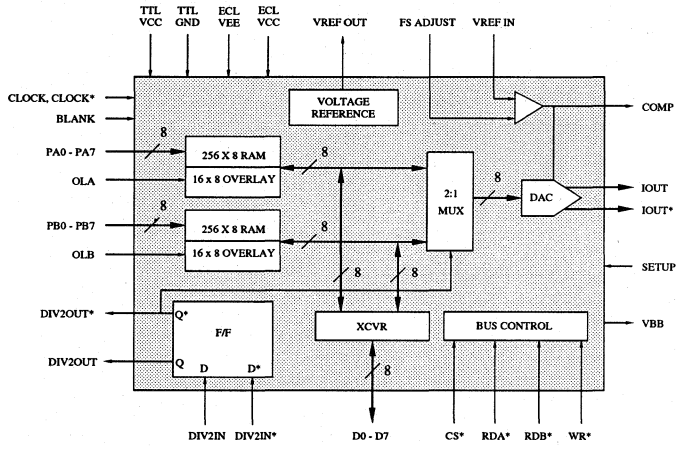
Applications

- Graphics Terminals
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt424

Functional Block Diagram



Product Description

The Bt492 is an 8-bit RAMDAC designed specifically for high-performance, high-resolution color graphics.

The 2:1 multiplexed pixel inputs enable Bt492 interface with 180 MHz pixel data, simplifying interface with the frame buffer. On-chip divide- by-2 of the clock is provided, generating the 180 MHz differential load clocks. The pixel, DIV2IN, and blank inputs, and the DIV2OUT and DIV2OUT* outputs, are 100K ECL compatible. The blanking signal is pipelined to maintain synchronization with the pixel data.

The MPU interface signals (D0–D7, CS*, RDA*, RDB*, and WR*) are TTL compatible. During MPU accesses to the RAM, the address is input through the pixel ports (PA0–PA7 and PB0–PB7).

An on-chip voltage reference is available, or an external reference may be used. A single external resistor controls the full-scale output current.

The Bt492 generates an RS-343A-compatible video signal and can drive either doubly- terminated 75 Ω or 50 Ω coax directly without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/2 LSB over the full temperature range.

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L492001 Rev. H

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt492 has two 256 x 8 RAMs, a 2:1 multiplexer, a single 8-bit DAC, and an MPU interface.

MPU data is input and output through the D0–D7 data lines. During MPU accesses to the color palette RAMs, the RAMs are addressed through the PAx, PBx, and OLx inputs, and the internal pipeline registers are transparent. During MPU write cycles (WR* = 0), data is written to both RAMs. The MPU may read either RAM through the RDA* and RDB* control inputs. (See Figure 1.)

BLANK should be asserted during MPU accesses to prevent the data values associated with the MPU address from appearing at the analog outputs. Following an MPU cycle, BLANK should be asserted for at least one valid pixel cycle before the PAx and PBx inputs can be properly routed to the analog outputs.

Frame Buffer Interface

Pixel data on the PA0–PA7 and OLA inputs (even data), and PB0–PB7 and OLB inputs (odd data) is latched on the falling edge of DIV2OUT*, as illustrated in Figure 2.

The OLx inputs determine whether the Px0–Px7 inputs address the 256 x 8 color palette RAM (OLx = 0) or the 16 x 8 overlay palette RAM (OLx = 1). When addressing the overlay RAM, Px4–Px7 are ignored. The outputs of the RAMs are then multiplexed at the pixel clock rate, and they drive the 8-bit video D/A converter.

DIV2IN is defined to be one half the CLOCK rate. To simplify system design, the Bt492 outputs a DIV2OUT* signal which, when connected to the DIV2IN pin, generates a clock equal to one half the CLOCK rate. For a color system requiring three Bt492s, the DIV2OUT signals may be synchronized by connecting the DIV2OUT* signal on one of the devices to the DIV2IN pins of all three devices. Signal paths must be kept short and equal for each connection. The unused DIV2OUT signals from the remaining Bt492s can be used to clock the shift registers driving the Bt492 pixel inputs.

The BLANK input is also latched on the falling edge of DIV2OUT*. This input overrides the PA0–PA7, OLA, PB0–PB7, and OLB inputs. Blanking information is output synchronously with the even pixel data.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and ECL VCC. RSET has a typical value of 1092 Ω for generation of RS-343A video into a 37.5 Ω load, or 729 Ω for generation of RS-343A video into a 25 Ω load. The on-chip voltage reference (VREF OUT) may be used to provide the reference for the VREF IN pins of up to three Bt492s, or an external reference may be used.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOUT output through a 25 Ω resistor to ECL VCC (assuming a doubly- terminated 50 Ω load). The IOUT* output is used to generate the positive video signal.

The D/A converter on the Bt492 uses a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed when identical current sources and current steering their outputs are used. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt492 can directly drive either a 37.5 Ω or 25 Ω load, such as a doubly-terminated 75 Ω or 50 Ω coaxial cable.

Circuit Description (continued)

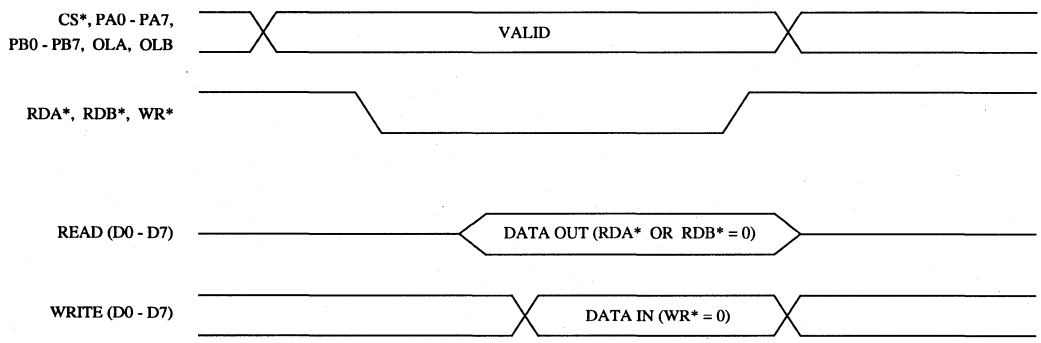

Figure 1. MPU Read/Write Timing.

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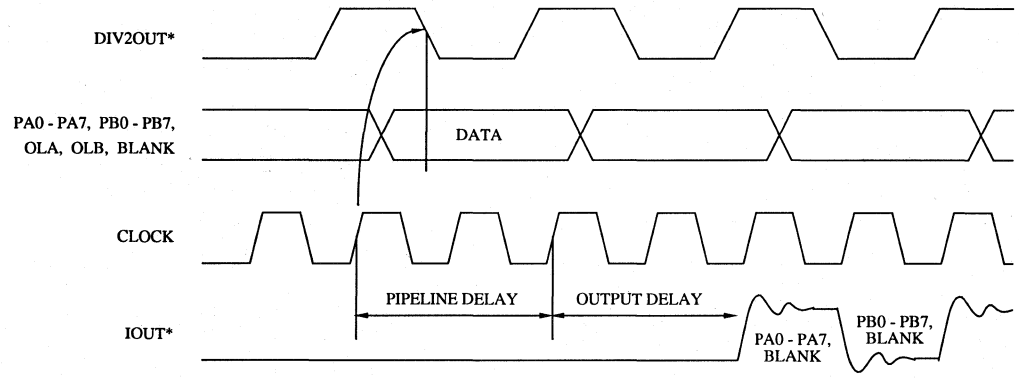
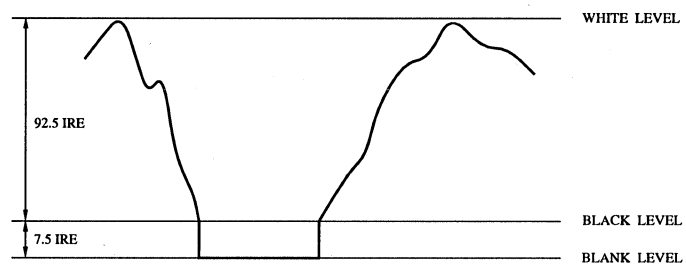


Figure 2. Video Input/Output Timing.

MA RSET = 729	MA RSET = 1092	V
00.00	00.00	0.000
- 26.40	- 17.60	- 0.660
- 28.56	- 19.05	- 0.714



Note: RSET = 729 Ω (50 Ω doubly-terminated load) or 1092 Ω (75 Ω doubly-terminated load), and VREF IN = –1.2 V. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveforms (IOUT*).

Description	RSET = 729 Ω IOUT* (mA)	RSET = 1092 Ω IOUT* (mA)	BLANK	DAC Input Data
WHITE	0	0	0	$FF
DATA	data	data	0	data
BLACK	–26.40	–17.62	0	$00
BLANK			1	$xx
SETUP = ECL VCC	–26.40	–17.62		
SETUP = float	–28.56	–19.05		

Note: Typical with VREF IN = –1.2 V.

Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logical one drives the analog output to the blanking level, as specified in Table 1. It is latched on the falling edge of DIV2OUT*. When BLANK is a logical one, the PA0–PA7, PB0–PB7, OLA, and OLB inputs are ignored. Blanking information is output synchronously with the even pixel data.
PA0–PA7, PB0–PB7	Even and odd pixel data inputs (ECL compatible). D0 is the least significant data bit. They are latched on the falling edge of DIV2OUT* while CS* is a logical one. PAx represent the even pixel data, and PBx represent the odd pixel data. Even data represents the first (leftmost) pixel on the display screen. Coding is binary. PA0 and PB0 are the LSBs.
OLA, OLB	Even and odd overlay data inputs (ECL compatible). When OLA or OLB are a logical one, the 4 MSBs of the corresponding pixel inputs (Px4–Px7) are ignored, and the 4 LSBs are used to select 1 of 16 available data words in the overlay palette. OLA and OLB are latched on the falling edge of DIV2OUT* while CS* is a logical one. If left floating, they will pull themselves to DVEE.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). They are typically the pixel clock rate of the video system.
DIV2IN, DIV2IN*	Differential CLOCK/2 inputs (ECL compatible). These clocks must be one half the CLOCK rate. They may be configured for single-ended operation by connecting DIV2IN* to VBB.
DIV2OUT*, DIV2OUT	CLOCK/2 differential outputs (ECL compatible). When DIV2OUT* is connected to the DIV2IN pin, these outputs are one half the CLOCK rate. When not connected to DIV2IN, they generate a signal that is DIV2IN synchronized to CLOCK and inverted.
IOUT, IOUT*	Differential video current outputs. These high-impedance current sources can directly drive either a doubly-terminated 50 Ω or 75 Ω coaxial cable (Figures 4 and 5 in the PC Board Layout Considerations section). Both outputs, whether used or not, should have the same output load for best settling time.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 µF ceramic chip capacitor must be connected between this pin and AVEE (Figures 4 and 5). The COMP capacitors must be as close to the device as possible to keep lead inductance to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
SETUP	Pedestal control input. If SETUP is connected to ECL VCC, the blanking pedestal on the output is disabled, making the black and blanking levels the same (0 IRE). If SETUP is left floating, the 7.5 IRE blanking pedestal is enabled (see Figure 3).
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and ECL VCC controls the magnitude of the full-scale video signal (Figures 4 and 5). The IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: RSET (Ω) = K * VREF IN (V) / IOUT (mA) where K = 17,205 if SETUP = float or 15,915 if SETUP = ECL VCC. *Note:* The RSET value may require adjustment to generate the specified video levels because of variations in processing and depending on whether the internal or an external reference is used.

Pin Descriptions (continued)

Pin Name	Description
VREF OUT	Voltage reference output. This output provides a –1.2 V (typical) reference and may be connected to the VREF IN inputs of up to three Bt492s. When driving multiple Bt492s, 100 Ω of interconnect resistance should be used to minimize noise pickup. If VREF OUT is not used to provide a voltage reference, it should remain floating.
VREF IN	Voltage reference input. An external voltage reference, such as the one shown in Figure 6 in the Application Information section, or the VREF OUT pin must supply this input with a –1.2 V (typical) reference. A 0.01 µF ceramic chip capacitor in parallel with a 0.001 µF ceramic chip capacitor must be connected between this pin and ECL VCC, as shown in Figures 4 and 5. The decoupling capacitors must be as close to the device as possible to keep lead inductance to an absolute minimum.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable MPU data to be written to or read from the device. When CS* is a logical one, D0–D7 are three-stated. While CS* is a logical zero, the PA0–PA7, PB0–PB7, OLA, and OLB inputs are used to address the color palette RAM and overlay RAM, and the internal pipeline registers are configured to be transparent.
RDA*, RDB*	Read control input (TTL compatible). To read data from RAM A, both CS* and RDA* must be logical zeros. To read data from RAM B, both CS* and RDB* must be logical zeros. MPU addressing on PAx, PBx, and OLx must be valid while RDA* or RDB* is a logical zero. CS*, RDA*, and RDB* must not be logical zeros simultaneously (see Figure 9 in the Timing Waveforms section).
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be logical zeros. MPU addresses on PAx and PBx are accepted on the falling edge of WR* or CS*, whichever occurs first. Data is accepted on the rising edge of WR* or CS*, whichever occurs first. MPU addressing on PAx, PBx, and OLx must be valid while WR* is a logical zero. RDx* and WR* must not be logical zeros simultaneously (see Figure 10 in the Timing Waveforms section).
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VBB	A –1.3 V output. A 0.01 µF decoupling capacitor to ECL VCC reduces threshold jitter.
TTL VCC	TTL power. All TTL VCC pins must be connected together.
TTL GND	TTL ground. All TTL GND pins must be connected together.
ECL VCC	ECL ground. All ECL VCC pins must be connected together (see Figures 4 and 5).
DVEE	ECL digital power. All DVEE pins must be connected together (see Figures 4 and 5).
AVEE	ECL analog power. All AVEE pins must be connected together (see Figures 4 and 5).
	Warning: A ferrite bead must be used to connect the AVEE power pins to the analog power plane, as illustrated in Figures 4 and 5.
Alignment Pin	The alignment pin is connected to the metallic cavity lid, which is electrically isolated.

Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
CLOCK	H1	D0	E10	VBB	C2
CLOCK*	G2	D1	D11		
		D2	D10	TTL VCC	F11
DIV2IN	D1	D3	C11		
DIV2IN*	D2	D4	C10	TTL GND	F10
DIV2OUT	E2	D5	B11	TTL GND	E11
DIV2OUT*	E1	D6	A10	TTL GND	A9
		D7	B10	TTL GND	B9
BLANK	H2				
		CS*	B7	ECL VCC	A6
PA0	J2	RDA*	A7	ECL VCC	F1
PA1	K1	RDB*	B8	ECL VCC	L6
PA2	L2	WR*	A8	ECL VCC	K10
PA3	L3			ECL VCC	K11
PA4	K3	IOUT	J10, J11		
PA5	L4	IOUT*	H10, H11	DVEE	A5
PA6	K4			DVEE	B6
PA7	L5	SETUP	K7	DVEE	F2
OLA	K5	COMP	L8	DVEE	G1
		VREF IN	K8	DVEE	K6
PB0	C1	VREF OUT	K9	DVEE	L7
PB1	B2	FS ADJUST	L9		
PB2	B1			AVEE	G10
PB3	A2	N/C	K2	AVEE	G11
PB4	B3	N/C	J1		
PB5	A3	N/C	L10	alignment	C3
PB6	B4			pin (LID)	
PB7	A4				
OLB	B5				

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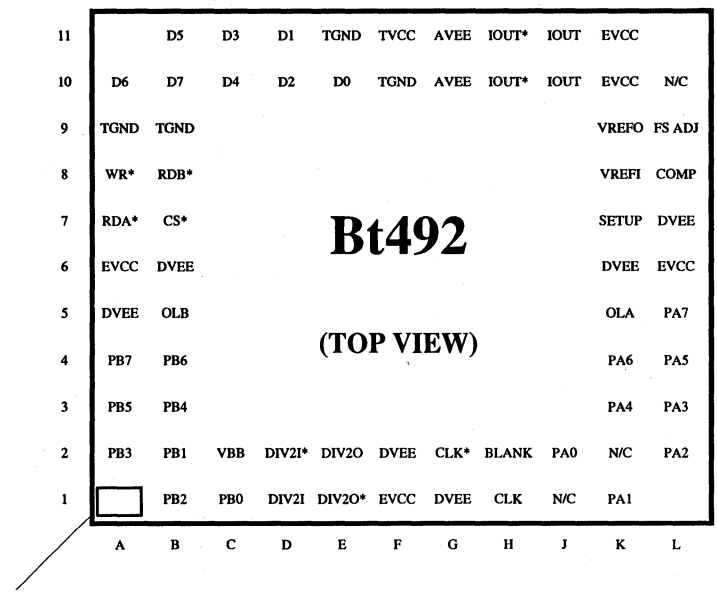
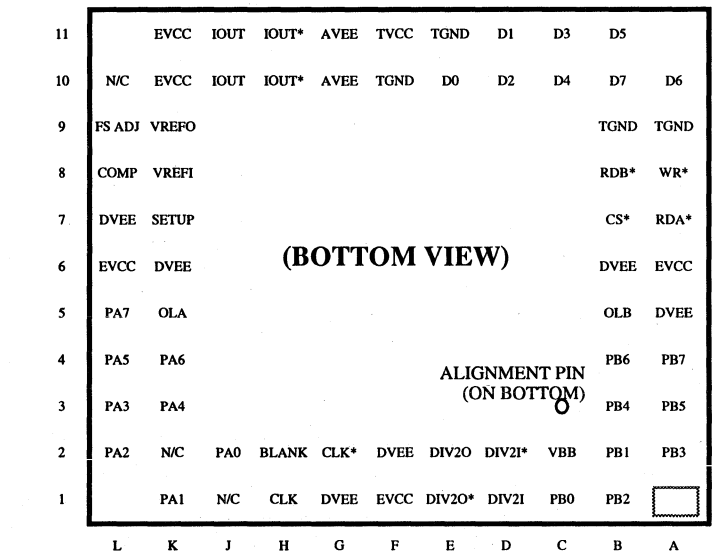
Pin Descriptions (continued)





PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt492 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of AVEE and ECL VCC pins should be as short as possible to minimize inductive ringing.

Sockets

Only flush mount sockets should be used, such as the Advanced Interconnect KS06985TG.

Ground Planes

The ground plane should encompass all Bt492 ground pins, any voltage reference circuitry, power supply bypass circuitry for the Bt492, the analog output traces, and all the digital signal traces leading to the Bt492.

Power Planes

The Bt492 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 4 and 5. This bead should be located within 3 inches of the Bt492.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt492 power pins, any external voltage reference circuitry, and any output amplifiers.

Portions of the regular PCB power and ground planes must not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, another ferrite bead must be installed between the AVEE power pins and the analog power plane, as illustrated in Figures 4 and 5. The ferrite bead must be as close as possible to the AVEE pins.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog-power-plane side of the ferrite bead for the AVEE pins, as illustrated in Figures 4 and 5.

COMP Decoupling

Ceramic chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance.

Digital Signal Interconnect

The digital inputs to the Bt492 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

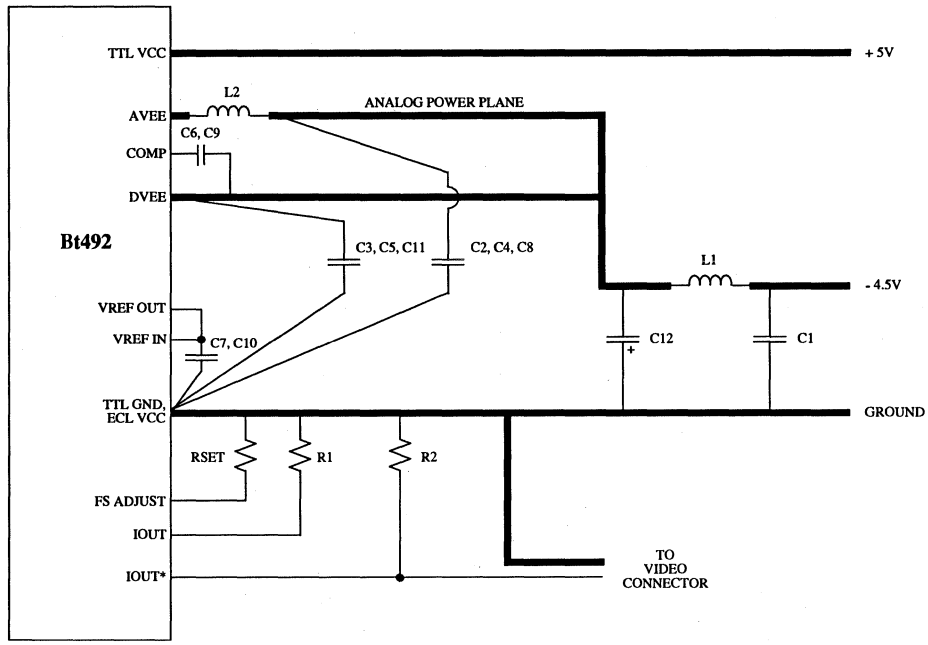
Any termination resistors for the digital inputs should be connected to the regular PCB power plane, or termination and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane rather than the analog power plane, to maximize the high-frequency power supply rejection.

The analog transmission lines must have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)

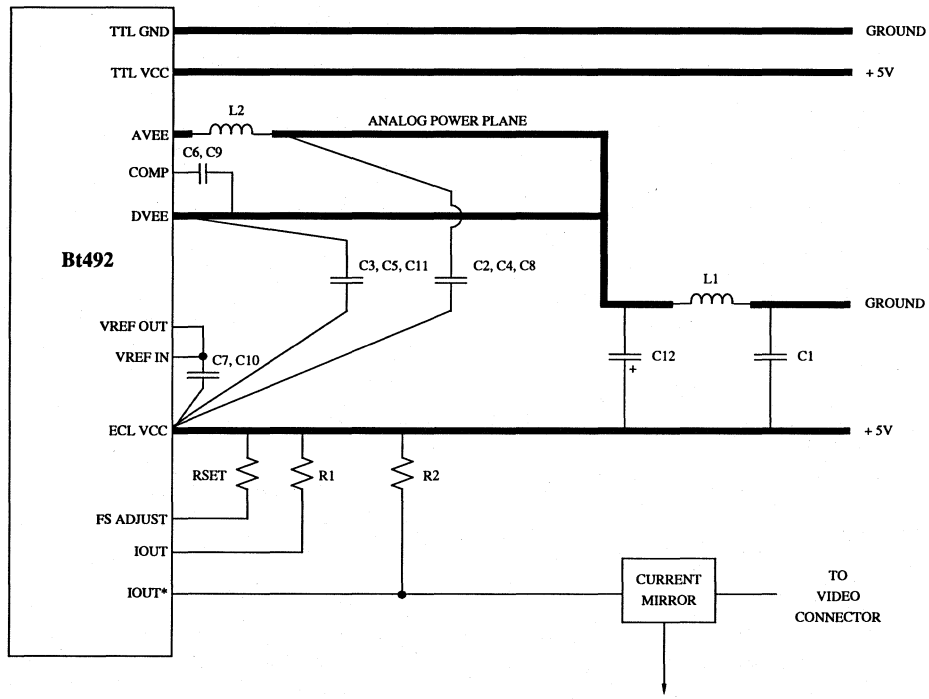


Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8–C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	24.9 Ω 1% metal film resistor	Dale CMF-55C
R2	49.9 Ω 1% metal film resistor	Dale CMF-55C
RSET	732 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt492. R1, R2, and RSET values assume doubly-terminated 50 Ω load on IOUT*.

Figure 4. Typical Connection Diagram and Parts List (Dual Supply Operation).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8–C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	24.9 Ω 1% metal film resistor	Dale CMF-55C
R2	49.9 Ω 1% metal film resistor	Dale CMF-55C
RSET	732 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt492. R1, R2, and RSET values assume doubly-terminated 50 Ω load on IOUT*.

Figure 5. Typical Connection Diagram and Parts List (Single Supply Operation).

Application Information

Terminated ECL Inputs

All ECL inputs of the Bt492 should be terminated with normal ECL termination practices. In addition, all of the ECL digital inputs have internal pulldown junctions. Thus, if an ECL digital input is left floating, it assumes the logical-zero state.

External Voltage Reference

An external voltage reference may be used with the Bt492, as shown in Figure 6. In this instance, the VREF OUT pin should be left floating.

The VREF IN pin still requires bypass capacitors to ECL VCC.

Single-Supply Operation

The Bt492 may be operated from a single +5 V supply when the power supply pins are connected as shown:

TTL VCC = +5 V
TTL GND = 0 V
ECL VCC = +5 V
DVEE, AVEE = 0 V

The current mirror on the analog output is required to reference the video signal to ground rather than +5 V.

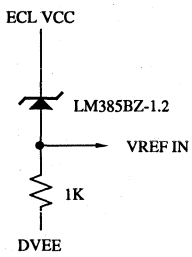


Figure 6. External Voltage Reference.

Differential Clock Inputs

The Clock and Clock* inputs should be terminated using normal ECL termination practices and cross-terminated with 150 Ω to improve the common mode input voltage rejection. See Figure 7.

Using Multiple Bt492s

For color applications, three Bt492s may be used, as illustrated in Figure 8. This example generates 256 simultaneous colors from a 16.8-million color palette and supports a 2k x 2k pixel resolution.

Both the even and odd pixel data require separate shift registers (Bt424s). The MPU TTL address bus is also interfaced to the Bt492 pixel inputs with the Bt424s.

The DIV2OUT–DIV2IN connections generate CLOCK*/2 and ensure the three Bt492s operate in a synchronous fashion. When the timing window for DIV2IN is being analyzed, the propagation delay of the CLOCK and DIV2OUT signals must be included through the transmission lines of the physical layout on the PC board.

Although the Bt492s share the voltage reference and analog power/ground planes, each Bt492 must have its own power supply decoupling, COMP decoupling, VREF IN decoupling, AVEE ferrite bead, RSET resistor, and IOUT termination resistors.

Optimum layout should minimize CLOCK and DIV2 line length. Low dielectric stripline is recommended, and the propagation delays between CLOCK and DIV2 should match as closely as possible.

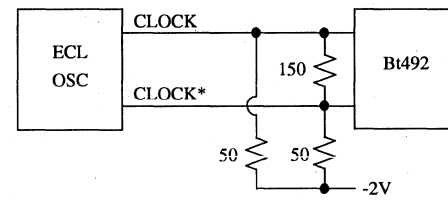


Figure 7. Differential Clock Input Termination.

Application Information (continued)

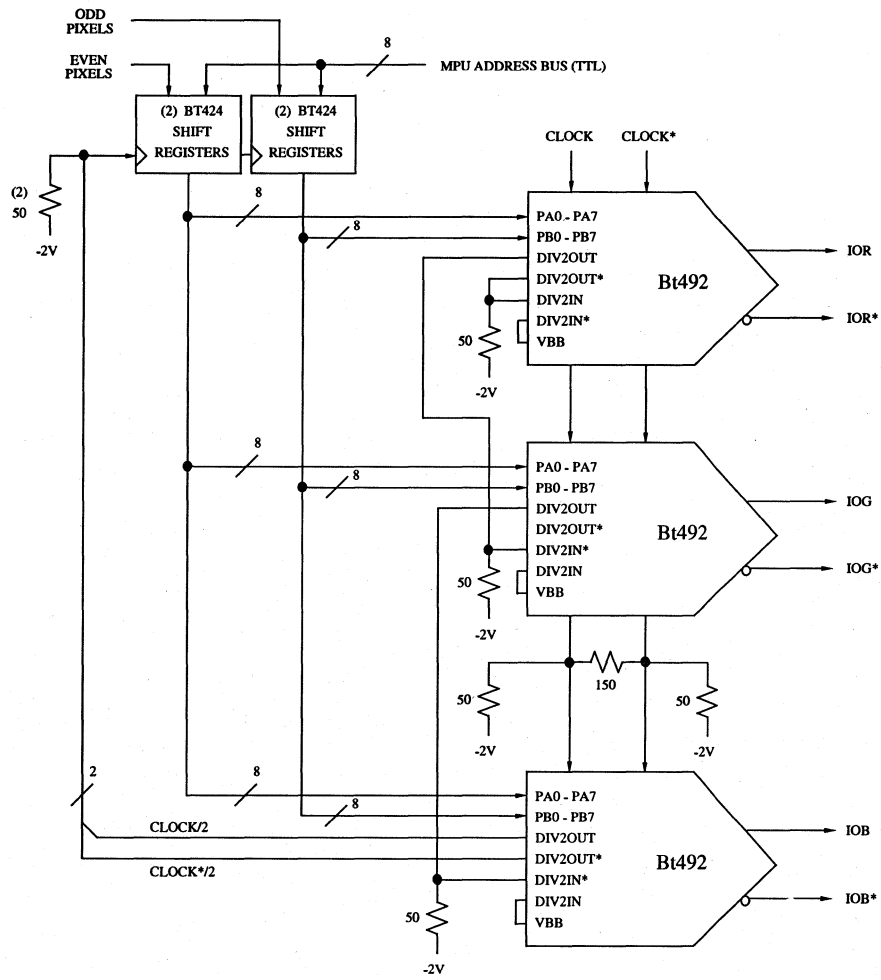


Figure 8. Using Multiple Bt492s.

5

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
ECL Power Supply	DVEE,	–4.2	–4.5	–5.5	V
ECL Ground	AVEE		0		V
TTL Power Supply	ECL VCC	4.75	5	5.25	V
TTL Ground	TTL VCC		0		V
Ambient Operating Temperature	TTL GND	0		+ 70	°C
Output Load	TA		25		Ω
Reference Voltage	RL	–1.15	–1.21	–1.27	V
FS ADJUST Resistor	VREF IN		729		Ω

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL Supply (measured to ECL VCC)	DVEE, AVEE			–6.5	V
TTL Supply (measured to GND)	TTL VCC			+7.0	V
Voltage on Any ECL Input Pin		ECL VCC		DVEE	V
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	V
Analog Output Short Circuit Duration to Any Common			indefinite		
Ambient Operating Temperature		–55		+125	°C
Storage Temperature	TA	–65		+150	°C
Junction Temperature	TS			+175	°C
	TJ				
Soldering Temperature (5 seconds, 1/4 inch from pin)	TSOL			260	°C
Junction to Ambient					
Still Air				28	°C / W
400 LFM				13	°C / W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/2	LSB
Gray Scale Error					
Internal Reference				±10	% Gray Scale
External Reference				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
TTL Digital Inputs					
Input High Voltage	VIH	2.0		TTL VCC +0.5	V
Input Low Voltage	VIL	TTL GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			–700	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		6		pF
TTL Digital Outputs					
Output High Voltage (IOH = –2 mA)	VOH	2.4			V
Output Low Voltage (IOL = 20 mA)	VOL			0.5	V
ECL Digital Inputs					
Input High Voltage	VIH	–1165		–880	mV
Input Low Voltage	VIL	–1810		–1475	mV
Input High Current	IIH			220	µA
Input Low Current	IIL	0.5			µA
Input Capacitance (f = 1 MHz, Vin = VIHmax)	CIN		6		pF
CLOCK, CLOCK* Differential Input Voltage		±400			mV
ECL Digital Outputs					
Output High Voltage	VOH	–1025		–880	mV
Output Low Voltage	VOL	–1810		–1620	mV

See test conditions on next page.

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DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Output					
Gray Scale Current Range		–10		–40	mA
Output Current (Note 1)					
White Level		0	–5	–50	µA
Black Level Relative to White		–25.08	–26.40	–27.72	mA
Blank Level Relative to Black					
SETUP = ECL VCC		0	0	0	mA
SETUP = float		–2.05	–2.16	–2.28	mA
Blank Level Relative to White		–27.13	–28.56	–30	mA
LSB Size			–103.5		µA
Output Compliance	VOC	–1.2		+ 1.5	V
Output Impedance	ROUT		10		K Ω
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Reference Input Current	IREF IN			10	µA
Reference Output Voltage	VREF OUT	–1.15	–1.21	–1.27	V
Reference Output Current	IREF OUT	–200			µA
VREF OUT Tempco			± 75		ppm
VBB Output Voltage (load = 500 µA)	VBB	–1260	–1320	–1380	mV
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 kHz)	PSRR		0.1		% / % Δ AVEE
DVEE + AVEE Supply Current	IEE			455	mA
TTL VCC Supply Current	ICC			100	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full-scale output current, VREF IN = –1.21 V, and SETUP = float. All ECL inputs have 50 Ω to –2.0 V. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: When using internal reference, RSET may require adjustment to meet these limits.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			360	MHz
CS* and Address Setup Time	1	10			ns
CS* and Address Hold Time	2	20			ns
RDx* Asserted to Data Bus Driven	3			10	ns
RDx* Asserted to Data Valid	4			10	ns
RDx* Negated to Data Bus 3-Stated	5			15	ns
WR* Pulse Width Low	6	55			ns
Write Data Setup Time	7	30			ns
Write Data Hold Time	8	5			ns
Pixel and Control Setup Time	9	0			ns
Pixel and Control Hold Time	10	1.5			ns
Clock Cycle Time	11	2.8			ns
Clock Pulse Width High	12	1			ns
Clock Pulse Width Low	13	1			ns
DIV2OUT Delay	14	0.5		1.5	ns
DIV2IN Setup Time (to rising edge of CLOCK)	15	0.5			ns
DIV2IN Hold Time (to rising edge of CLOCK)	16	1			ns
Analog Output Delay	17		2	4	ns
Analog Output Rise/Fall Time				1	ns
Analog Output Settling Time	18		3	5	ns
Clock and Data Feedthrough			tbd		dB
Pipeline Delay		3	3	3	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full-scale output current, VREF IN = –1.21 V, and SETUP = float. ECL input values are –0.95 to –1.69 V with input rise/fall times ≤ 1 ns, measured between the 20-percent and 80-percent points. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. All ECL inputs have 50 Ω to –2.0 V, unless otherwise specified. Analog output load ≤ 10 pF. See timing notes in Figure 11. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Timing Waveforms

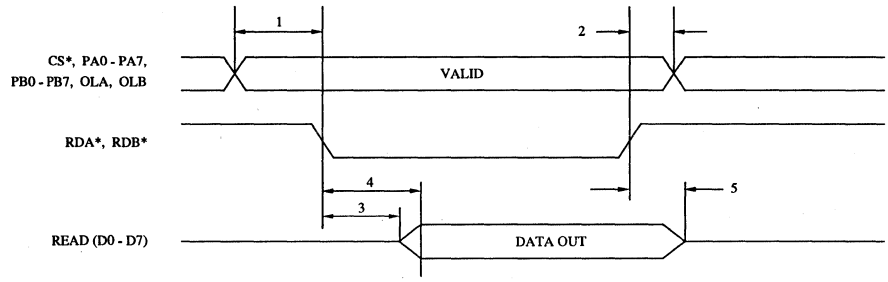


Figure 9. MPU Read Timing.

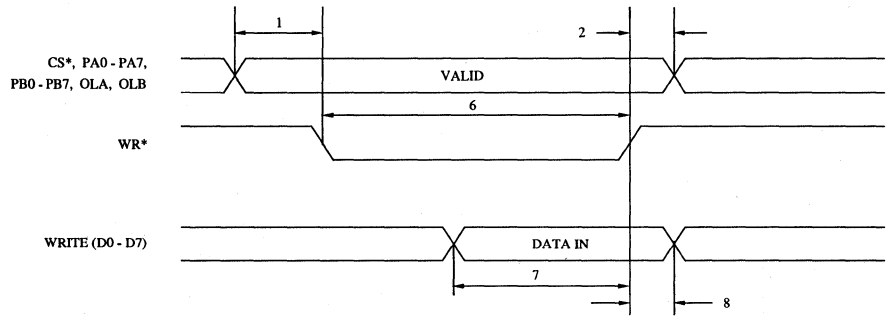
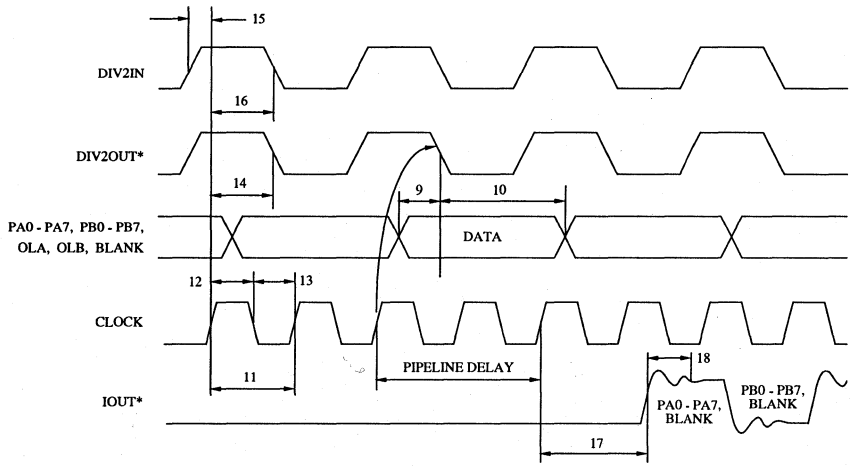


Figure 10. MPU Write Timing.

Timing Waveforms (continued)



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 percent.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 11. Video Input/Output Timing.

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Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt492KG360	360 MHz	68-pin Ceramic PGA with Alignment Pin and Heatsink	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice.

Bt494

160 MHz
Monolithic CMOS
RAMDAC™

Distinguishing Features

- 160 MHz, 110 MHz Operation
- 1:1, 2:1, or 4:1 Multiplexed Pixel Ports
- Pseudo Color or True Color Support
- Double-Buffered Pseudo Color Support
- Three 256 x 8 Color Palette RAMs
- Programmable Setup (0 or 7.5 IRE)
- 2 Overlay Planes
- 2 Cursor Planes
- Input and Output Signature Registers
- JTAG Support
- 169-pin PGA Package

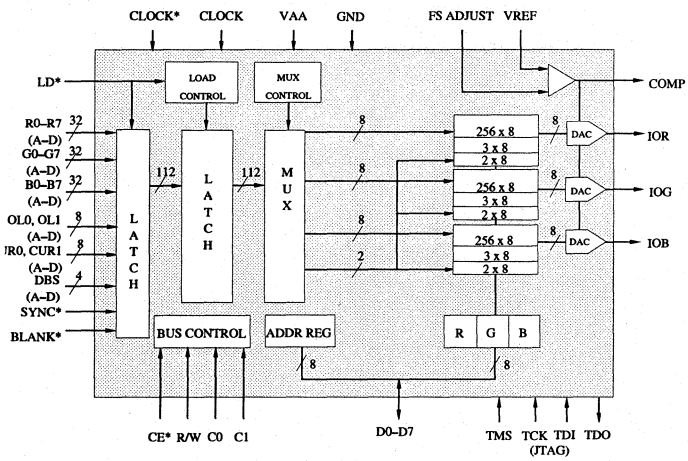
Applications

- High-Resolution Color Graphics
- Medical Imaging
- Visualization
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt463

Functional Block Diagram



Product Description

The Bt494 is a high-performance RAMDAC designed for high-resolution, true-color graphics. It has three 256 x 8 lookup tables with triple 8-bit D/A converters to support 24-bit true color for monitors with up to 1600 x 1280 resolution. The Bt494 also supports single- or double-buffered 8-bit pseudo color. The Bt494 contains two overlay planes and a dedicated two-plane cursor port.

On-chip features include programmable 1:1, 2:1, or 4:1 input multiplexing of the pixels, bit plane masking, and a programmable setup (0 or 7.5 IRE).

The Bt494 supports double-buffered pseudo color by using the DBS input pin to switch on a pixel- by-pixel basis from the red port to the green port.

The Bt494 has significant testability features, including input and output signature analysis registers, and fully supports the Joint Test Action Group (JTAG) specification.

The Bt494 is pin and software compatible to the Bt463 and is offered in a pin grid array package.

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L494001 Rev. A

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt494 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs allow color updating without contention with the display refresh process.

The C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU (Table 1). The 12-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit. ADDR0 and ADDR8 correspond to data bus bit D0. ADDR12–ADDR15 are ignored during MPU write cycles and return logical zeroes when read by the MPU.

The control registers are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When the control registers and the color palette RAM are accessed, the address register increments following a read or write cycle.

Writing/Reading Color Palette RAM

To write color data, the MPU loads the address register with the address of the color palette, overlay palette, or cursor color register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM or cursor color register. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read the color palette RAM or cursor color register, the MPU loads the address register with the address of the color palette RAM location or cursor color register to be read. Reading color data is similar to writing it, except the MPU executes read cycles.

When accessing the cursor color registers, the address register increments to $0102 following a blue read or write cycle. The color palette RAM does not have a wraparound feature after the last valid address. However, any attempt to write past $020F does not affect previous data load cycles. The address register will reset to $0000 after incrementing past $0FFF.

ADDR0–16	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–11)
$0100	10	cursor color 0 (Note 1)
$0101	10	cursor color 1 (Note 1)
$0200	10	ID register ($2C)
$0201	10	command register_0
$0203	10	command register_2
$0205	10	R0–R7 read mask register
$0206	10	G0–G7 read mask register
$0207	10	B0–B7 read mask register
$0208	10	CUR and OL read mask register
$0209	10	R0–R7 blink mask register
$020A	10	G0–G7 blink mask register
$020B	10	B0–B7 blink mask register
$020C	10	CUR and OL blink mask register
$020D	10	test register
$020E	10	input signature register (Note 2)
$020F	10	output signature register (Note 1)
$0220	10	revision register ($A)
$0000–$00FF	11	color palette RAM (Note 1)
$0201	11	overlay color 1 (Note 1)
$0202	11	overlay color 2 (Note 1)
$0203	11	overlay color 3 (Note 1)

Note 1: Requires three read/write cycles.
Note 2: Two out of three valid read/write cycles.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

When accessing the color palette RAM, overlay palette RAM, signature analysis registers, or cursor color registers, the address register increments after every third read/write cycle for each addressable location. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

For 8-bit registers, the address increments after every read/write cycle.

Figure 1 illustrates the MPU read/write timing of the Bt494.

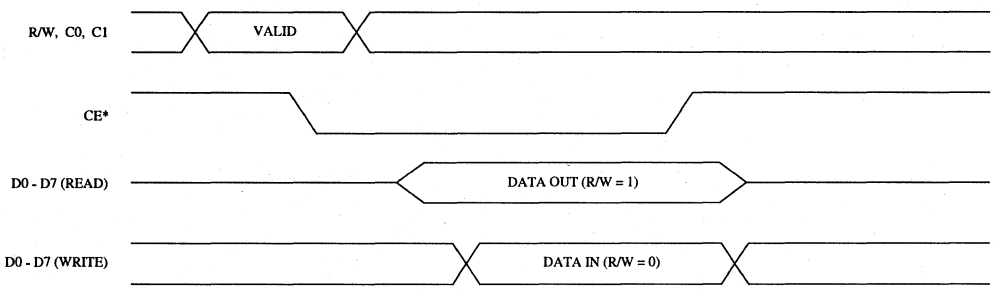

Figure 1. MPU Read/Write Timing.

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Circuit Description (continued)

Frame Buffer Interface

To enable transfer of pixel data from the frame buffer at TTL data rates, the Bt494 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information for either 1, 2, or 4 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 1-, 2-, or 4-pixel resolution. Typically, the LD* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

For 1:1, 2:1, or 4:1 input multiplexing, the Bt494 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until 1, 2, or 4 pixels have been output, at which point the cycle repeats.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK. This enables computation of the LD* signal by externally dividing CLOCK by 2 or 4, independent of the propagation delays of the LD* generation logic. As a result, the pixel, overlay, and cursor data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than three (in 4:1 mode), clock cycles. This LOAD signal transfers the latched pixel, overlay, and cursor data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 1:1 multiplexing is specified, the CLOCK and CLOCK* signals are ignored and pixel data is latched on the rising edge of LD*. If 2:1 multiplexing is specified, only one rising edge of LD* should occur every two clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

Color Palette RAM

The color lookup table consists of three independent 256-entry RAMs.

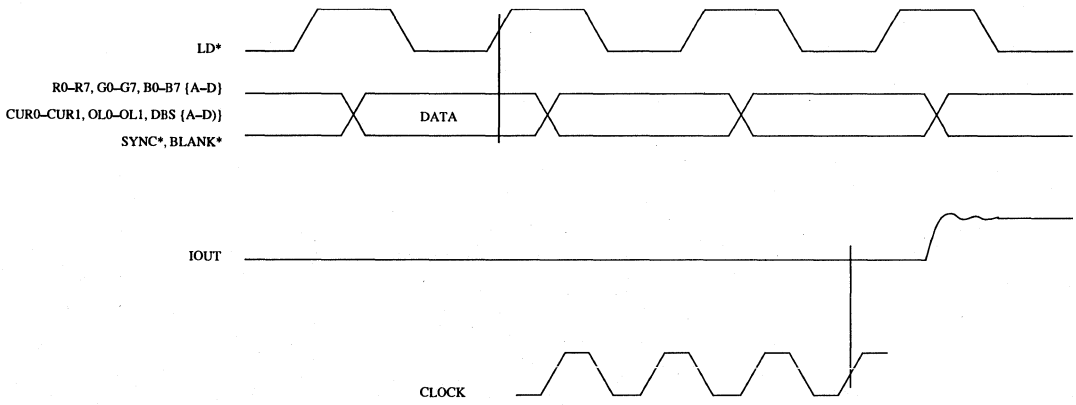


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Video Generation

Every clock cycle, up to 24 bits of color information are presented to the three 8-bit D/A converters.

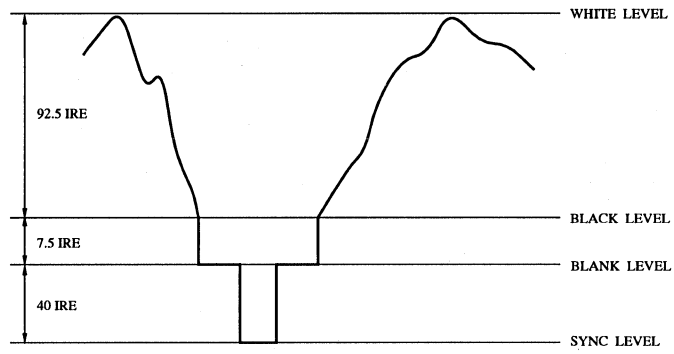
The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 2 and 3 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt494 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveform (SETUP = 7.5 IRE).

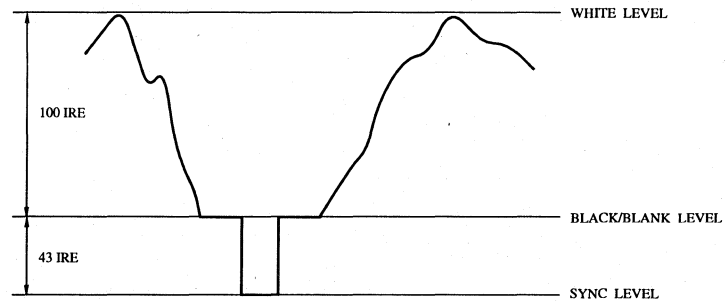
Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 2. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 3. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

Hardware Cursor Interface

Pins CUR0 and CUR1 (A–D) can be used to interface the Bt494 with one or two Bt431 hardware cursor chips. Table 4 contains more details.

CUR1	CUR0	CURSOR COLOR
0	0	RAM Palette or Overlays
0	1	0
1	0	1
1	1	1

Table 4. Cursor Interface Operation.

Overlay Operation

Pins OL0 and OL1 (A–D) provide two-plane normal overlay inputs. Three overlay colors are available. These must be in CLUT RAM address locations: $0201, $0202, and $0203. Refer to Table 5.

OL0	OL1	Overlay Color	RAM Address Location
0	0	—	—
0	1	1	$0201
1	0	2	$0202
1	1	3	$0203

Table 5. Overlay Interface Operation.

Boundary-Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt494 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the JTAG. Conforming to the IEEE P1149.1 *Standard Test Access Port and Boundary Scan Architecture*, the Bt494 has dedicated pins that are used for testability purposes only.

JTAG's approach to testability uses boundary-scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a Boundary-Scan Register (BSR), which applies or captures test data used for functional verification of the RAMDAC. The JTAG approach is particularly useful for board testers that use functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data Input), and TDO (Test Data Out). These four TAP pins can completely verify the RAMDAC. With boundary-scan cells at each digital pin, the Bt494 can apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access to and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry.

The output result is scanned out on the TDO pin and externally checked. The Timing Waveform section contains timing information. While isolating the Bt494 from the other components on the board, the user has easy access to all Bt494 digital pins through the TAP and can perform complete functionality tests without expensive testers.

The bidirectional MPU port is given special attention with respect to JTAG. Because JTAG requires control over each digital pin, an additional Output Enable (OE) function is included in the BSR for the MPU pins. In conjunction with the JTAG instruction, the OE will configure the MPU port as an input or output.

With the JTAG bus, users also have access to a vital portion of the Bt494, the Output Signature Analysis Register (OSAR). See Figure 5. With access to this register, users can easily verify expected video data serially through the JTAG port. The OSAR is located between the lookup table and the inputs to the DACs.

The Power-On Reset (POR) circuitry ensures that the Bt494 initializes each pin to operate in a RAM-DAC mode instead of a JTAG test mode during power-up sequence.

A variety of verification procedures can be performed through the TAP controller. Through a set of eight instructions, the Bt494 can verify board connectivity at all digital pins, generate artificial pixel vectors on chip, check signatures on system pixel streams, and scan vectors in and out of the pixel shifter and signature analysis register. The instructions are accessible through a simple state machine.

Note: Since the boundary scan (JTAG) circuitry is intended for gross functional verification, it is tested and guaranteed operational at VAA >= 5.0 volts and VIL on JTAG pins at 0.6 volts max. Maximum JTAG clock speed (TCK) is 50 MHz.

5

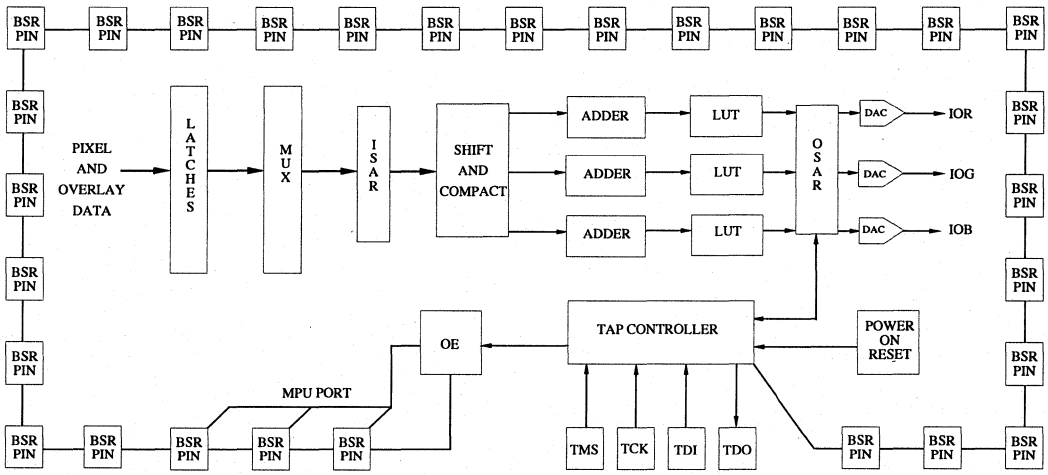


Figure 5. JTAG Block Diagram.

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 2:1 multiplexing

These bits specify whether 1:1, 2:1, or 4:1 multiplexing is to be used for the pixel and overlay inputs. If 2:1 is specified, the {C} and {D} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one half the CLOCK rate. If 4:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fourth the CLOCK rate. If 1:1 is specified, the {B}, {C}, and {D} inputs are ignored.

In the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

The pipeline delay of the Bt494 can be reset to a fixed 13 clock cycles. In this instance, each time the input multiplexing is changed, the Bt494 must be reset again to a fixed pipeline delay.

CR05 Mode select

(0) True color
(1) Pseudo color

This bit specifies whether the chip is operating in true color or pseudo-color mode. When in PC mode, the DBS pin selects either R7–R0 pins (DBS = 0) or B7–B0 pins (DBS = 1) as the pseudo-color pixel port.

CR04 reserved (logical zero)

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off). The counters that determine the blink rate are reset when writing to command register_0. For the blink function to operate properly, SYNC* must toggle only once on horizontal retrace and two times or more on vertical retrace.

CR01, CR00 reserved (logical zero)

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. A 0 IRE specifies that the black and blank levels are the same.
CR25–CR23	reserved (logical zero)	
CR22	Input SAR capture selection (0) lower 16 bits (1) upper 16 bits	This bit specifies whether the 16-bit input signature analysis register (SAR) should capture the lower or upper 16 bits of the pixel path. When CR22 is selected as a logical one, 3 of the upper 16 bits will be ground. The input SAR is guaranteed operational only for the 110 MHz speed grade on the current revision.
CR21	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all signature analysis register (SAR) clocking. Logical zero is the normal mode with pixel position (A, B, C, or D) determined by the test register. Logical one is a special mode for chip testing. (In this instance, SAR operation is not guaranteed for clock rates above 30 MHz.)
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The SARs are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt494, the value read by the MPU will be $2C. Data written to this register is ignored.

Pixel Read Mask Register

The 24-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. D0 corresponds to R0, B0, G0, and CUR0.

Pixel Blink Mask Register

The 24-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. D0 corresponds to R0, B0, G0, and CUR0. For the blink function to operate properly, SYNC* must toggle no more than once on horizontal retrace and more than once on vertical retrace.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt494. The 4 most significant bits signify the revision letter in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored.

Internal Registers (continued)

Red, Green, and Blue Output Signature Analysis Registers (OSAR)

Signature Operation

These three 8-bit signature analysis registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the OSARs while BLANK* is a logical zero to load the seed value. The OSARs use data loading into the output DACs to calculate the signatures. JTAG logic can access the OSAR independently of the MPU operation. MPU accesses to the OSARs require one address register load to address $020F, followed by three reads or writes to the red, green, and blue signature registers. D0 corresponds to R0, G0, and B0.

When a test display is loaded into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

Data-Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

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Input Signature Analysis Registers (ISAR)

Signature Operation

This 16-bit signature analysis register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the ISAR while BLANK* is a logical zero to load the seed value. The ISAR uses R0–R7, G0–G7, B0–B7, CUR0–CUR1, OL0–OL1, and DBS (selected by command bit CR22) to calculate the signatures. When CR22 is a logical one, the upper 16 bits are used. B0–B7, CUR0–CUR1, OL0–OL1, DBS, and the remaining 3 bits are ground (logical zero). The 16 bits of data latched in the ISAR may be masked (forced low) by the read mask registers. MPU accesses to the ISAR require one address register load to $020E, followed by three reads or writes to lower byte, upper byte, and dummy access. D0 corresponds to R0, B0, G0, and CUR0.

When a test display is loaded into the frame buffer, a given value for the ISAR will be returned if all circuitry is working properly.

Note: The input signature analysis register is operational at frequencies < 120 MHz only.

Data-Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the ISAR changes slightly. Rather than determining the signature, it just captures and holds the 16 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the ISAR captures the 16 bits of pixel data addressing the color palette RAM. As only 1 of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Internal Registers (continued)

Test Register

This 8-bit register is used for testing the Bt494. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 2:1 pixel multiplexing is specified, signature analysis is done on every second pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel. D0–D2 are used for 2:1 and 4:1 multiplexing to specify whether to use the A, B, C, or D pixel inputs, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	reserved
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	—	—
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables comparison of that function; the result is D3. The output levels of the DACs should be constant for 5 µs to allow enough time for detection. The capture occurs over one LD* period set by a logical one at any of the pixel pins B0A, B0B, B0C, or B0D.

For normal operation, D4–D7 must be logical zeroes.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as detailed in Tables 2 and 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 2 and 3; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The R0–R7 {A–D}, G0–G7 {A–D}, OL0–OL1 {A–D}, CUR0–CUR1 {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is the output clock (1:1 multiplex mode) or is one half or one fourth of CLOCK, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
R0-R7, G0-G7, B0-B7 {A–D}	Red, green, and blue pixel select inputs (TTL compatible). If nonzero data exists in the assigned overlay input port, then pixel data inputs are ignored. Either 1, 2, or 4 consecutive pixels (up to 24 bits per pixel) are input through this port. All 4 pixels (96 bits) are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 1, 2, or 4 pixels have been output, at which point the cycle repeats.
OL0, OL1 {A–D}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*. When they are nonzero, the overlay palette RAM is accessed and the R0–R7, G0–G7, and B0–B7 {A–D} inputs are ignored. Overlay information (up to 2 bits per pixel) for either 1, 2, or 4 consecutive pixels is input through this port. Unused inputs should be connected to GND. If nonzero data exists on CUR0 and CUR1, overlay input pixels will be ignored.
CUR0, CUR1 {A–D}	Cursor inputs (TTL compatible). If these inputs are nonzero, the color and overlay input pixels are ignored; one of two cursor colors is selected. Unused inputs should be connected to GND.
DBS{A–D}	Double buffer select (TTL compatible). If the Bt494 is in pseudo-color mode, a zero value causes the R7–R0 pins to act as the pixel input. If a one value, G7–G0 pins act as the pixel input. This pin allows double-buffered pseudo-color operation on a pixel-by-pixel basis.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
TCK	Test Clock (TTL compatible). It is used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When JTAG operations are not being performed, this pin is pulled low by internal circuitry.
TMS	Test Mode Select (TTL compatible). It is a JTAG input pin whose transitions drive the JTAG state machine through its sequences. When JTAG operations are not being performed, this pin is pulled high by internal circuitry.
TDI	Test Data Input (TTL compatible). It is a JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When JTAG operations are not being performed, this pin is pulled high by internal circuitry.
TDO	Test Data Output (TTL compatible). It is a JTAG output pin used to verify test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences, and will be three-stated at all other times. When JTAG operations are not being performed, this pin should be left floating.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Pin Descriptions (continued)

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>GND</td><td>Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>COMP</td><td>Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (see Figure 6 in the PC Board Layout Considerations section). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>FS ADJUST</td><td>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (see Figure 6). The IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

RSET (Ω) = K1 * VREF (V) / IOG (mA)

The full-scale output current on IOR and IOB for a given RSET is:

IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)

where K1 and K2 are defined as:

<table><tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr><tr><td>7.5 IRE</td><td>K1 = 11,294</td><td>K2 = 8,067</td></tr><tr><td>0 IRE</td><td>K1 = 10,684</td><td>K2 = 7,457</td></tr></table></td></tr>
<tr><td>VREF</td><td>Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 6, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CLOCK,
CLOCK*</td><td>Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CE*</td><td>Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches must be avoided on this edge-triggered input.</td></tr>
<tr><td>R/W</td><td>Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.</td></tr>
<tr><td>C0, C1</td><td>Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as shown in Table 1. They are latched on the falling edge of CE*.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
</table>

Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
BLANK*	J1
SYNC*	H1
LD*	H3
CLOCK*	J3
CLOCK	J2
R0A	F2
R0B	G3
R0C	F1
R0D	G1
R1A	F3
R1B	D1
R1C	E2
R1D	E1
R2A	C2
R2B	B1
R2C	D2
R2D	C1
R3A	C3
R3B	D3
R3C	E3
R3D	B2
R4A	A1
R4B	B3
R4C	C4
R4D	D4
R5A	A3
R5B	C5
R5C	A2
R5D	B4
R6A	A5
R6B	B6
R6C	A4
R6D	B5
R7A	A7
R7B	C7
R7C	A6
R7D	C6
G0A	A9
G0B	B8
G0C	A8
G0D	B7

Signal	Pin Number
G1A	A10
G1B	B10
G1C	B9
G1D	C10
G2A	A12
G2B	C11
G2C	A11
G2D	B11
G3A	A14
G3B	B12
G3C	A13
G3D	C12
G4A	A16
G4B	C13
G4C	A15
G4D	B13
G5A	C14
G5B	B15
G5C	A17
G5D	B14
G6A	D15
G6B	B16
G6C	E15
G6D	C15
G7A	D16
G7B	C17
G7C	C16
G7D	B17
B0A	T16
B0B	T17
B0C	R16
B0D	R17
B1A	R15
B1B	R14
B1C	P15
B1D	U17
B2A	T14
B2B	U15
B2C	T15
B2D	U16

Signal	Pin Number
B3A	T13
B3B	U13
B3C	R13
B3D	U14
B4A	R12
B4B	U11
B4C	T12
B4D	U12
B5A	T11
B5B	U9
B5C	R11
B5D	U10
B6A	R10
B6B	U8
B6C	T10
B6D	T9
B7A	T7
B7B	U6
B7C	T8
B7D	U7
CUR0A	R6
CUR0B	U4
CUR0C	R7
CUR0D	U5
CUR1A	T5
CUR1B	U2
CUR1C	T6
CUR1D	U3
OL0A	T4
OL0B	R4
OL0C	R5
OL0D	U1
OL1A	R3
OL1B	N3
OL1C	T3
OL1D	T1
TMS	D17
TCK	E16
TDI	E17
TDO	F17

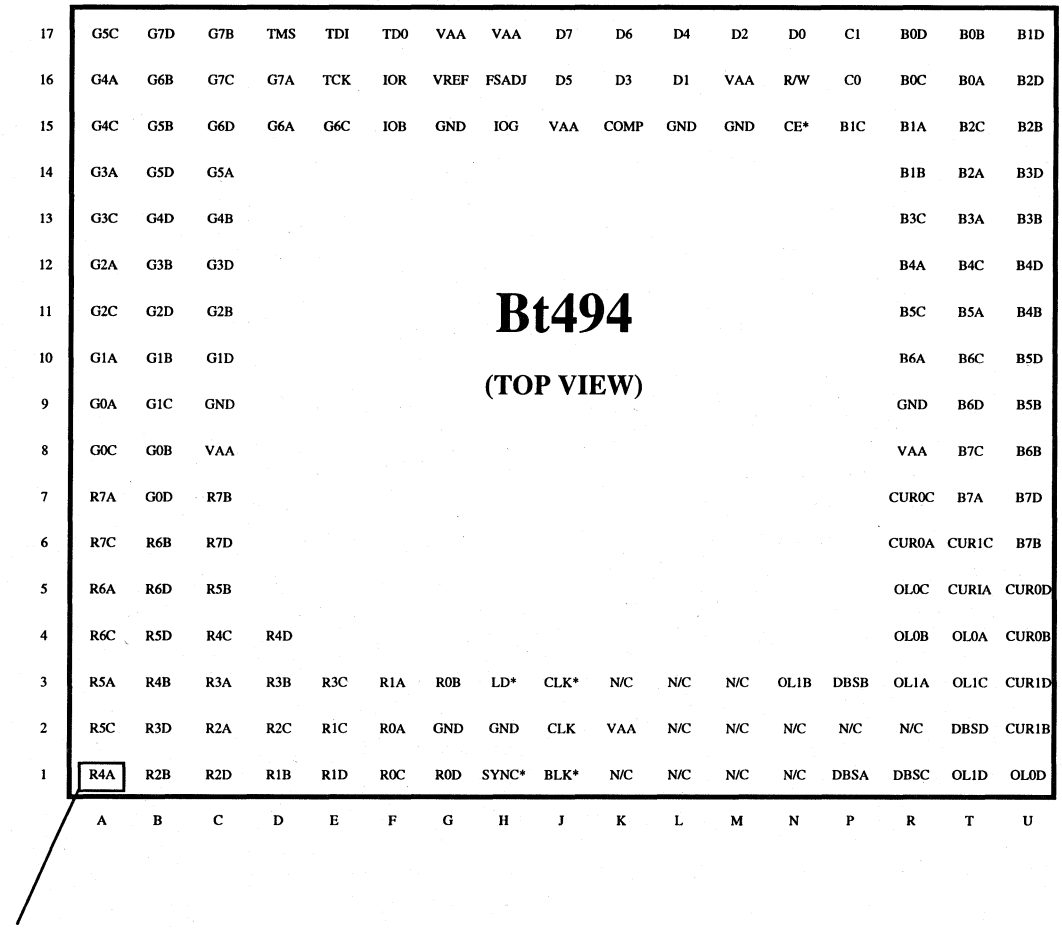
Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
DBSA	P1
DBSB	P3
DBSC	R1
DBSD	T2
D0	N17
D1	L16
D2	M17
D3	K16
D4	L17
D5	J16
D6	K17
D7	J17

Signal	Pin Number
IOR	F16
IOG	H15
IOB	F15
COMP	K15
FS ADJUST	H16
VREF	G16
CE*	N15
R/W	N16
C1	P17
C0	P16

Signal	Pin Number
VAA	C8
VAA	G17
VAA	H17
VAA	J15
VAA	K2
VAA	R8
VAA	M16
GND	C9
GND	G2
GND	G15
GND	H2
GND	L15
GND	M15
GND	R9
N/C	M1
N/C	P2
N/C	N1
N/C	R2
N/C	L1
N/C	N2
N/C	L3
N/C	M3
N/C	K1
N/C	L2
N/C	K3
N/C	M2

Pin Descriptions (continued)—169-pin PGA Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
17	G5C	G7D	G7B	TMS	TDI	TD0	VAA	VAA	D7	D6	D4	D2	D0	C1	B0D	B0B	B1D
16	G4A	G6B	G7C	G7A	TCK	IOR	VREF	FSADJ	D5	D3	D1	VAA	R/W	C0	B0C	B0A	B2D
15	G4C	G5B	G6D	G6A	G6C	IOB	GND	IOG	VAA	COMP	GND	GND	CE*	B1C	B1A	B2C	B2B
14	G3A	G5D	G5A												B1B	B2A	B3D
13	G3C	G4D	G4B												B3C	B3A	B3B
12	G2A	G3B	G3D												B4A	B4C	B4D
11	G2C	G2D	G2B												B5C	B5A	B4B
10	G1A	G1B	G1D												B6A	B6C	B5D
9	G0A	G1C	GND												GND	B6D	B5B
8	G0C	G0B	VAA												VAA	B7C	B6B
7	R7A	G0D	R7B												CUR0C	B7A	B7D
6	R7C	R6B	R7D												CUR0A	CUR1C	B7B
5	R6A	R6D	R5B												OL0C	CURIA	CUR0D
4	R6C	R5D	R4C	R4D											OL0B	OL0A	CUR0B
3	R5A	R4B	R3A	R3B	R3C	R1A	R0B	LD*	CLK*	N/C	N/C	N/C	OL1B	DBSB	OL1A	OL1C	CUR1D
2	R5C	R3D	R2A	R2C	R1C	R0A	GND	GND	CLK	VAA	N/C	N/C	N/C	N/C	N/C	DBSD	CUR1B
1	R4A	R2B	R2D	R1B	R1D	R0C	R0D	SYNC*	BLK*	N/C	N/C	N/C	N/C	DBSA	DBSC	OL1D	OL0D

Pin Descriptions (continued)—169-pin PGA Package

	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
17	B1D	B0B	B0D	C1	D0	D2	D4	D6	D7	VAA	VAA	TD0	TDI	TMS	G7B	G7D	G5C
16	B2D	B0A	B0C	C0	R/W	VAA	D1	D3	D5	FSADJ	VREF	IOR	TCK	G7A	G7C	G6B	G4A
15	B2B	B2C	B1A	B1C	CE*	GND	GND	COMP	VAA	IOG	GND	IOB	G6C	G6A	G6D	G5B	G4C
14	B3D	B2A	B1B												G5A	G5D	G3A
13	B3B	B3A	B3C												G4B	G4D	G3C
12	B4D	B4C	B4A												G3D	G3B	G2A
11	B4B	B5A	B5C					**Bt494**							G2B	G2D	G2C
10	B5D	B6C	B6A												G1D	G1B	G1A
9	B5B	B6D	GND					**(BOTTOM VIEW)**							GND	G1C	G0A
8	B6B	B7C	VAA												VAA	G0B	G0C
7	B7D	B7A	CUR0C												R7B	G0D	R7A
6	B7B	CUR1C	CUR0A												R7D	R6B	R7C
5	CUR0D	CURIA	OL0C												R5B	R6D	R6A
4	CUR0B	OL0A	OL0B											R4D	R4C	R5D	R6C
3	CUR1D	OL1C	OL1A	DBSB	OL1B	N/C	N/C	N/C	CLK*	LD*	R0B	R1A	R3C	R3B	R3A	R4B	R5A
2	CUR1B	DBSD	N/C	N/C	N/C	N/C	N/C	VAA	CLK	GND	GND	R0A	R1C	R2C	R2A	R3D	R5C
1	OL0D	OL1D	DBSC	DBSA	N/C	N/C	N/C	N/C	BLK*	SYNC*	R0D	R0C	R1D	R1B	R2D	R2B	R4A

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt494, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16). This application note can be found in Brooktree's *Applications Handbook.*

The layout should be optimized for lowest noise on the Bt494 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possiple, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt494 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt494 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 6. This bead should be located within 3 inches of the Bt494. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 6 is for low-frequency power supply ripple; the 0.1 µF and 0.01-µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

PC Board Layout Considerations (continued)

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

Digital Signal Interconnect

The digital inputs to the Bt494 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt494 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt494 to minimize reflections. Unused analog outputs should be connected to GND.

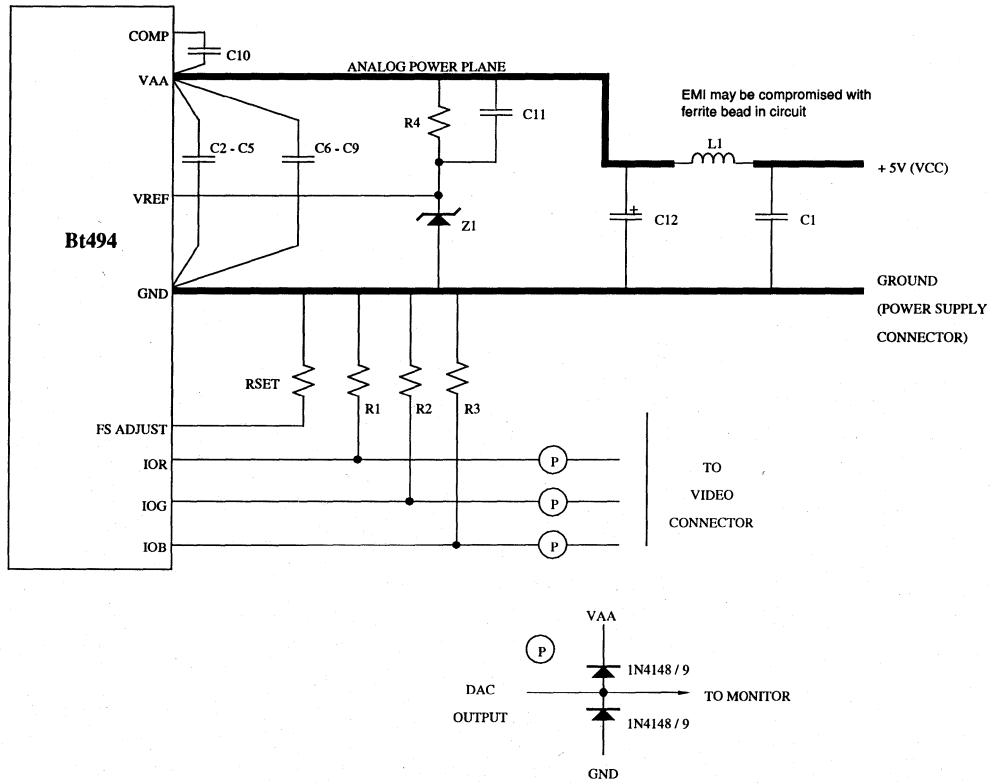
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt494 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111 (Note 1)
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt494.

Note 1: Or equivalent only.

Figure 6. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt494 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 7.)

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt494 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by two or four (depending on whether 2:1 or 4:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal only if fixed pipeline is not required. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt494 is being used, it is recommended that the Bt438 or Bt440 Clock Generator Chip be used to generate the clock and load signals. It supports 4:1 input multiplexing of the Bt494 and will also optionally set the pipeline delay of the Bt494 to 9 clock cycles. The Bt438 may also be used to interface the Bt494 to a TTL clock. Figure 7 illustrates use of the Bt438 with the Bt494.

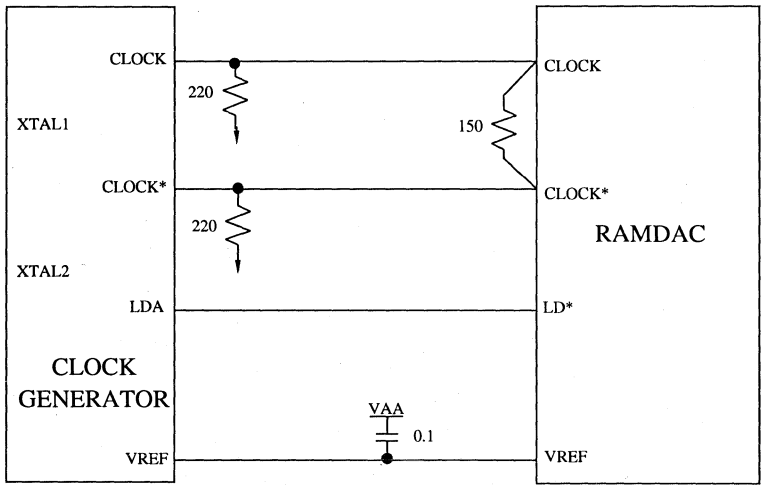


Figure 7. Generating the Bt494 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt494, although fixed after a power-up condition, may be anywhere from 7–11 clock cycles. The Bt494 contains additional circuitry enabling the pipeline delay to be fixed at 9 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt494.

To reset the Bt494, it should be powered-up with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

Resetting the Bt494 to a 9-clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt494s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask registers should be $00. Blinking may be done under software control via the read mask registers.

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt494

The Bt494 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Registers (Signature Mode)

The input signature register is 16 bits wide, capturing pixel information prior to the lookup tables. Since the pixel path is 24 bits wide, the lower or upper 16 bits are selected for capture via command bit CR22.

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 16-bit or 24-bit wide linear feedback shift register on each succeeding pixel that is latched. It is important to note that in either the 2:1 or 4:1 multiplexed modes, the SARs latch only one pixel per "load group." Thus, the SARs are operating only on every second or fourth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, or D) is latched for generating new signatures by setting bits D0–D2 in the test register.

In 1:1 mux mode, the SARs will generate signatures on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (test register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt494 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt494 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 16-bit or 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, for example, one scan-line or one frame buffer's worth of pixels. Then, at the succeeding blank state, the resultant 16-bit or 24-bit signature canbe read out by the MPU. The 24-bit signature register data is a result of the

same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 2:1 or 4:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, or D—being selected.

It is not simple to describe algorithmically the specific linear feedback shift operation used in the Bt494. The linear feedback configurations are shown in Figures 8 and 9.

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Registers (Data Strobe Mode)

Setting command bit CR20 to a logic one puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt494. The levels of most inputs do not matter *except* that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs. Likewise, the input SAR may be read with 2 MPU reads.

In general, the color read-out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (1, 2, or 4 periods), then hold all pixel-related inputs and perform the three MPU reads as described. This process is best done on a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt494 is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register. The capture occurs over one LD* period set by a logic one at pixel port B0 (A–D).

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

Application Information (continued)

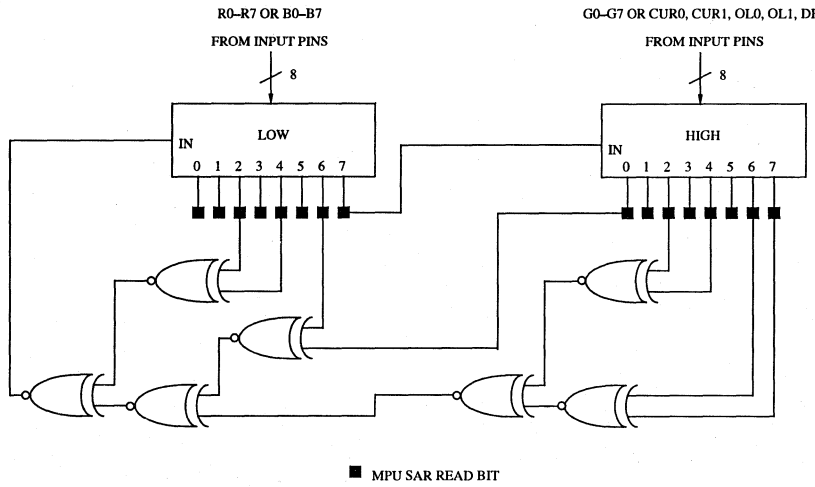


Figure 8. Input Signature Analysis Register Circuit.

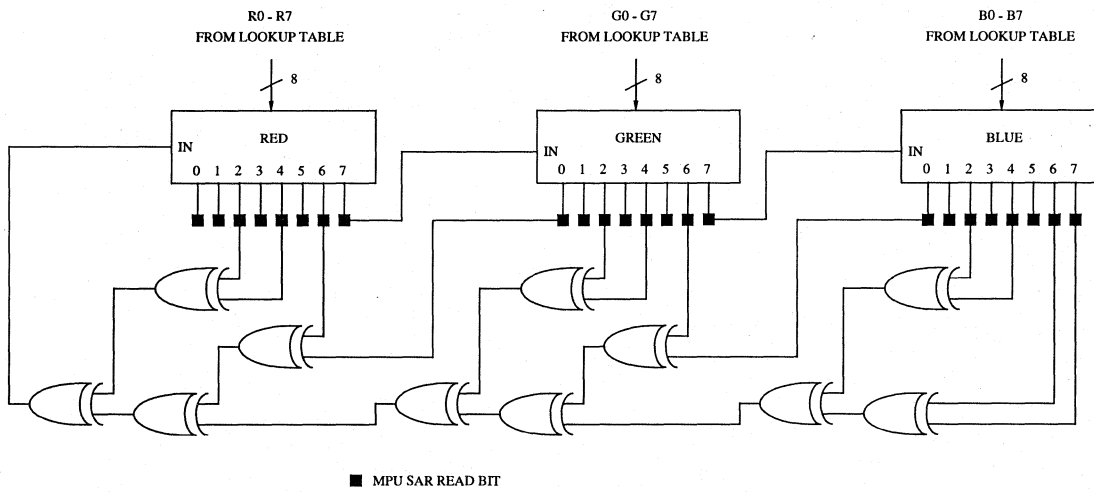


Figure 9. Output Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt494

Following a power-on sequence, the Bt494 must be initialized. This sequence will configure it as follows:

- 4:1 multiplexed true-color operation
- 2 overlay planes on OL0, OL1
- sync enabled on IOG, 7.5 IRE blanking pedestal
- 2 cursor planes on CUR0, CUR1

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $00 to reserved location	10
Write $C0 to command register 2	10
Write $00 to reserved location	10
Write $FF to pixel read mask register R0- R7	10
Write $FF to pixel read mask register G0–G7	10
Write $FF to pixel read mask register B0–B7	10
Write $FF to pixel read mask register CUR & OL	10
Write $00 to pixel blink mask register R0- R7	10
Write $00 to pixel blink mask register G0–G7	10
Write $00 to pixel blink mask register B0–B7	10
Write $00 to pixel blink mask register CUR & OL	10
Write $00 to test register	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $0FF)	11
Write green data to RAM (location $0FF)	11
Write blue data to RAM (location $0FF)	11

Cursor Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10

Overlay Palette RAM Initialization (Note 1)

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $201)	11
Write green data to RAM (location $201)	11
Write blue data to RAM (location $201)	11
Write red data to RAM (location $202)	11
Write green data to RAM (location $202)	11
Write blue data to RAM (location $202)	11
Write red data to RAM (location $203)	11
Write green data to RAM (location $203)	11
Write blue data to RAM (location $203)	

Note 1: The unused overlay palette locations are: $204–$20F.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
PGA	TJ			+170	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			80	µA
Input Low Current (Vin = 0.4 V)	IIL			–80	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	15	pF
Clock Inputs (CLOCK, CLOCK*)				6	
Differential Input Voltage	ΔVIN	0.6		1	V
Input High Current (Vin = 4.0V)	IKIH			–1	µA
Input Low Current (Vin = 0.4 V)	IKIL			15	µA
Input Capacitance (f = 1 MHz, Vin = 4.0V)	CKIN		4		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = 400 µA)	VOH	2.4		0.4	V
Output Low Voltage (IOL = 3.2 mA)	VOL			10	V
3-state Current	IOZ				µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		90		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note: All JTAG DC parameters are tested to a minimum VAA = 5.0 volts wth VIL on JTAG pins at 0.6 volts max.

A C Characteristics

Parameter	Symbol	Min/Typ/ Max	160 MHz	135 MHz	110 MHz	Units
Clock Rate	Fmax	max	160	135	110	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	67.5	67.5	55	MHz
2:1 multiplexing		max	67.5	67.5	55	MHz
4:1 multiplexing		max	40	33.75	27.5	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	15	15	15	ns
CE* Low Time	3	min	50	50	50	ns
CE* High Time	4	min	25	25	25	ns
CE* Asserted to Data Bus Driven	5	min	7	7	7	ns
CE* Asserted to Data Valid	6	max	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	20	20	20	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	3	3	3	ns
TMS, TDI Setup Time	10	min	8	8	8	ns
TMS, TDI Hold Time	11	min	6	6	6	ns
TCK Low Time	12	min	10	10	10	ns
TCK High Time	13	min	10	10	10	ns
TCK Asserted to TDO Driven	14	min	5	5	5	ns
TCK Asserted to TDO Valid	15	max	20	20	20	ns
TCK Negated to TDO 3-Stated	16	max	20	20	20	ns
Pixel and Control Setup Time	17	min	3	3	3	ns
Pixel and Control Hold Time	18	min	2	2	2	ns
Clock Cycle Time	19	min	6.25	7.4	9.09	ns
Clock Pulse Width High Time	20	min	2.8	3.2	4	ns
Clock Pulse Width Low Time	21	min	2.8	3.2	4	ns
LD* Cycle Time	22					
1:1 multiplexing		min	14.81	14.81	18.18	ns
2:1 multiplexing		min	14.81	14.81	18.18	ns
4:1 multiplexing		min	25	29.63	36.36	ns
LD* Pulse Width High Time	23					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	6	6	8	ns
4:1 multiplexing		min	10	12	15	ns
LD* Pulse Width Low Time	24					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	6	6	8	ns
4:1 multiplexing		min	10	12	15	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	160 MHz	135 MHz	110 MHz	Units
Analog Output Delay	25	typ	25	25	25	ns
Analog Output Rise/Fall Time	26	typ	1.5	1.5	1.5	ns
Analog Output Settling Time	27	max	8	8	8	ns
Clock and Data Feedthrough		typ	tbd	tbd	tbd	dB
Glitch Impulse (Note 1)		typ	50	50	50	pV – sec
DAC-to-DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	7	7	7	Clocks
		max	11	11	11	Clocks
VAA Supply Current (Note 1)	IAA	typ	400	380	365	mA
		max	tbd	tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF, D0–D7 output load ≤75 pF. See the timing dimensions and notes in Figures 10–12. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 1: At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.
Note 2: All JTAG AC parameters are tested to a minimum VAA = 5.0 volts withVIL on JTAG pins at 0.6 volts max.

Timing Waveforms

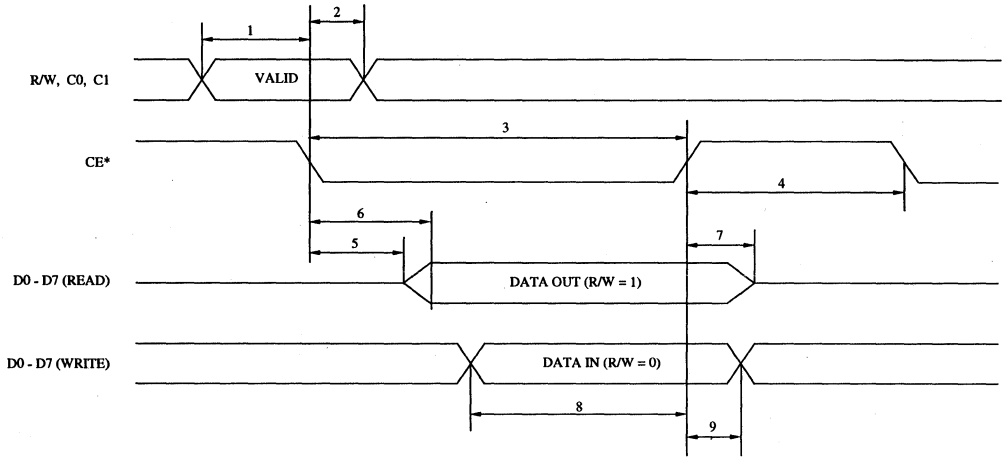
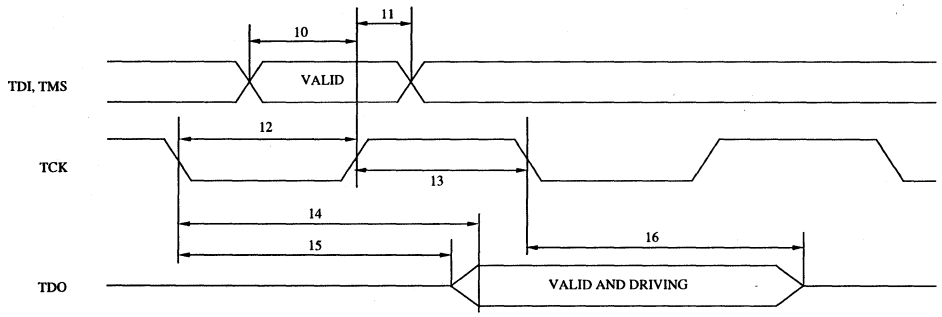


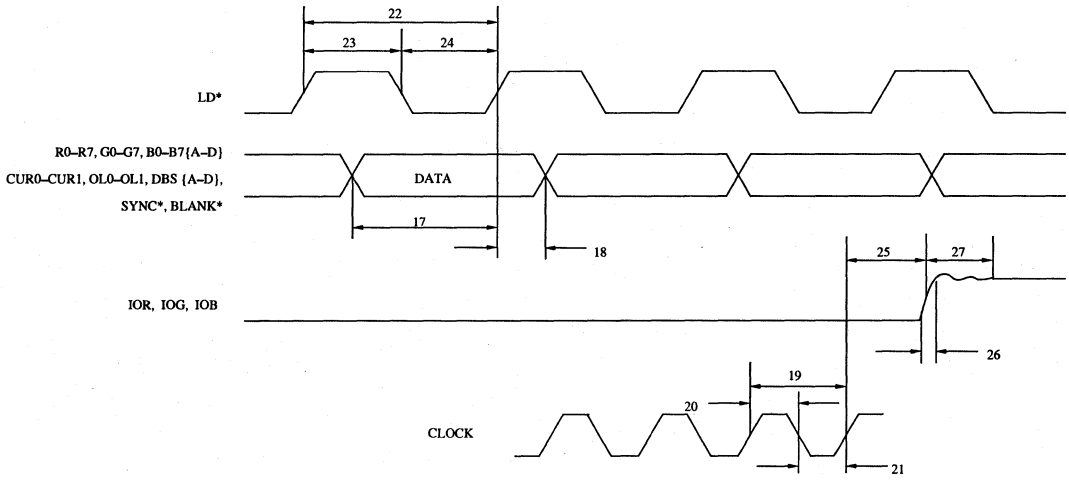
Figure 10. MPU Read/Write Timing Dimensions.



Note 1: TMS and TDI are sampled on the rising edge of TCK.
Note 2: TDO changes after the falling edge of TCK.

Figure 11. JTAG Timing.

Timing Waveforms



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1LSB.

Note 3: Output rise/fall time is measured between 10 percent and 90 percent points of full-scale transition.

Figure 12. Video Input/Output Timing.

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Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt494KG135	135 MHz	169-pin PGA	0° to +70° C
Bt494KG110	110 MHz	169-pin PGA	0° to +70° C
Bt494KG160	160 MHz	169-pin PGA	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt496

100 MHz
Monolithic CMOS
256 x 9 Triple Color Palette
CMYK/RGB RAMDAC™

Distinguishing Features

- CMYK-to-RGB Conversion
- 100 MHz Operation
- 4:1–128:1 Multiplexed Pixel Port
- Three 256 x 9 Color Palette RAMs
- 1x to 16x Integer Zoom Support
- 1, 2, 4, 8, 16, or 32 Bits per Pixel
- Pixel Panning Support
- Simultaneous Support of Zoom, Panning, and Pixel Unpacking
- Programmable Setup (0 or 7.5 IRE)
- 9-Bit DACs
- VRAM Clock Generation
- TTL SYNC Output
- 207-pin PGA Package

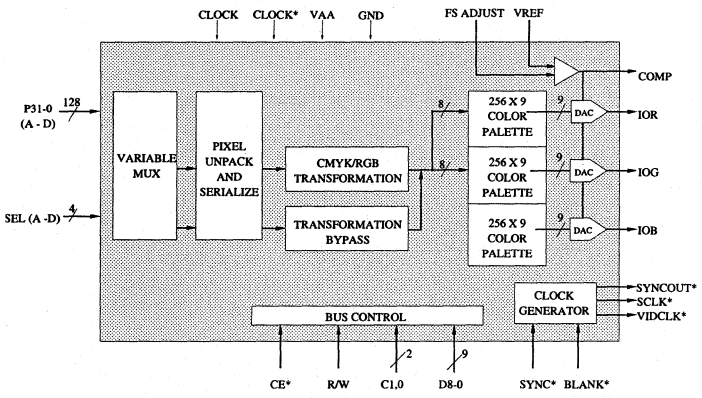
Applications

- Printer Prepress
- Desktop Color
- High-Resolution Color Graphics

Benefits

- Smaller Boardspace
- Ease of Design with Turnkey Solution
- Provides New Capabilities to End Customers

Functional Block Diagram



Product Description

The Bt496 triple 9-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics used in printer prepress and desktop color applications. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing to the frame buffer, while maintaining the 100 MHz video data rates required for sophisticated color graphics.

The CMYK-to-RGB transformation block allows the frame buffer to manipulate data in the CMYK color space while the high-resolution monitor continues to display the image in RGB color space.

On-chip features include three 256 x 9 color palette RAMs, 4:1 input multiplexing of the pixel port, bit plane masking, programmable setup (0 or 7.5 IRE), pixel panning support, 1x to 16x integer zoom support, and CMYK-to-RGB color space conversion.

Pixel data can be input as 1, 2, 4, 8, 16, or 32 bits per pixel.

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L496001 Rev. A

Brooktree®

Product Description (continued)

The Bt496 contains transformation logic that performs real-time color space conversion from CMYK (Cyan, Magenta, Yellow, Black) pixels to RGB. Selection of CMYK-to-RGB conversion is made on a pixel-by-pixel basis with the SEL (A–D) inputs. This allows the display of individual windows of CMYK data combined with 24-bit RGB pixel-type windows on the same frame.

The Bt496 also supports pixel multiplexing rates of 4:1 (32/24 bits per pixel), 8:1 (16 bits per pixel), 16:1 (8 bits per pixel), 32:1 (4 bits per pixel), 64:1 (2 bits per pixel), and 128:1 (1 bit per pixel).

True color is supported in the 4:1 mode (32 bits per pixel CMYK /24 bits per pixel RGB) or in the 8:1 mode (16 bits per pixel RGB). Furthermore, the true-color interpretation of each pixel when in the 8:1 mode is scan line (not pixel-by-pixel) selectable to be 5, 5, 5; 6, 5, 5; or 6, 6, 4 bits of red, green, and blue.

The Bt496's use of 9-bit resolution output DACs allows effective gamma correction to gamma values of 2.7 without excessive color table entry duplication.

Multiplex modes providing 8 or less bits per pixel will address the color tables in pseudo-color fashion.

Integer zoom from 1x through 16x (inclusive) and panning to a 4-pixel resolution is also supported. The Bt496 also supports simultaneous use of zoom and pan at any of the pixel input multiplex modes.

There are two clock outputs: serial clock (SCLK*) and video clock (VIDCLK*). SCLK* is used for generating the frame buffer VRAM serial output clock. The period of SCLK* is automatically varied by the Bt496 to match the current configuration of zoom and multiplex mode so that SCLK* only occurs as often as necessary to load new pixel input data.

The VIDCLK* output is used by the system to generate the display timing signals, i.e., SYNC*, BLANK*, etc. These control signals are latched by the Bt496 on the fall of each VIDCLK*. The VIDCLK* period is programmable through the MPU port to be 1/4, 1/8, 1/16, or 1/32 of the pixel clock rate.

The Bt496 also provides a TTL-level SYNCOUT* signal, which is delayed from the input SYNC* signal by the pipeline depth of the Bt496. SYNCOUT* mirrors the SYNC-level activity on IOG. This signal may be redriven and used to provide SYNC* to monitors requiring a separate sync signal.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt496 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs allow color updating without contention with the display refresh process.

The control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU (see Table 1). The 9-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (9 bits each of red, green, and blue), using the internal address register to select the primary color palette RAM. After the blue write cycle, the address register then increments to the next location, which the MPU may continue by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

When accessing the color palette RAM, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 9 bits of the address register (ADDR0–8) are accessible to the MPU. ADDR0 corresponds to D0.

ADDR8–0	C1,C	Addressed by MPU
$xxx	00	Address Register (Addr8-0)
$xxx	01	Reserved
$000	10	ID Register ($081)
$001	10	Revision Register
$002	10	Command Register 0
$003	10	Command Register 1
$004	10	Command Register 2
$006	10	Red Pixel Read Mask Register
$007	10	Green Pixel Read Mask Register
$008	10	Blue Pixel Read Mask Register
$00C	10	Red Signature Register
$00D	10	Green Signature Register
$00E	10	Blue Signature Register
$00F	10	Test Register
$100–$1FF	10	CMYK Correction Factor LUT
$000–$0FF	11	Color Palette RAMs

Table 1. MPU Addressing Map.

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Although the color palette RAM registers are dual ported, if the pixel data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for 1 or more of the pixels on the display screen to be disturbed. Only 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers are also accessed through the address register in conjunction with the C inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and CMYK LUT, the address register increments following a read or write cycle.

If an invalid address is loaded into the address register, data written to the device will be ignored, and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt496.

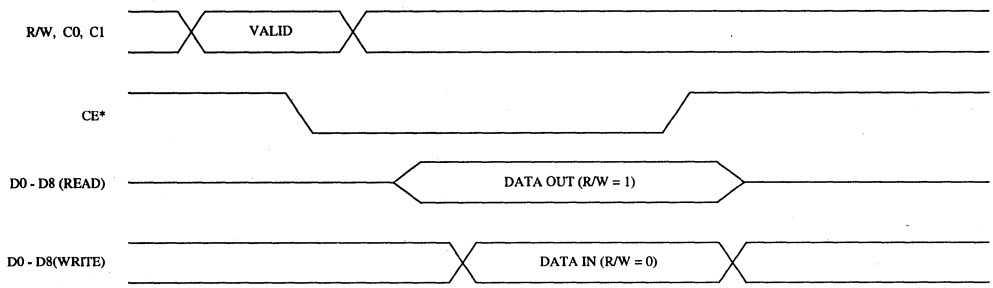

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, multiple pixels are supplied to the Bt496 each input pixel clock cycle. The number of pixels supplied each input cycle depends on the number of bits that each pixel contains. The Bt496 supports pixel depths of 32 (CMYK format), 24, 16 (RGB true color), 8, 4, 2, and 1 (pseudo color). Table 2 summarizes the available pixel formats.

When the Bt496 is running in the 4:1 multiplex mode, CMYK/RGB selection is made with the SEL inputs on a pixel-by-pixel basis. Other modes are frame selectable through command register settings.

The Bt496 provides an output clock signal (SCLK*) whose falling edge is used to load input pixel data. The SCLK period is automatically adjusted to occur only as often as required for a given pixel depth and zoom factor.

The Bt496 also provides another output clock (VIDCLK*) that should be used for the generation of the SYNC* and BLANK* inputs. The frequency of VIDCLK* is selectable to be 1/4, 1/8, 1/16, or 1/32 of the pixel clock through command register settings.

SCLK* and VIDCLK* should be immediately re-driven by a high-input impedance-inverting driver such as the Signetics 74F1804, whose output is then used to clock the frame buffer serial output data and video timing generator.

For further information on SYNC*, BLANK*, VIDCLK*, SCLK*, and input pixel timings refer to Video Generation in this section, and to the Timing Waveforms section.

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Pixel Depth	Multiplex Mode	Pixel Format
32	4:1	CMYK
24	4:1	True-Color RGB, 8-8-8
16	8:1	True-Color RGB, 5-5-5, 6-5-5, 6-6-4
8	16:1	Pseudo Color
4	32:1	Pseudo Color
2	64:1	Pseudo Color
1	128:1	Pseudo Color

Table 2. Pixel Formats Supported.

Circuit Description (continued)

Read Masking

Each CLOCK cycle, pixels are processed by the read mask and command registers. Through the read mask registers, individual pixel inputs may be enabled or disabled for display. The read mask registers are not initialized. They must be initialized by the user after power up for proper operation.

In true-color modes, each pixel is processed by the red, green, and blue read mask registers prior to addressing the color lookup tables.

In pseudo-color modes, each of the RGB read mask registers is separately applied to the same expanded color index prior to addressing the corresponding palette RAM. For example, in 4-bit-per-pixel mode, if the pixel value is $05 and the RGB read mask registers contain $F3, $0F, and $7C, then the palette entries used would be $01 for red, $05 for green, and $04 for blue.

Pixel Zoom

The Bt496 supports 1x to 16x integer zoom through the use of pixel replication. All pixel inputs are zoomed.

If 2x zooming is specified, the first pixel is output for two clock cycles, followed by the third pixel for two clock cycles, followed by the second pixel for two clock cycles, etc. Zooming of 3x is similar, except each pixel is output for three clock cycles. Zoom is supported for all bit depths.

The SCLK* period is lengthened appropriately for each of the possible zoom values. If 2x zooming is specified, the SCLK* period is twice as long as that for 1x zoom; for 3x zoom, the SCLK* period is three times as long as 1x zoom, for 4x zoom, the SCLK* period is four times as long as 1x zoom, etc.

Regardless of the zoom value, pixel data is latched only once per SCLK* period.

Pixel Panning

Pixel panning is specified to a four prezoomed pixel granularity. Valid pan values depend on the bit-per-pixel mode. Panning is accomplished partially by delaying Sync and blank signals beyond their normal position by no more than 32 screen pixels. Panning field bits used depends on the number of bits per pixel. Table 3 is the interpretation of the pan select field in command register 1.

Block mode

The Bt496 supports block modes for bit-per-pixel depths of 1, 2, 4, 8, 16, and 32 bits (Table 4). All pixel inputs are used regardless of pixel depth. Pixel unpacking may be from the MSB or LSB of each pixel port, selectable by command register bit CR03. Pixel mapping for these modes is summarized in Table 5 for MSB unpacking and Table 6 for LSB unpacking.

The SCLK* period is automatically adjusted for different pixel depth. For example, if the pixel depth is changed from 16 to 8 bits, the SCLK* period will be twice as long.

Bits per Pixel	CR18–CR14	Number of Pixels Panned
32	(xxxxx) 0 pixels	0
16	(00000) 0 pixels (10000) 4 pixels	0, or 4
8	(00000) 0 pixels (01000) 4 pixels (10000) 8 pixels (11000) 12 pixels	0, 4, 8, or 12
4	(00000) 0 pixels (00100) 4 pixels (01000) 8 pixels . . (11100) 28 pixels	0, 4, 8, 12, 16, 20, 24, or 28
2	(00000) 0 pixels . . . (11110) 60 pixels	0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, or 60.
1	(00000) 0 pixels . . . (11111) 124 pixels	0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60, 64, 68, 72, 76, 80, 84, 88, 92, 96, 100, 104, 108, 112, 116, 120, or 124.

Table 3. Pixel Pan.

Bits per Pixel	Pixels per SCLK*	Colors Displayable
1	128	2
2	64	4
4	32	16
8	16	256
16	8	64K
32	4	16.7M

Table 4. Block Mode Operation.

Circuit Description (continued)

Pixel Port Bits		Bit-per-Pixel Depth					
		32/24	16	8	4	2	1
PA	31–24	Pixel 1 (Black)	Pixel 1	Pixel 1	Pixel 1	Pixel 1	Pixel 1
	23–16	Pixel 1 (Cyan/Red)		Pixel 2	.	.	.
	15–8	Pixel 1 (Magenta/Green)	Pixel 2	Pixel 3	.	.	.
	7–0	Pixel 1 (Yellow/Blue)		Pixel 4	Pixel 8	Pixel 16	Pixel 32
PB	31–24	Pixel 2 (Black)	Pixel 3	Pixel 5	Pixel 9	Pixel 17	Pixel 33
	23–16	Pixel 2 (Cyan/Red)		Pixel 6	.	.	.
	15–8	Pixel 2 (Magenta/Green)	Pixel 4	Pixel 7	.	.	.
	7–0	Pixel 2 (Yellow/Blue)		Pixel 8	Pixel 16	Pixel 32	Pixel 64
PC	31–24	Pixel 3 (Black)	Pixel 5	Pixel 9	Pixel 17	Pixel 33	Pixel 65
	23–16	Pixel 3 (Cyan/Red)		Pixel 10	.	.	.
	15–8	Pixel 3 (Magenta/Green)	Pixel 6	Pixel 11	.	.	.
	7–0	Pixel 3 (Yellow/Blue)		Pixel 12	Pixel 24	Pixel 48	Pixel 96
PD	31–24	Pixel 4 (Black)	Pixel 7	Pixel 13	Pixel 25	Pixel 49	Pixel 97
	23–16	Pixel 4 (Cyan/Red)		Pixel 14	.	.	.
	15–8	Pixel 4 (Magenta/Green)	Pixel 8	Pixel 15	.	.	.
	7–0	Pixel 4 (Yellow/Blue)		Pixel 16	Pixel 32	Pixel 64	Pixel 128

Table 5. Pixel Port Unpacking from MSB (CR03 = 0).

Pixel Port Bits		Bit-per-Pixel Depth					
		32/24	16	8	4	2	1
PA	31–24	Pixel 1 (Black)	Pixel 2	Pixel 4	Pixel 8	Pixel 16	Pixel 32
	23–16	Pixel 1 (Cyan/Red)		Pixel 3	.	.	.
	15–8	Pixel 1 (Magenta/Green)	Pixel 1	Pixel 2	.	.	.
	7–0	Pixel 1 (Yellow/Blue)		Pixel 1	Pixel 1	Pixel 1	Pixel 1
PB	31–24	Pixel 2 (Black)	Pixel 4	Pixel 8	Pixel 16	Pixel 32	Pixel 64
	23–16	Pixel 2 (Cyan/Red)		Pixel 7	.	.	.
	15–8	Pixel 2 (Magenta/Green)	Pixel 3	Pixel 6	.	.	.
	7–0	Pixel 2 (Yellow/Blue)		Pixel 5	Pixel 9	Pixel 17	Pixel 33
PC	31–24	Pixel 3 (Black)	Pixel 6	Pixel 12	Pixel 24	Pixel 48	Pixel 96
	23–16	Pixel 3 (Cyan/Red)		Pixel 11	.	.	.
	15–8	Pixel 3 (Magenta/Green)	Pixel 5	Pixel 10	.	.	.
	7–0	Pixel 3 (Yellow/Blue)		Pixel 9	Pixel 17	Pixel 33	Pixel 65
PD	31–24	Pixel 4 (Black)	Pixel 8	Pixel 16	Pixel 32	Pixel 64	Pixel 128
	23–16	Pixel 4 (Cyan/Red)		Pixel 15	.	.	.
	15–8	Pixel 4 (Magenta/Green)	Pixel 7	Pixel 14	.	.	.
	7–0	Pixel 4 (Yellow/Blue)		Pixel 13	Pixel 25	Pixel 49	Pixel 97

Table 6. Pixel Port Unpacking from LSB (CR03 = 1).

Circuit Description (continued)

Shift Clock Generation

The Bt496 facilitates the generation of the VRAM shift clock by providing SCLK*. SCLK* should be used to clock the VRAM shift registers that provide pixel data to the Bt496. The ratio of SCLK* to pixel CLOCK is adjusted so that all pixel input bits are presented once during each SCLK* period. The Bt496 supports zoom concurrently with each of the block modes, requiring a number of different SCLK* periods. For example, with 32-bit-per-pixel depth and 1x zoom, SCLK* occurs every four CLOCK cycles; or for 16-bit-per-pixel depth and 1x zoom or 8-bit-per-pixel depth and 2x zoom, SCLK* occurs every eight CLOCK cycles. The SCLK* period may be computed with the following formula:

$$\lambda = 128\ (Z/D)$$

where λ is the SCLK* period (in pixel clock cycles), Z is the zoom factor, and D is the pixel depth. Table 7 is a list of SCLK* periods for all possible combinations of pixel depth and zoom.

Zoom Factor	Pixel Depth					
	32	16	8	4	2	1
1	4	8	16	32	64	128
2	8	16	32	64	128	256
3	12	24	48	96	192	384
4	16	32	64	128	256	512
5	20	40	80	160	320	640
6	24	48	96	192	384	768
7	28	56	112	224	448	896
8	32	64	128	256	512	1024
9	36	72	144	288	576	1152
10	40	80	160	320	640	1280
11	44	88	176	352	704	1408
12	48	96	192	384	768	1536
13	52	104	208	416	832	1664
14	56	112	224	448	896	1792
15	60	120	240	480	960	1920
16	64	128	256	512	1024	2048

Table 7. SCLK* Period Table (in Pixel Clock Cycles).

SCLK* is stopped (in a logical-one state) during blanking to allow the system to reload the VRAM serial shift registers. System implementations using midline transfer may need to insert a VRAM shift clock pulse during blanking time to load the shift register tap address. The system may insert this additional clock without incurring additional gate delays by using a NAND driver for SCLK*. The unused (and normally high) input on the NAND driver may then be used to insert additional SCLK*s. These implementations already present valid pixel information at the end of the blanking period. Therefore, the first SCLK* asserted by the Bt496 should load pixel data. For these implementations, CR08 should be a logical zero. Further information is contained in Figure 2 and in the Video Generation section.

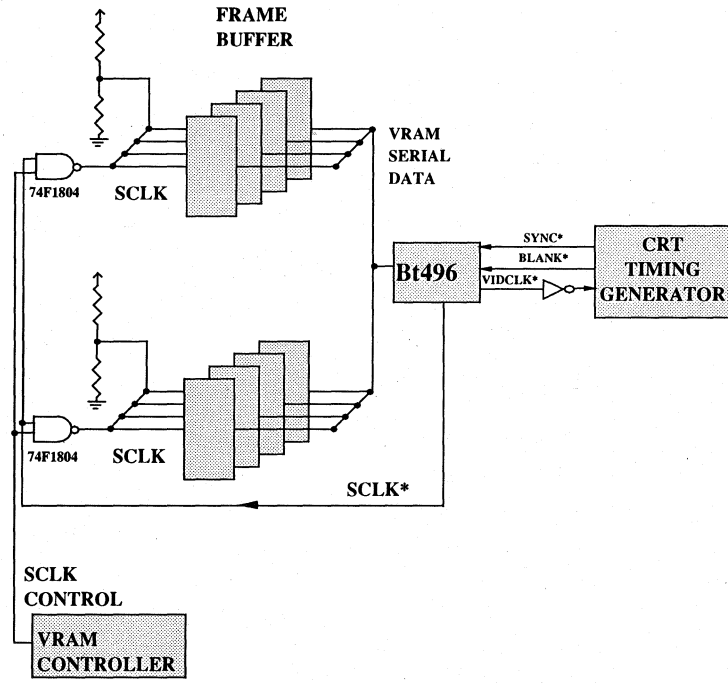

Figure 2. VRAM Serial Clock Interface.

Circuit Description (continued)

Color Modes

The Bt496 processes the pixel types listed in Table 8.

Pixel Type	Description
32 bit, CMYK, True Color	Subtractive color space, 8 bits each of black, cyan, magenta, and yellow for each pixel. Pixels are converted to RGB color space, masked, then used to address color tables.
24 bit, RGB, 8-8-8, True Color	8 bits each of red, green, and blue for each pixel. Additional 8 supplied pixel bits are ignored. Pixels are RGB masked, then used to address color tables.
16 bit, RGB, 5-5-5, True Color	5 bits each of red, green, and blue for each pixel. Additional supplied pixel bit in MSB of pixel data is ignored. Color component values are left-justified into three 8-bit values.
16 bit, RGB, 6-5-5, True Color	6 bits of red, 5 bits each of green and blue for each pixel. Color component values are left-justified into three 8-bit values.
16 bit, RGB, 6-6-4, True Color	6 bits each of red and green, and 4 bits of blue for each pixel. Color component values are left-justified into three 8-bit values.
8 bit, RGB, Pseudo Color	8 bits of supplied pixel data are read masked into three color palette addresses, then used to address color palettes.
4 bit, RGB, Pseudo Color	4 bits of supplied pixel data are right-justified into an 8-bit value, then read masked into three color palette addresses.
2 bit, RGB, Pseudo Color	2 bits of supplied pixel data are right-justified into an 8-bit value, then read masked into three color palette addresses.
1 bit, RGB, Pseudo Color	1 bit of supplied pixel data is right-justified into an 8-bit value, then read masked into three color palette addresses.

Table 8. Pixel Processing Modes.

When 32-bit-per-pixel depth is specified, each of the 4 pixels may be selected for CMYK or RGB processing on a pixel basis by using the CMYK control inputs. A CMYK pixel has 8 bits each for black, cyan, magenta, and yellow. CMYK pixel mapping is detailed in Table 9. If the CMYK controls specify RGB processing, 8 bits each for red, green, and blue are used. The remaining 8 bits are ignored.

When 16-bit-per-pixel depth is specified, 8 pixels are presented each SCLK period. One of three modes for pixel interpretation is selected by CR05 and CR04. The pixel bits supplied for each channel are used as the MSBs of the color table addresses. To maintain the ability to produce a full-scale output without reloading a gamma-corrected color lookup table, the supplied bits are duplicated from left (MSB) to right (LSB) into the unspecified address bits of the color table. This value is then subject to read masking. This operation is detailed in Table 10.

When 8-bit-or-less-per-pixel depth is specified, the Bt496 operates in pseudo-color mode, presenting the same 8-bit value to all three color palette tables (subject to read masking).

Pixel Depth	SEL	Pixel Number	Transformation Input Pixel Mapping			
			Black (7–0)	Cyan (7–0)	Magenta (7–0)	Yellow (7–0)
32	1	1	P31A–P24A	P23A–P16A	P15A–P8A	P7A–P0A
		2	P31B–P24B	P23B–P16B	P15B–P8B	P7B–P0B
		3	P31C–P24C	P23C–P16C	P15C–P8C	P7C–P0C
		4	P31D–P24D	P23D–P16D	P15D–P8D	P7D–P0D

Table 9. CMYK Pixel Format.

		Red Address								Green Address								Blue Address							
5:5:5	RAM Address	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Pixel Input	14	13	12	11	10	14	13	12	9	8	7	6	5	9	8	7	4	3	2	1	0	4	3	2
		30	29	28	27	26	30	29	28	25	24	23	22	21	25	24	23	20	19	18	17	16	20	19	18
6:5:5	RAM Address	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Pixel Input	15	14	13	12	11	10	15	14	9	8	7	6	5	9	8	7	4	3	2	1	0	4	3	2
		31	30	29	28	27	26	31	30	25	24	23	22	21	25	24	23	20	19	18	17	16	20	19	18
6:6:4	RAM Address	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Pixel Input	15	14	13	12	11	10	15	14	9	8	7	6	5	4	9	8	3	2	1	0	3	2	1	0
		31	30	29	28	27	26	31	30	25	24	23	22	21	20	25	24	19	18	17	16	19	18	17	16

Table 10. Color Table Address Generation for 16-bit True Color.

Circuit Description (continued)

Pixels may be unpacked starting from the MSBs by setting CR03 = 0. To unpack starting from the LSBs, set CR03 = 1. Tables 5 and 6 list the pixel input bit mapping for all available pixel depths. Tables 11 and 12 provide greater detail on pixel unpacking for true-color modes, as does Table 13 for pseudo-color modes.

Bit(s) per pixel	SEL Input	CR05–CR04	Bits per			Pixel Number	Red(7–0)	Green(7–0)	Blue(7–0)
			Red	Gree	Blue				
24	0	XX	8	8	8	1	R7–0 = P23A–P16A	G7–0 = P15A–P8A	B7–0 = P7A–P0A
						2	R7–0 = P23B–P16B	G7–0 = P15B–P8B	B7–0 = P7B–P0B
						3	R7–0 = P23C–P16C	G7–0 = P15C–P8C	B7–0 = P7C–P0C
						4	R7–0 = P23D–P16D	G7–0 = P15D–P8D	B7–0 = P7D–P0D
16	X	00	5	5	5	1	R7–3 = P30A–P26A	G7–3 = P25A–P21A	B7–3 = P20A–P16A
						2	R7–3 = P14A–P10A	G7–3 = P9A–P5A	B7–3 = P4A–P0A
						3	R7–3 = P30B–P26B	G7–3 = P25B–P21B	B7–3 = P20B–P16B
						4	R7–3 = P14B–P10B	G7–3 = P9B–P5B	B7–3 = P4B–P0B
						5	R7–3 = P30C–P26C	G7–3 = P25C–P21C	B7–3 = P20C–P16C
						6	R7–3 = P14C–P10C	G7–3 = P9C–P5C	B7–3 = P4C–P0C
						7	R7–3 = P30D–P26D	G7–3 = P25D–P21D	B7–3 = P20D–P16D
						8	R7–3 = P14D–P10D	G7–3 = P9D–P5D	B7–3 = P4D–P0D
16	X	01	6	5	5	1	R7–2 = P31A–P26A	G7–3 = P25A–P21A	B7–3 = P20A–P16A
						2	R7–2 = P15A–P10A	G7–3 = P9A–P5A	B7–3 = P4A–P0A
						3	R7–2 = P31B–P26B	G7–3 = P25B–P21B	B7–3 = P20B–P16B
						4	R7–2 = P15B–P10B	G7–3 = P9B–P5B	B7–3 = P4B–P0B
						5	R7–2 = P31C–P26C	G7–3 = P25C–P21C	B7–3 = P20C–P16C
						6	R7–2 = P15C–P10C	G7–3 = P9C–P5C	B7–3 = P4C–P0C
						7	R7–2 = P31D–P26D	G7–3 = P25D–P21D	B7–3 = P20D–P16D
						8	R7–2 = P15D–P10D	G7–3 = P9D–P5D	B7–3 = P4D–P0D
16	X	10	6	6	4	1	R7–2 = P31A–P26A	G7–2 = P25A–P20A	B7–4 = P19A–P16A
						2	R7–2 = P15A–P10A	G7–2 = P9A–P4A	B7–4 = P3A–P0A
						3	R7–2 = P31B–P26B	G7–2 = P25B–P20B	B7–4 = P19B–P16B
						4	R7–2 = P15B–P10B	G7–2 = P9B–P4B	B7–4 = P3B–P0B
						5	R7–2 = P31C–P26C	G7–2 = P25C–P20C	B7–4 = P19C–P16C
						6	R7–2 = P15C–P10C	G7–2 = P9C–P4C	B7–4 = P3C–P0C
						7	R7–2 = P31D–P26D	G7–2 = P25D–P20D	B7–4 = P19D–P16D
						8	R7–2 = P15D–P10D	G7–2 = P9D–P4D	B7–4 = P3D–P0D

Table 11. True-Color Pixel Formats, MSB Pixel Unpacking (CR03 = 0).

Circuit Description (continued)

Bit(s) per pixel	SEL Input	CR05–CR04	Bits per Band			Pixel Number	Color Palette		
			Red	Gree	Blue		Red(7–0)	Green(7–0)	Blue(7–0)
24	0	XX	8	8	8	1	R7–0 = P23A–P16A	G7–0 = P15A–P8A	B7–0 = P7A–P0A
						2	R7–0 = P23B–P16B	G7–0 = P15B–P8B	B7–0 = P7B–P0B
						3	R7–0 = P23C–P16C	G7–0 = P15C–P8C	B7–0 = P7C–P0C
						4	R7–0 = P23D–P16D	G7–0 = P15D–P8D	B7–0 = P7D–P0D
16	X	00	5	5	5	1	R7–3 = P14A–P10A	G7–3 = P9A–P5A	B7–3 = P4A–P0A
						2	R7–3 = P30A–P26A	G7–3 = P25A–P21A	B7–3 = P20A–P16A
						3	R7–3 = P14B–P10B	G7–3 = P9B–P5B	B7–3 = P4B–P0B
						4	R7–3 = P30B–P26B	G7–3 = P25B–P21B	B7–3 = P20B–P16B
						5	R7–3 = P14C–P10C	G7–3 = P9C–P5C	B7–3 = P4C–P0C
						6	R7–3 = P30C–P26C	G7–3 = P25C–P21C	B7–3 = P20C–P16C
						7	R7–3 = P14D–P10D	G7–3 = P9D–P5D	B7–3 = P4D–P0D
						8	R7–3 = P30D–P26D	G7–3 = P25D–P21D	B7–3 = P20D–P16D
16	X	01	6	5	5	1	R7–2 = P15A–P10A	G7–3 = P9A–P5A	B7–3 = P4A–P0A
						2	R7–2 = P31A–P26A	G7–3 = P25A–P21A	B7–3 = P20A–P16A
						3	R7–2 = P15B–P10B	G7–3 = P9B–P5B	B7–3 = P4B–P0B
						4	R7–2 = P31B–P26B	G7–3 = P25B–P21B	B7–3 = P20B–P16B
						5	R7–2 = P15C–P10C	G7–3 = P9C–P5C	B7–3 = P4C–P0C
						6	R7–2 = P31C–P26C	G7–3 = P25C–P21C	B7–3 = P20C–P16C
						7	R7–2 = P15D–P10D	G7–3 = P9D–P5D	B7–3 = P4D–P0D
						8	R7–2 = P31D–P26D	G7–3 = P25D–P21D	B7–3 = P20D–P16D
16	X	10	6	6	4	1	R7–2 = P15A–P10A	G7–2 = P9A–P4A	B7–4 = P3A–P0A
						2	R7–2 = P31A–P26A	G7–2 = P25A–P20A	B7–4 = P19A–P16A
						3	R7–2 = P15B–P10B	G7–2 = P9B–P4B	B7–4 = P3B–P0B
						4	R7–2 = P31B–P26B	G7–2 = P25B–P20B	B7–4 = P19B–P16B
						5	R7–2 = P15C–P10C	G7–2 = P9C–P4C	B7–4 = P3C–P0C
						6	R7–2 = P31C–P26C	G7–2 = P25C–P20C	B7–4 = P19C–P16C
						7	R7–2 = P15D–P10D	G7–2 = P9D–P4D	B7–4 = P3D–P0D
						8	R7–2 = P31D–P26D	G7–2 = P25D–P20D	B7–4 = P19D–P16D

Table 12. True-Color Pixel Formats, LSB Pixel Unpacking (CR03 = 1).

Bit(s) per pixel	Pixel Number	Color Table Addressing (RA7–0)	
		MSB Unpacking (CR03 = 0)	LSB Unpacking (CR03 = 1)
8	1	RA7–0 = P31A–P24A	RA7–0 = P7A–P0A
	2	RA7–0 = P23A–P16A	RA7–0 = P15A–P8A
	3	RA7–0 = P15A–P8A	RA7–0 = P23A–P16A
	4	RA7–0 = P7A–P0A	RA7–0 = P31A–P24A
	5	RA7–0 = P31B–P24B	RA7–0 = P7B–P0B
	.	.	.
	.	.	.
	.	.	.
	16	RA7–0 = P7D–P0D	RA7–0 = P31D–P24D
4	1	RA3–0 = P31A–P28A	RA3–0 = P3A–P0A
	.	.	.
	.	.	.
	.	.	.
	8	RA3–0 = P3A–P0A	RA3–0 = P31A–P28A
	9	RA3–0 = P31B–P28B	RA3–0 = P3B–P0B
	.	.	.
	.	.	.
	.	.	.
	32	RA3–0 = P3D–P0D	PA3–0 = P31D–P28D
2	1	RA1–0 = P31A–P30A	RA1–0 = P1A–P0A
	.	.	.
	.	.	.
	.	.	.
	16	RA1–0 = P1A–P0A	RA1–0 = P31A–P30A
	17	RA1–0 = P31B–P30B	RA1–0 = P1B–P0B
	.	.	.
	.	.	.
	.	.	.
	64	RA1–0 = P1D–P0D	RA1–0 = P31D–P30D
1	1	RA0 = P31A	RA0 = P0A
	.	.	.
	.	.	.
	.	.	.
	32	RA0 = P0A	RA0 = P31A
	33	RA0 = P31B	RA0 = P0B
	.	.	.
	.	.	.
	.	.	.
	128	RA0 = P0D	RA0 = R31D

Table 13. Pseudo-Color Pixel Formats.

Circuit Description (continued)

CMYK-to-RGB Conversion

The Bt496 allows printer prepress applications to directly display data in the CMYK color space. This eliminates the need for the application to maintain, manipulate, and convert image data to or from the RGB color space, generally required by graphics display systems. In systems that use the Bt496, the application may directly store CMYK image data into the frame buffer. Conversion from the CMYK color space to the RGB color space needed by generic CRT monitors is performed in real time by the Bt496 at the display refresh rate of the monitor.

The color-space conversion transformation performed by the Bt496 is based on the inverse of a color separation algorithm explained in this section. Since an understanding of the CMYK color space is required, some background information is given.

CMY Color Space

The CMY (Cyan, Magenta, Yellow) color space is an alternative color space that is related to the RGB color space as follows:

	Relationship to RGB Space
Cyan	White—Red
Magenta	White—Green
Yellow	White—Blue

The CMY color space is also referred to as a "subtractive color space" because of this relationship to the RGB color space.

Prepress applications generally require that image data ultimately be specified in a subtractive color space, as the printing process creates colors by using inks (which absorb color) on white paper. Ideally, a cyan ink absorbs red light, leaving only that portion of the spectrum (i.e., green and blue) to be perceived by the eye; a magenta ink absorbs green light, leaving red and blue; and a yellow ink absorbs blue, leaving red and green. For example, progressively reducing the level (i.e., saturation) of cyan increases the red content. The following table lists the alternative representations for some common colors.

CMYK Color Space

The mixing of CMY process colors does not yield a good black. The use of more costly colored inks to achieve colors that contain various amounts of gray can be reduced by also using a black process color.

Color	RGB Space			CMY Space		
	R	G	B	C	M	Y
Black	0	0	0	1	1	1
Red	1	0	0	0	1	1
Green	0	1	0	1	0	1
Blue	0	0	1	1	1	0
Cyan	0	1	1	1	0	0
Magenta	1	0	1	0	1	0
Yellow	1	1	0	0	0	1
Gray	0.5	0.5	0.5	0.5	0.5	0.5
White	1	1	1	0	0	0

When a black process color is added to the CMY color space, another color space results. This is commonly known as the CMYK (Cyan, Magenta, Yellow, and Black) color space.

When a black level is specified, transformations from RGB to CMYK are nonunique. An obvious example is in the representation of gray colors. Here, equal amounts of CMY with no black, zero amounts of CMY with some amount of black, or a mixture of these may be used to achieve the same gray color. The amount of process black used to replace the gray content in the CMY process colors is commonly called the GCR (Gray Component Replacement) level. A value of 1 for GCR indicates that the maximum amount of process black is used to substitute for CMY gray level; a value of zero indicates that no process black is used.

To explain the conversion process, the following quantities are defined:

$x_{min} = min\ (C, M, Y)$

$x_{max} = max\ (C, M, Y)$

$d = x_{max} - x_{min}$

The conversion process can then be expressed as follows:

$R = 1 - C - k$

$G = 1 - M - k$

$B = 1 - Y - k$

where

$k = min(k_1, k_2)$,

$k_1 = 1 - x_{max}$, and

$k_2 = Kf(d)$

Circuit Description (continued)

The function $f(d)$ is implemented with a 256 x 8 lookup table. This table must be loaded by the MPU. This function depends on the desired relationship of GCR and saturation. The function $f(x)$ used is of the form

$$f(x) = G^{(a-1)}(1-x)^{b}$$

where G is the GCR, a relates the black with the CMY levels for the desired GCR, and b relates black with the CMY levels with respect to saturation.

As an example for loading the lookup table, if the desired GCR level is 0.7 with $a = 5$ and $b = 2$, the function to implement is:

$$f(x) = (0.7)^{(5-1)}(1-x)^{2}$$

To tabulate the values of this function for $0 \le x \le 1$ (i.e., 0000 0000 ≤ x ≤ 1111 1111, binary), the MPU must load the lookup table with the values listed in Table 14.

A simplified block diagram of the CMYK-to-RGB transformation is shown in Figure 3.

Location	Contents	Location	Contents
$00	$3D	$4A–$4C	$1E
$01–$02	$3C	$4D–$4F	$1D
$03–$04	$3B	$50–$52	$1C
$05–$06	$3A	$53–$55	$1B
$07–$08	$39	$56–$58	$1A
$09–$0B	$38	$59–$5C	$19
$0C–$0D	$37	$5D–$5F	$18
$0E–$0F	$36	$60–$62	$17
$10–$11	$35	$63–$66	$16
$12–$13	$34	$67–$69	$15
$14–$16	$33	$6A–$6D	$14
$17–$18	$32	$6E–$70	$13
$19–$1A	$31	$71–$74	$12
$1B–$1D	$30	$75–$78	$11
$1E–$1F	$2F	$79–$7C	$10
$20–$21	$2E	$7D–$80	$0F
$22–$24	$2D	$81–$85	$0E
$25–$26	$2C	$86–$89	$0D
$27–$29	$2B	$8A–$8E	$0C
$2A–$2B	$2A	$8F–$92	$0B
$2C–$2E	$29	$93–$97	$0A
$2F–$30	$28	$98–$9D	$09
$31–$33	$27	$9E–$A2	$08
$34–$36	$26	$A3–$A8	$07
$37–$38	$25	$A9–$AF	$06
$39–$3B	$24	$B0–$B6	$05
$3C–$3E	$23	$B7–$BD	$04
$3F–$40	$22	$BE–$C6	$03
$41–$43	$21	$C7–$D0	$02
$44–$46	$20	$D1–$DE	$01
$47–$49	$1F	$DF–$FF	$00

Table 14. CMYK-to-RGB Transformation with RAM Contents for GCR = 0.7, a = 5, and b = 2.

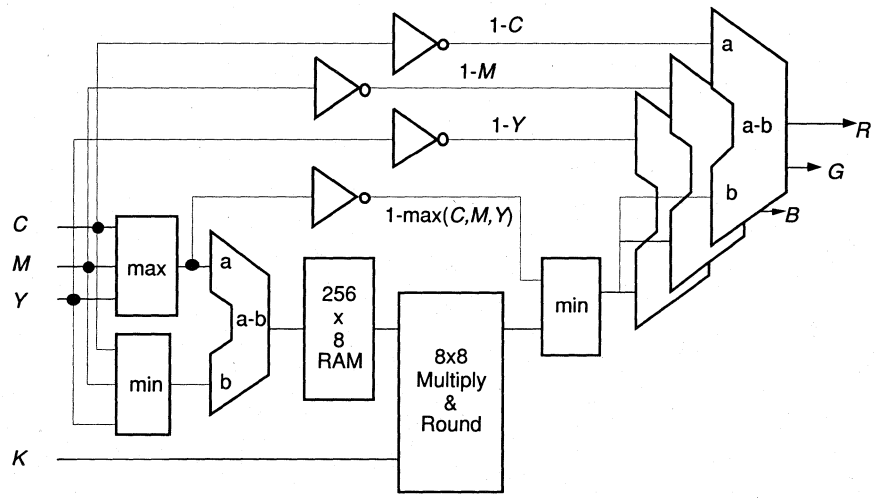

Figure 3. CMYK–to–RGB Conversion.

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Circuit Description (continued)

Video Generation

Video input pixel timing is shown in Figure 4.

The VIDCLK* output is a free-running clock typically used for clocking the display timing generator. The MPU controls the period of VIDCLK* by setting bits CR07 and CR06 in command register 0. VIDCLK* may be CLOCK/4, CLOCK/8, CLOCK/16, or CLOCK/32. SYNC and BLANK information is latched with each falling edge of VIDCLK* and inserted into the pipelined pixel stream at the appropriate time. No relationship should be considered to exist between the SYNC*/BLANK* signals and the incoming pixel data. The SYNC* and BLANK* inputs are used to provide the RAMDAC with timing information; i.e., blank duration, front porch, sync duration, and back porch.

Since VIDCLK* generally runs with a different period from SCLK*, SYNC* and BLANK* may be provided at a higher resolution than the number of pixels loaded each SCLK*. Thus, not all pixels loaded with the last active SCLK* will necessarily be displayed on the screen. However, on the leading edge of the scan line, the first pixel loaded by SCLK* will be the first pixel displayed.

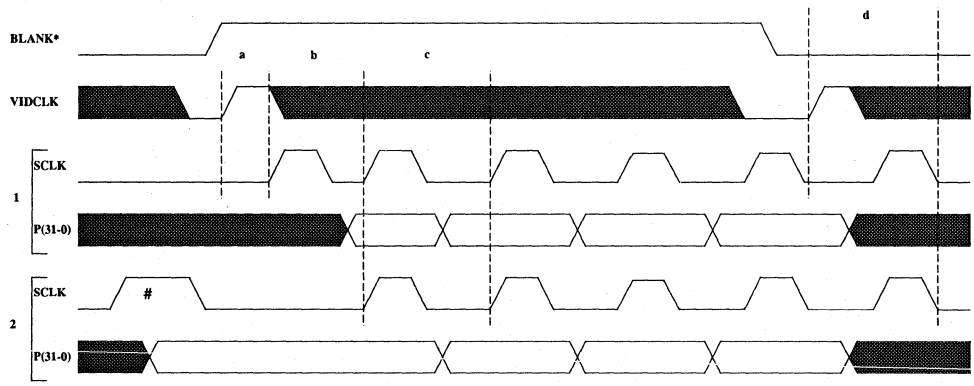
The SYNCOUT* signal follows the SYNC* input by the number of pipeline stages internal to the Bt496. It is positioned with pixel resolution and should be used to derive the SYNC signal for displays requiring separate TTL sync. The RAMDAC pipeline delay present from the input pixel port to the output is constant for a given pixel pan amount.

It is recommended that MPU operations requiring display synchronization to blank and/or sync (e.g., command register updates) read command register "CR21 and CR20" to synchronize. SYNC* and/or BLANK* input signals will not provide accurate synchronization because of the size and variability of the Bt496's pipeline depth.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 5 and 6. Command register 2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 15 and 16 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt496 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for



#: SCLK pulse provided by system

a: 1-4 Clock Cycles

b: 4 Clock Cycles

c: f (bit depth, zoom)

d: trailing edge of last possible SCLK cycle: about 6 clock cycles

Brackets indicate versions of SCLK selectable by command register: 1-Non midline transfer, 2-Midline transfer

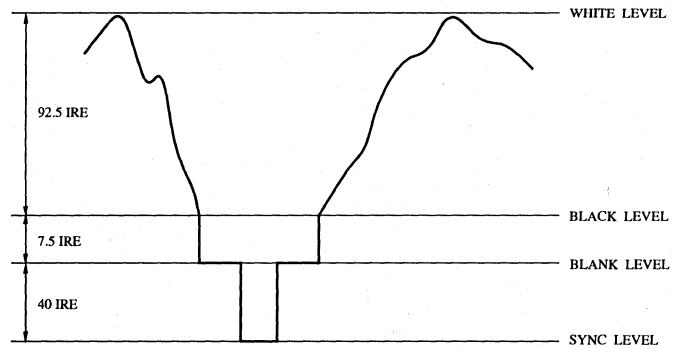
Note: For clarity, this figure shows SCLK and VIDCLK outputs inverted.

Figure 4. Video Input Pixel Timing.

Circuit Description (continued)

precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed with the use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 562 Ω (0.5%), and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 5. Composite Video Output Waveform (SETUP = 7.5 IRE).

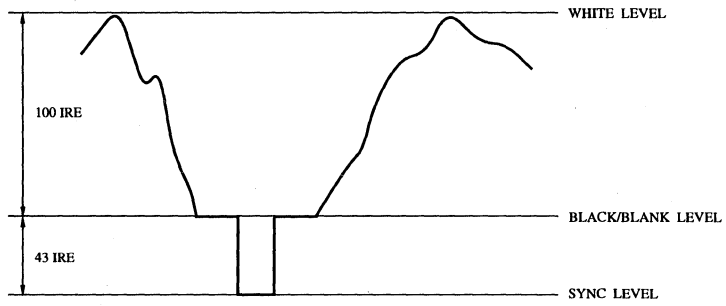
Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 562 Ω (0.5%), and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 15. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 530 Ω (0.5%), and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 6. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 530 Ω (0.5%), and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 16. Video Output Truth Table (SETUP = 0 IRE).

Command Register 0

This register is located at internal address $002 and may be written or read by the MPU at any time. This register must be initialized by the user after power up for proper operation.

Bit(s)	Function	Description
CR08	SCLK* Control (0) extra pulse not needed (1) extra pulse needed	This bit specifies whether the first SCLK* pulse after a blanked time is needed (logical one) to read the first pixel item. A logical zero indicates that the system has externally provided the first VRAM shift clock, and the Bt496 may latch valid pixel data with the first SCLK*.
CR07, CR06	VIDCLK Select (00) CLOCK/4 (01) CLOCK/8 (10) CLOCK/16 (11) CLOCK/32	Video clock output period select
CR05,CR04	16-bit-per-pixel true color mode (00) 5 red, 5 green, 5 blue (01) 6 red, 5 green, 5 blue (10) 6 red, 6 green, 4 blue (11) reserved	These bits specify the interpretation of the pixel data when the device is processing in 16-bit-per-pixel mode. These bits are ignored in other modes.
CR03	Pixel Unpacking Mode (0) unpacked from MSB (1) unpacked from LSB	This bit specifies the unpacking mode for pixels of less than 32 bits. When this bit is a logical zero, pixels are unpacked starting from PA bit 31. When this bit is a logical one, pixels are unpacked starting from PA bit 0.
CR02–CR00	Block Mode Select (11X) – Reserved (101) – 32 bits per pixel (100) – 16 bits per pixel (011) – 8 bits per pixel (010) – 4 bits per pixel (001) – 2 bits per pixel (000) – 1 bit per pixel	These bits specify whether the pixel data is input as 1, 2, 4, 8, 16, or 32 bits per pixel.

Internal Registers (continued)

Command Register 1

This register is located at internal address $003 and may be written or read by the MPU at any time. This register must be initialized by the user after power up for proper operation.

Bit(s)	Function	Description
CR18–CR14	Pan Select	These bits specify the pan amount. Pan may be specified to a 4-pixel prezoomed boundary. Valid pan ranges depend on the bits-per-pixel setting. Table 3 contains bit definitions.
CR13, CR10	Zoom Factor (0000) – 1x . . . (1111) – 16x	These bits specify the zoom amount. For 2x zoom, the first pixel is output for two clock cycles, followed by the second pixel for two clock cycles, the third pixel for two clock cycles, etc. For 3x zoom, the first pixel is output for three clock cycles, the second pixel for three clock cycles, the third pixel for three clock cycles, etc.

Internal Registers (continued)

Command Register 2

This register is located at internal address $004 and may be written or read by the MPU at any time. This register must be initialized by the user after power up for proper operation.

Bit(s)	Function	Description
CR28	Reserved	
CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero). A logical zero on this bit will disable CR21 and the SYNCOUT* pin.
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25–CR22	Reserved	
CR21	SYNC	This bit tracks the SYNC level on IOG and specifies whether SYNC is being output onto IOG (logical one) or not (logical zero). This bit is read only. Any attempts to write to this bit will be ignored.
CR20	BLANK	This bit tracks the BLANK level and specifies whether BLANK is being output onto IOR, IOG, and IOB (logical one) or not (logical zero). This bit should be used to synchronize MPU events to display blanking time. This bit is read only. Any attempts to write to this bit will be ignored.

Internal Registers (continued)

ID Register ($000)

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt496, the value read by the MPU will be $081. Data written to this register is ignored.

Revision Register ($001)

This 9-bit register may be read by the MPU to determine the revision level of the Bt496. The upper 4 bits indicate revisions while the lower 5 bits should be ignored. The current revision is $A. Data written to this register is ignored.

Pixel Read Mask Registers ($006-$008)

The 24-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. This register must be initialized by the user after power up for proper operation. D0 corresponds to P0.

Red, Green, and Blue Signature Registers ($00C-$00E)

The test register must be enabled in order to use the signature or the data strobe mode. Refer to the Test Register ($00F) description in this section. During normal operation, the test registers should be disabled for power consideration.

Signature Mode

These three 9-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed values.

When a test display is loaded into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. Refer to the Application Information Test Register section for more information.

Data Strobe Mode

If "data strobe testing" is selected, the operation of the signature registers changes. Rather than determining the signatures, they capture red, green, and blue data being presented to the three DACs. Test Features of the Bt496 in the Application Information section contains further test register information.

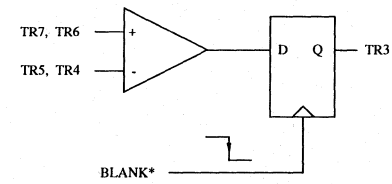
Internal Registers (continued)

Test Register ($00F)

This 9-bit register is used to test the Bt496.

Bits	Function	Description
TR8	Test Mode Enable (0) disable test mode (1) enable test mode	This bit specifies whether the test mode is enabled or disabled. The test register must be enabled in order to select signature analysis or data strobe test modes. For normal operation, test registers should be for power considerations.
TR7–TR3	Comparator	TR7–TR3 are used to compare the analog RGB outputs to each other and to a 150 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs, and whether the DACs are functional. See below.
TR2–TR1	Continuity result	These pins are used to assist in an ATE continuity test. Their function is not defined at this time.
TR0	Test Mode Select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers hold the test result for both test modes.

TR7	TR6	TR5	TR4	TR3
red select	green select	blue select	150 mV ref. select	result



TR7–TR4		If TR3 = 1	If TR3 = 0
0000	normal operation	—	—
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 150 mV reference	red > 150 mV	red < 150 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 150 mV reference	green > 150 mV	green < 150 mV

The table above lists the valid comparison combinations. A logical one enables that function to be compared; the result is TR3. For normal operation, TR7–TR3 must be logical zeros.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 15 and 16. It is latched on the falling edge of VIDCLK*.
SYNC*	Composite sync control input (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 5 and 6). SYNC* does not override any other control or data input, as shown in Tables 15 and 16; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the falling edge of VIDCLK*.
SYNCOUT*	Composite sync control output (TTL compatible). This output is typically used to generate the composite sync signal for CRTs requiring separate sync.
SCLK*	VRAM shift clock output (TTL compatible). The falling edge of this output is used to clock the input pixel data. The shift clock frequency is a function of the number of bits per pixel and the zoom factor. An external inverting buffer should be used to drive the pixel VRAM serial clock inputs. Waveform is active (low) for four CLOCK cycles, then inactive (high) as required to achieve cycle time. The shift clock is automatically stopped/started for blanked intervals.
VIDCLK*	Video clock output (TTL compatible). This output is CLOCK divided by 4, 8, 16, or 32, as programmed in command register 0. Sync and blank inputs are latched by this clock. 50/50 duty cycle.
P31–P0 {A–D}	Pixel inputs (TTL compatible). These inputs are used to specify color palette locations in RGB or pseudo-color modes. In CMYK mode, these pixels are converted to RGB color space, then used to specify which locations of the color palette RAM are used to provide color information. These inputs are latched on the falling edge of SCLK*.
SEL(A-D)	SEL mode select inputs (TTL compatible). These inputs specify the interpretation of the pixels supplied on the pixel inputs. A high level causes the corresponding pixel inputs to be interpreted as CMYK data. A low level indicates RGB pixel data. These inputs are valid only in 32-bit per pixel mode. These inputs are latched on the falling edge of SCLK*.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 8). Each of these outputs, whether used or not, should have the same output load.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 8). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 8). The IRE relationships in Figures 5 and 6 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = K1 * VREF (V) / IOG (mA)

Pin Descriptions (continued)

Pin Name	Description
	The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω) where K1 and K2 are defined as: **Setup** / **IOG** / **IOR, IOB** 7.5 IRE / K1 = 11,294 / K2 = 8,067 0 IRE / K1 = 10,684 / K2 = 7,457
VREF	Voltage reference input. An external voltage reference circuit must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 8 in the PC Board Layout Considerations section. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as shown in Table 1. They are latched on the falling edge of CE*.
D0–D8	Data bus (TTL compatible). Data is transferred into and out of the device over this 9-bit bidirectional data bus. D0 is the least significant bit.

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Pin Descriptions (continued)

Signal	Pin Number
BLANK*	N14
SYNC*	P15
SYNCOUT*	C3
CLOCK	T16
CLOCK*	T17
SCLK*	S2
VIDCLK*	R15
SELA	B14
SELB	A15
SELC	A14
SELD	C13
P0A	D5
P0B	C4
P0C	A2
P0D	B3
P1A	C2
P1B	B1
P1C	D3
P1D	E4
P2A	D2
P2B	C1
P2C	D1
P2D	E3
P3A	F2
P3B	E2
P3C	G3
P3D	F3
P4A	G1
P4B	G2
P4C	H3
P4D	H4
P5A	H1
P5B	H2
P5C	J2
P5D	J4
P6A	J3
P6B	J1
P6C	K1
P6D	K2
P7A	K3
P7B	K4
P7C	L2
P7D	L1
P8A	M3
P8B	L3
P8C	N2
P8D	M2

Signal	Pin Number
P9A	N3
P9B	P1
P9C	R1
P9D	P2
P10A	N4
P10B	P3
P10C	T1
P10D	R2
P11A	R4
P11B	P5
P11C	T4
P11D	U3
P12A	U4
P12B	R5
P12C	P6
P12D	T5
P13A	R6
P13B	U5
P13C	T6
P13D	P7
P14A	R7
P14B	U6
P14C	U7
P14D	T7
P15A	R8
P15B	P8
P15C	U8
P15D	T8
P16A	T9
P16B	P9
P16C	R9
P16D	U9
P17A	U10
P17B	T10
P17C	R10
P17D	P10
P18A	T11
P18B	U11
P18C	P11
P18D	R11
P19A	T12
P19B	U12
P19C	U13
P19D	R12

Signal	Pin Number
P20A	T13
P20B	P12
P20C	R13
P20D	U14
P21A	U15
P21B	T14
P21C	P13
P21D	R14
P22A	P16
P22B	R17
P22C	P17
P22D	N15
P23A	M16
P23B	N16
P23C	L15
P23D	M15
P24A	L17
P24B	L16
P24C	K15
P24D	K14
P25A	K17
P25B	K16
P25C	J16
P25D	J14
P26A	J15
P26B	J17
P26C	H17
P26D	H16
P27A	H15
P27B	H14
P27C	G16
P27D	G17
P28A	F15
P28B	G15
P28C	E16
P28D	F16
P29A	E15
P29B	D17
P29C	C17
P29D	D16

Pin Descriptions (continued)

Signal	Pin Number
P30A	E14
P30B	D15
P30C	B17
P30D	C16
P31A	B15
P31B	A16
P31C	C14
P31D	D13
IR	A8
IG	A7
IB	A6
VAA	B5
VAA	B9
VAA	C8
VAA	C9
VAA	D6
VAA	D8
VAA	F1
VAA	F17
VAA	G4
VAA	G14
VAA	L4
VAA	L14
VAA	M1
VAA	M17
GND	A5
GND	A9
GND	B7
GND	B8
GND	C5
GND	D9
GND	D12
GND	E1
GND	E17
GND	F4
GND	F14
GND	M4
GND	M14
GND	N1
GND	N17
GND	P4
GND	U17
COMP	D7
FSADJ	C6
VREF	C7
CE*	A3
R/W	D10
C1	A10
C0	B10

Signal	Pin Number
D0	B11
D1	A11
D2	A12
D3	C11
D4	D11
D5	B12
D6	A13
D7	C12
D8	B13

5

Pin Descriptions (continued)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T
17	N/C	P30C	P29C	P29B	GND	VAA	P27D	P26C	P26B	P25A	P24A	VAA	GND	P22C	P22B	CLK*	GND
16	P31B	N/C	P30D	P29D	P28C	P28D	P27C	P26D	P25C	P25B	P24B	P23A	P23B	P22A	N/C	CLK	N/C
15	SELB	P31A	N/C	P30B	P29A	P28A	P28B	P27A	P26A	P24C	P23C	P23D	P22D	SYNC*	VIDCLK*	N/C	P21A
14	SELC	SELA	P31C	N/C	P30A	GND	VAA	P27B	P25D	P24D	VAA	GND	BLANK*	N/C	P21D	P21B	P20D
13	D6	D8	SELD	P31D										P21C	P20C	P20A	P19C
12	D2	D5	D7	GND										P20B	P19D	P19A	P19B
11	D1	D0	D3	D4				**Bt496**						P18C	P18D	P18A	P18B
10	C1	C0	N/C	R/W										P17D	P17C	P17B	P17A
9	GND	VAA	VAA	GND				**(TOP VIEW)**						P16B	P16C	P16A	P16D
8	IR	GND	VAA	VAA										P15B	P15A	P15D	P15C
7	IG	GND	VREF	COMP										P13D	P14A	P14D	P14C
6	IB	N/C	FSADJ	VAA										P12C	P13A	P13C	P14B
5	GND	VAA	GND	P0A										P11B	P12B	P12D	P13B
4	N/C	N/C	P0B	N/C	P1D	GND	VAA	P4D	P5D	P7B	VAA	GND	P10A	GND	P11A	P11C	P12A
3	CE*	POD	SYNC-OUT*	P1C	P2D	P3D	P3C	P4C	P6A	P7A	P8B	P8A	P9A	P10B	N/C	N/C	P11D
2	POC	N/C	P1A	P2A	P3B	P3A	P4B	P5B	P5C	P6D	P7C	P8D	P8C	P9D	P10D	SCLK*	N/C
1	NO	P1B	P2B	P2C	GND	VAA	P4A	P5A	P6B	P6C	P7D	VAA	GND	P9B	P9C	P10C	N/C

alignment marker (on top)
No pin at location A1

Pin Descriptions

	T	S	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
17	GND	CLK*	P22B	P22C	GND	VAA	P24A	P25A	P26B	P26C	P27D	VAA	GND	P29B	P29C	P30C	N/C
16	N/C	CLK	N/C	P22A	P23B	P23A	P24B	P25B	P25C	P26D	P27C	P28D	P28C	P29D	P30D	N/C	P31B
15	P21A	N/C	VIDCLK*	SYNC*	P22D	P23D	P23C	P24C	P26A	P27A	P28B	P28A	P29A	P30B	N/C	P31A	SELB
14	P20D	P21B	P21D	N/C	BLANK*	GND	VAA	P24D	P25D	P27B	VAA	GND	P30A	N/C	P31C	SELA	SELC
13	P19C	P20A	P20C	P21C										P31D	SELD	D8	D6
12	P19B	P19A	P19D	P20B										VSS	D7	D5	D2
11	P18B	P18A	P18D	P18C				**Bt496**						D4	D3	D0	D1
10	P17A	P17B	P17C	P17D										R/W	N/C	C0	C1
9	P16D	P16A	P16C	P16B				**(BOTTOM VIEW)**						AGND	VAA	VAA	AGND
8	P15C	P15D	P15A	P15B										VAA	VAA	AGND	IR
7	P14C	P14D	P14A	P13D										COMP	VREF	AGND	IG
6	P14B	P13C	P13A	P12C										VAA	FSADJ	N/C	IB
5	P13B	P12D	P12B	P11B										P0A	AGND	VAA	AGND
4	P12A	P11C	P11A	GND	P20A	GND	VAA	P7B	P5D	P4D	VAA	GND	P1D	N/C	POB	N/C	N/C
3	P11D	N/C	N/C	P10B	P9A	P8A	P8B	P7A	P6A	P4C	P3C	P3D	P2D	P1C	SYNC-OUT*	P0D	CE*
2	N/C	SCLK*	P10D	P9D	P8C	P8D	P7C	P6D	P5C	P5B	P4B	P3A	P3B	P2A	P1A	N/C	POC
1	N/C	P10C	P9C	P9B	GND	VAA	P7D	P6C	P6B	P5A	P4A	VAA	GND	P2C	P2B	P1B	NO

5

PC Board Layout Considerations

PC Board Considerations

The Bt496 layout should be optimized for lowest noise on the Bt496 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt496 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8" wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 7.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 8 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Digital Signal Interconnect

The digital inputs to the Bt496 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For

example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt496 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt496 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 8 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

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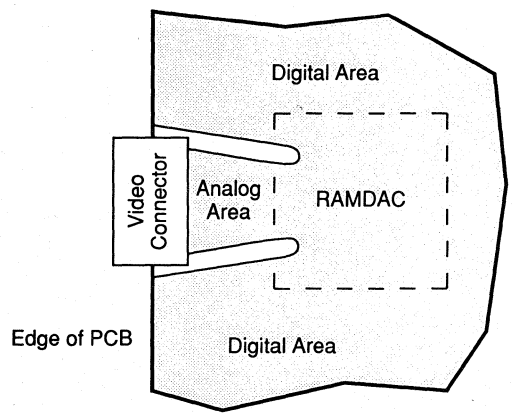
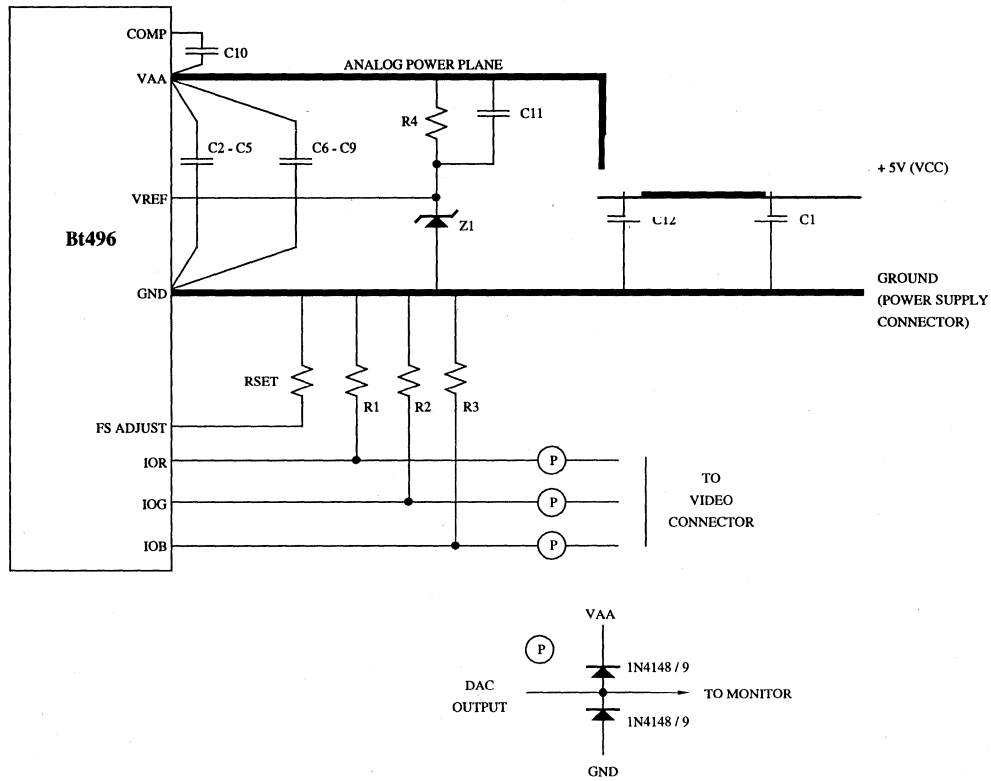


Figure 7. Representative Power/Ground Analog Area Layout.

PC Board Layout Considerations (continued)



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
R1, R2, R3	75-Ω 1% metal film resistor	Dale CMF-55C
R4	1000-Ω 1% metal film resistor	Dale CMF-55C
RSET	562 or 530-Ω 0.5% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt496.

Figure 8. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt496 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 9)

Typically, SCLK* is used to generate the pixel VRAM serial clock. Due to the low drive capability of the SCLK output, this signal should be immediately buffered by a high performance inverting buffer such as a Signetics 74F1804.

Figure 9 illustrates a sample VRAM serial clock generation circuit. Typically, VIDCLK is used for clocking the SYNC and BLANK generation logic.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt496 will not function using a single-ended clock with CLOCK* connected to ground.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by ensuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

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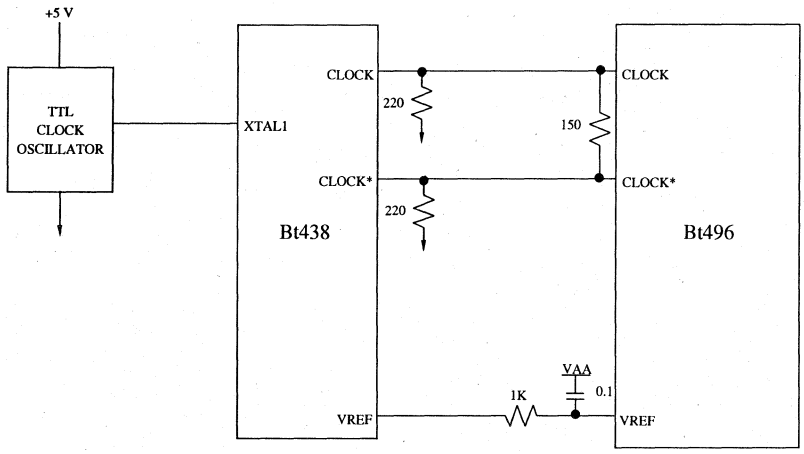

Figure 9. Generating the Bt496 Clock Signals.

Application Information (continued)

Test Features of the Bt496

The Bt496 contains a test register, three signature analysis registers, and an analog output comparator that assist the user in evaluating the performance and functionality of the part. For proper use of these test features, the test register must be enabled and the proper test method selected. Test Register ($00F) in the Internal Registers section should be referenced. During normal operation, the test register should be disabled for power considerations.

Signature Register (Signature Mode)

The signature register, when enabled (TR0 = 0), operates with three 9-bit vectors of data that are output from the color palette RAM. These three 9-bit vectors each represent a single color component of the pixel color and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs. The SARs act as three 9-bit-wide linear feedback shift registers on each succeeding pixel that is latched.

The Bt496 will only generate signatures while it is in active-display (BLANK* Negated). The SARs are available for reading and writing through the MPU port when the Bt496 is in a blanking state (BLANK* asserted).

Typically, the user will write three specific 9-bit seed values into the SARs. Then, a known pixel stream, e.g., one scan-line of pixels, will be input to the chip. At the succeeding blank state, the resultant 9-bit signatures can be read by the MPU. The 9-bit signature register data is a result of the same captured data that is fed to the DACs.

It is not simple to specify the algorithm that the linear feedback shift operation uses in the Bt496. The linear feedback configuration is shown in Figure 10. Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Signature Register (Data Strobe Mode)

Setting test register bit TR0 to "1" puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs capture and hold the pixel data that is selected. Any MPU data written to the SARs is ignored. This mode is most useful when using a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt496 is the analog output comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected with the test register. With a given setting, the respective signals (DAC outputs or the 150 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register.

Because of the comparator's swipe design, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test until capture.

Typically, users will create line-wide test bands of various colors. For each test, the result is obtained by reading test register bit D3.

Application Information (continued)

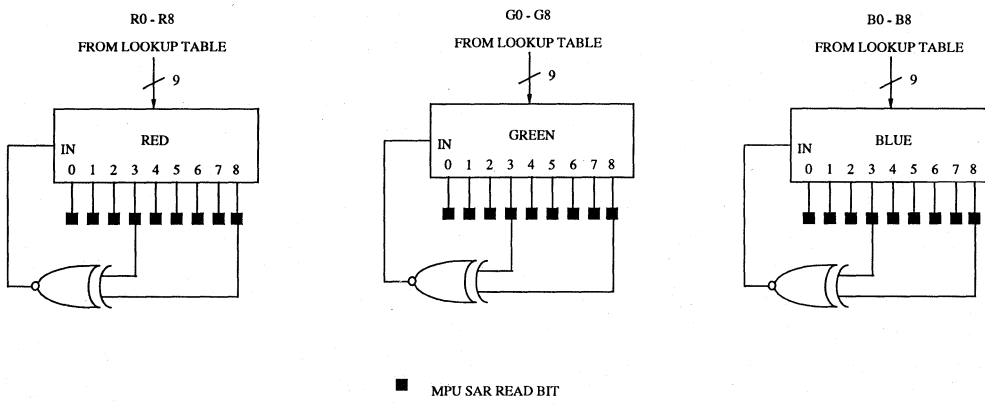

Figure 10. Signature Analysis Register Circuit.

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Application Information (continued)

Initializing the Bt496

Following a power-on, the Bt496 must be initialized. This sequence will configure the Bt496 as follows:

Pixel depth: 16 bits per pixel
Pixel unpacking mode: from MSB
RGB partitioning: 6 bits red, 5 bits green, 5 bits blue
All bits used in lookup table addressing (i.e., no masking)
Pan: 0 pixels; Zoom: 1x
Sync Enabled on IOG, 7.5 IRE blanking pedestal
VIDCLK = CLOCK/4
Midline VRAM transfer used
Signature analysis testing used

Control Register Initialization

Write $000 to Address Register
Write $014 to Command Register 0
Write $000 to Command Register 1
Write $0C0 to Command Register 2
Write $0FF to Red Pixel Read Mask Register
Write $0FF to Green Pixel Read Mask Register
Write $0FF to Blue Pixel Read Mask Register

Color Palette RAM initialization

Write $000 to Address Register
Write Red Data to Palette RAM (location $00)
Write Green Data to Palette RAM (location $00)
Write Blue Data to Palette RAM (location $00)
Write Red Data to Palette RAM (location $01)
Write Green Data to Palette RAM (location $01)
Write Blue Data to Palette RAM (location $01)

Write Red Data to Palette RAM (location $FF)
Write Green Data to Palette RAM (location $FF)
Write Blue Data to Palette RAM (location $FF)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		562		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin *(Note 1)*		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
PQFP	TJ			+150	°C
PGA	TJ			+175	°C
					°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins and should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		9	9	9	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)	DVIN	0.6		6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D8), SCLK*, VIDCLK.					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.0 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			37		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 562 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	100 MHz	Units
Clock Rate	Fmax	max	110	MHz
R/W, C1,C0 Setup Time	1	min	0	ns
R/W, C1,C0 Hold Time	2	min	15	ns
CE* Low Time	3	min	50	ns
CE* High Time	4	min	25	ns
CE* Asserted to Data Bus Driven	5	min	7	ns
CE* Asserted to Data Valid	6	max	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	ns
Write Data Setup Time	8	min	35	ns
Write Data Hold Time	9	min	3	ns
Pixel and Control Setup Time	10	min	0	ns
Pixel and Control Hold Time	11	min	6	ns
Clock Cycle Time	12	min	10	ns
Clock Pulse Width High Time	13	min	4.5	ns
Clock Pulse Width Low Time	14	min	4.5	ns

See test conditions on next page.

AC Characteristics (continued)

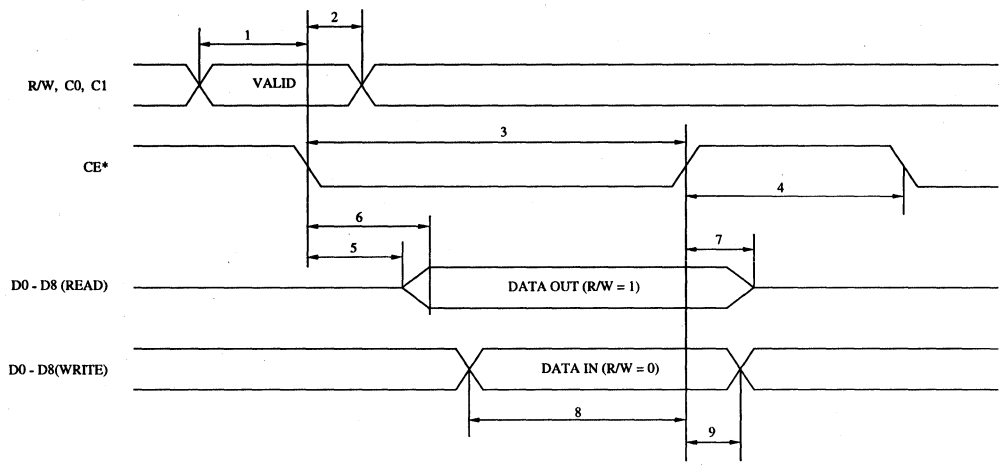
Parameter	Symbol	Min/Typ/ Max	100 MHz	Units
Analog Output Delay	18	typ	12	ns
Analog Output Rise/Fall Time	19	typ	1.5	ns
Analog Output Settling Time	20	max	8	ns
Clock and Data Feedthrough *(Note 1)*		typ	tbd	dB
Glitch Impulse *(Note 1)*		typ	50	pV – sec
DAC-to-DAC Crosstalk		typ	tbd	dB
Analog Output Skew		typ	0	ns
		max	2	ns
SYNC*, BLANK* Setup Time	21	min	3	ns
SYNC*, BLANK* Hold Time	22	min	10	ns
Pipeline Delay		min	tbd	Clocks
		max	tbd	Clocks
VAA Supply Current *(Note 2)*	IAA	typ	tbd	mA
		max	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 562 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 3 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF and D0–D8 output load ≤40 pF. See notes 1–3 in the Pixel Input/Output Timing diagram. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

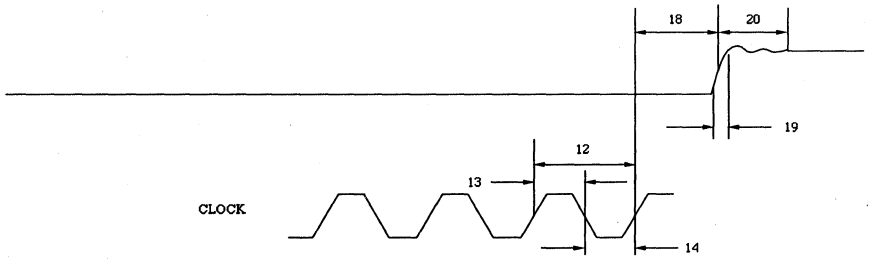
Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms



MPU Read/Write Timing Dimensions.



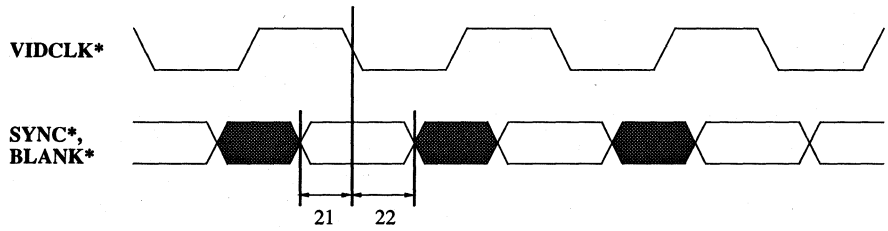
Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Pixel Input/Output Timing.

Timing Waveforms (continued)



Video Control Input Timing.

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Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt496KG100	100 MHz	207-pin Ceramic PGA	0° to +70° C

Section 6

VIDEODACs

Brooktree®

Contents

Bt101

50 MHz Monolithic CMOS Triple 8-bit VIDEODAC™

Distinguishing Features

- 50, 30 MHz Operation
- Triple 8-bit D/A Converters
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170-Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

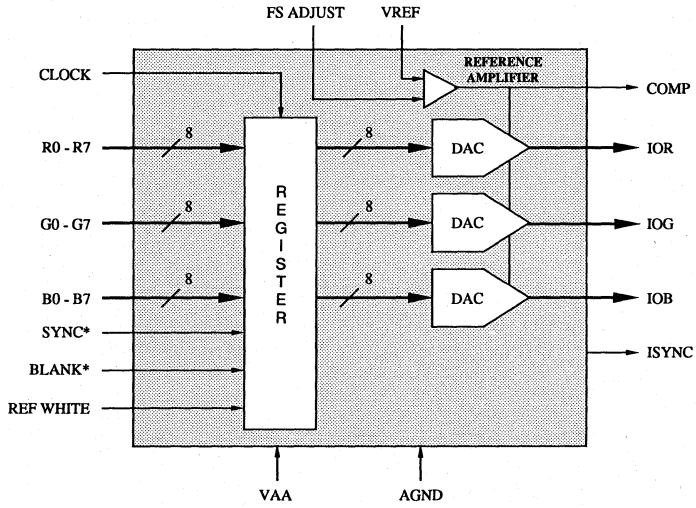
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt473, Bt121

Functional Block Diagram



Product Description

The Bt101 is a triple 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog outputs to the reference white level, regardless of the data inputs.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt101 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load and RS-170-compatible video signals into a singly-terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L101001 Rev. J

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt101 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown in Figure 1, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, forces the inputs of each D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output levels.

The ISYNC current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If ISYNC is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG, and IOB outputs will have the same full-scale output current.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 Ω for generation of RS-343A video into a 37.5 Ω load. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and should provide a low-impedance output.

The D/A converters on the Bt101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt101 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

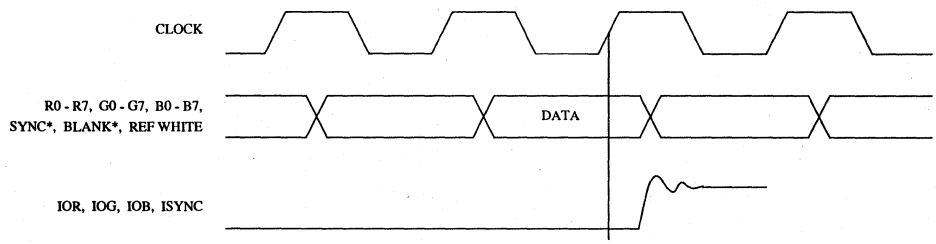
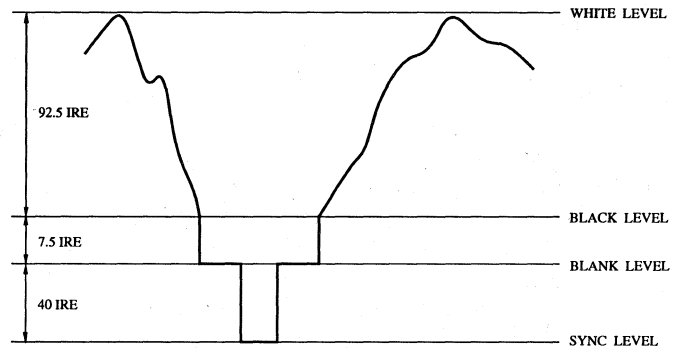


Figure 1. Input/Output Timing.

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 542 Ω, and VREF = 1.2 V. ISYNC is connected to IOG. RS-343A levels and tolerances are assumed on all levels.

Figure 2. Composite Video Output Waveforms.

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Description	IOG (mA)	IOR, IOB (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	1	$xx
WHITE	26.67	19.05	0	1	1	$FF
DATA	data + 9.05	data + 1.44	0	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	0	1	data
BLACK	9.05	1.44	0	1	1	$00
BLACK–SYNC	1.44	1.44	0	0	1	$00
BLANK	7.62	0	x	1	0	$xx
SYNC	0	0	x	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 542 Ω and VREF = 1.2 V. ISYNC is connected to IOG.

Table 1. Video Output Truth Table.

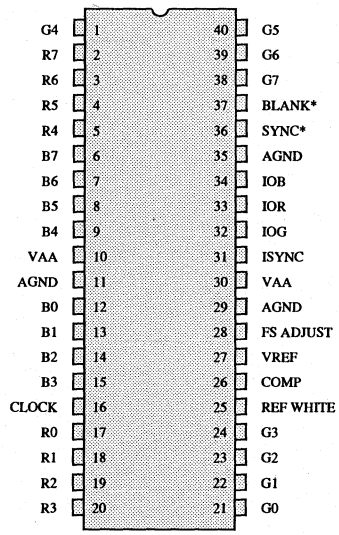
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as specified in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R7, G0–G7, B0–B7, and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 2). SYNC* does not override any other control or data input, as specified in Table 1; therefore, SYNC* should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R0–R7, G0–G7, and B0–B7 inputs. It is latched on the rising edge of CLOCK (see Table 1).
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. Typically, this current output is directly wired to the IOG output and enables sync information to be encoded onto the green channel. A logical zero on the SYNC* input causes no current to be output onto this pin, while a logical one causes the following current output: ISYNC (mA) = 3,442 * VREF (V) / RSET (Ω) If sync information is not required on the green channel, this output should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG (assuming ISYNC is connected to IOG) is: RSET (Ω) = 12,046 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 8,604 * VREF (V) / RSET (Ω)

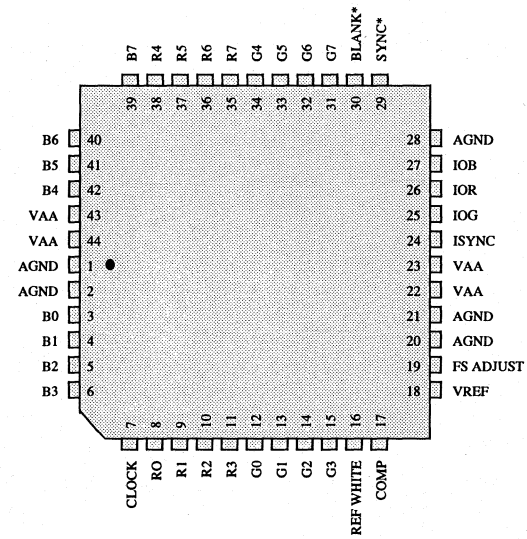
Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor in series with a resistor must be connected between this pin and the nearest VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
AGND	Analog ground. All AGND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.

40-pin CERDIP Package.



44-pin Plastic J-Lead (PLCC) Package.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt101 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated VIDEODAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt101 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt101 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt101. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 3 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

To optimize the settling time of the Bt101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time. An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

The COMP pin and series resistor must also be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

PC Board Layout Considerations *(continued)*

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt101 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt101 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the VIDEODAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Analog Signal Interconnect

The Bt101 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt101 to minimize reflections. Unused analog outputs should be connected to GND.

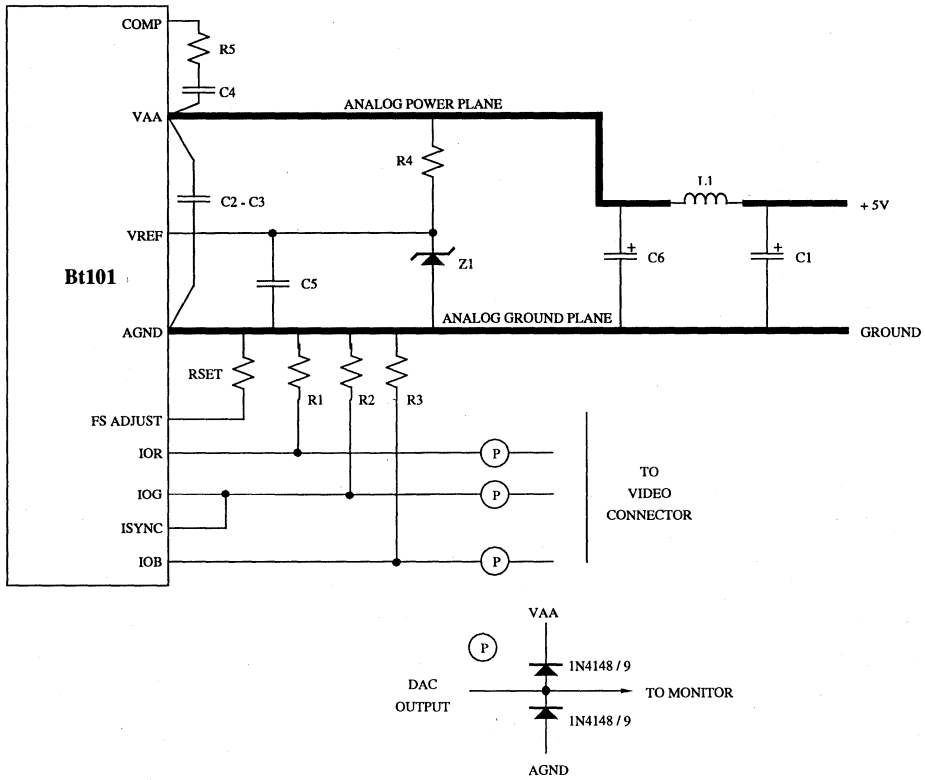
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt101 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C4, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
R5	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	549 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt101.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75 Ω load be used with an RSET value of about 774 Ω. If the Bt101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75 Ω and singly-terminated 75 Ω loads.

If the user is driving a large capacitive load [i.e., if load RC > 1/(20 fcπ) (where fc = clock frequency)], it is recommended that an output buffer be used to drive a doubly-terminated 75 Ω load.

NonVideo Applications

The Bt101 may be used in nonvideo applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be logical zeros and BLANK* should be a logical one. ISYNC should be connected to AGND. All three outputs will have the same full-scale output current.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}958 * VREF\ (V) / Iout\ (mA)$$

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 650 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a force-to-full-scale control.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA				
Bt101KC30, Bt101KPJ		0		+70	°C
Bt101BC		–25		+85	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.14	1.20	1.26	V
FS ADJUST Resistor	RSET		542		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	V
Voltage on any Signal Pin (Note 1)		AGND – 0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL		±0.3	±1	LSB
Differential Linearity Error	DL		±0.3	±1	LSB
Gray-Scale Error			±1	±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	AGND – 0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2		%
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Voltage Reference Input Current	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω, VREF = 1.200 V, and ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

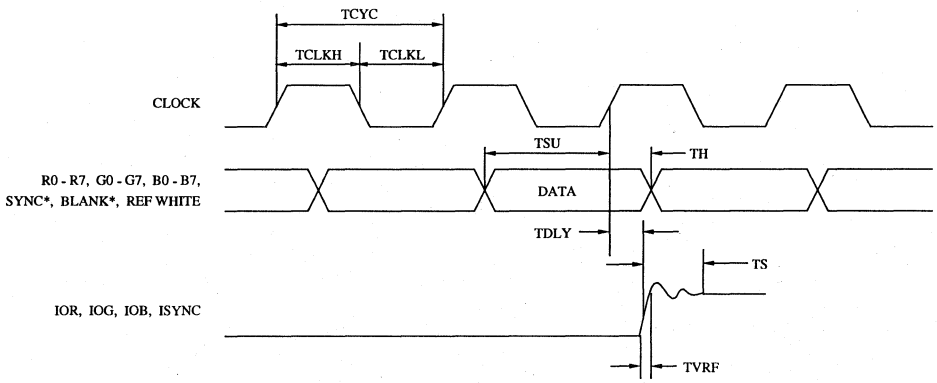
		50 MHz Devices			30 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time	TSU	6			8			ns
Data and Control Hold Time	TH	2			2			ns
Clock Cycle Time	TCYC	20			33.3			ns
Clock Pulse Width High Time	TCLKH	8			10			ns
Clock Pulse Width Low Time	TCLKL	8			10			ns
Analog Output Delay	TDLY		25			25		ns
Analog Output Rise/Fall Time	TVRF			8			9	ns
Analog Output Settling Time	TS		12			15		ns
Clock and Data Feedthrough (Note 1)			–28			–28		dB
Glitch Impulse (Note 1)			100			100		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	3		0	3	ns
Differential Gain Error	DG		1.8			1.8		% Gray Scale
Differential Phase Error	DP		1.2			1.2		Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current (Note 2)	IAA		120	175		100	140	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω, VREF = 1.200 V, ISYNC connected to IOG. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. COMP resistor = 15 Ω. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

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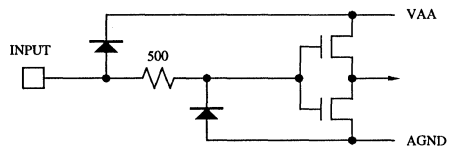
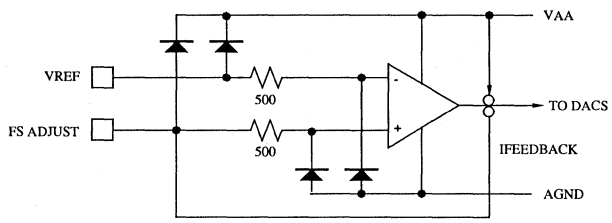
Figure 4. Input/Output Timing.

Ordering Information

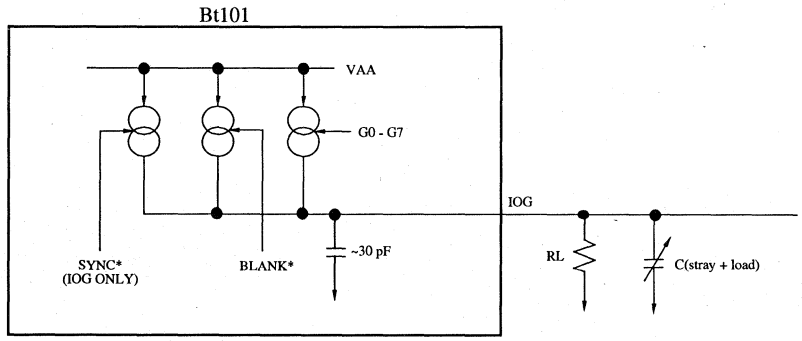
Model Number	Speed	Package	Ambient Temperature Range
Bt101BC	50 MHz	40-pin 0.6" CERDIP	–25° to +85° C
Bt101KC30	30 MHz	40-pin 0.6" CERDIP	0° to +70° C
Bt101KPJ	30 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt101EVM	Evaluation Board for the Bt101		



Equivalent Circuit of the Digital Inputs.



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output (IOG).

Bt103

75 MHz Monolithic CMOS Triple 4-bit VIDEODAC™

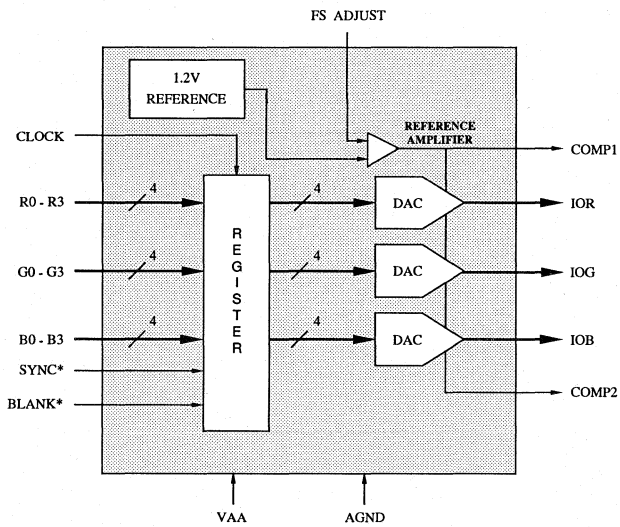
Distinguishing Features

- 75, 30 MHz Operation
- Triple 4-bit D/A Converters
- ±1/16 LSB Differential Linearity Error
- ±1/8 LSB Integral Linearity Error
- RS-343A/RS-170-Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 28-pin DIP Package
- Typical Power Dissipation: 800 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Functional Block Diagram



Product Description

The Bt103 is a triple 4-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync and blank, both pipelined to maintain synchronization with the color data. An on-chip voltage reference simplifies design, and a single external resistor controls the full-scale output current.

The Bt103 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load and RS-170-compatible video signals into a singly-terminated 75 Ω load, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/16 LSB and ±1/8 LSB, respectively, over the full temperature range.

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(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L103001 Rev. F

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt103 contains three 4-bit D/A converters, input registers, voltage reference, and a reference amplifier.

As shown in Figure 1, on the rising edge of each clock cycle, 12 bits of color information (R0–R3, G0–G3, and B0–B3) are latched into the device and presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK and pipelined to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 499 Ω for generation of RS-343A video into a 37.5 Ω load.

The D/A converters on the Bt103 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt103 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

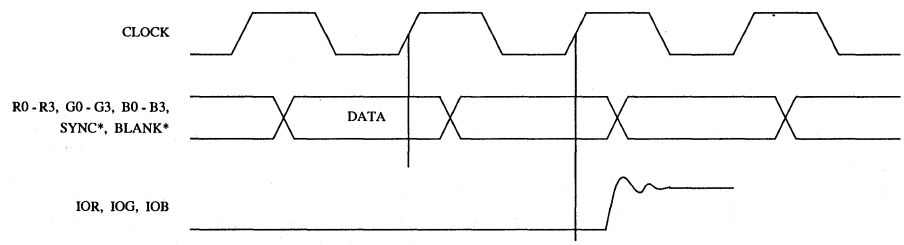
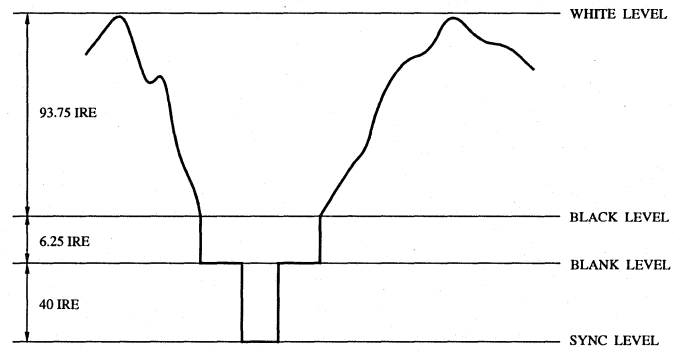


Figure 1. Input/Output Timing.

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.19	0.045	8.81	0.330
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load and RSET = 499 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 2.Composite Video Output Waveforms.

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Description	IOG (mA)	IOR (mA)	IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	19.05	1	1	$F
DATA	data + 8.81	data + 1.19	data + 1.19	1	1	data
DATA–SYNC	data+ 1.19	data + 1.19	data + 1.19	0	1	data
BLACK	8.81	1.19	1.19	1	1	$0
BLACK–SYNC	1.19	1.19	1.19	0	1	$0
BLANK	7.62	0	0	1	0	$x
SYNC	0	0	0	0	0	$x

Note: Typical with full-scale IOG = 26.67 mA. RSET = 499 Ω.

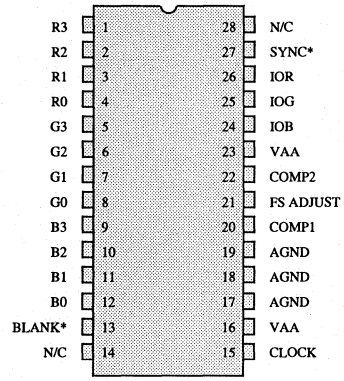
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R3, G0–G3, and B0–B3 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as specified in Table 1; therefore, SYNC* should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK.
R0–R3, G0–G3, B0–B3	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R3, G0–G3, B0–B3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = 13,308 / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 9,506 / RSET (Ω)

Pin Descriptions *(continued)*

Pin Name	Description
COMP1, COMP2	Compensation pins. These pins provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between these two pins (Figure 3). The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.



Note: N/C pins may be left floating without affecting the performance of the Bt103.

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PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt103 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated VIDEODAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt103 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt103 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt103. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each VAA pin to AGND. The capacitors should be placed as close as possible to the device VAA and AGND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 3 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

To optimize the settling time of the Bt103, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time. An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

To reduce low-frequency supply noise a larger COMP capacitor value may be required.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt103 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt103 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the VIDEODAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Analog Signal Interconnect

The Bt103 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt103 to minimize reflections. Unused analog outputs should be connected to GND.

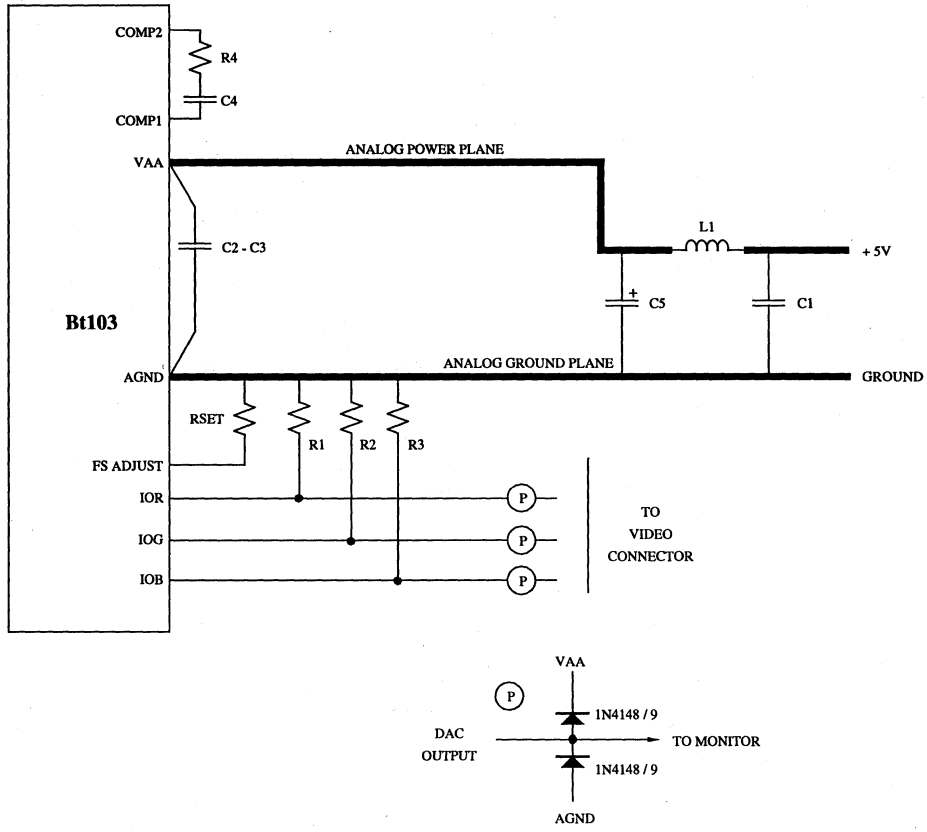
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt103 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1, C2, C3, C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	22 Ω 1% metal film resistor	Dale CMF-55C
RSET	499 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt103.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170-compatible video, it is recommended that a singly-terminated 75 Ω load be used with an RSET value of about 713 Ω. If the Bt103 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75 Ω and singly-terminated 75 Ω loads.

If the user is driving a large capacitive load [i.e., if load RC >1/(20 fcπ) (where fc = clock frequency)], it is recommended that an output buffer be used to drive a doubly-terminated 75 Ω load.

NonVideo Applications

The Bt103 may be used in nonvideo applications by disabling the video-specific control inputs. SYNC* should be a logical zero, and BLANK* should be a logical one. All three outputs will have the same full-scale output current.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 8{,}912 / Iout\ (mA)$$

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 594 / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA				
Bt103KC30		0		+70	°C
Bt103BC		–25		+85	°C
Output Load	RL		37.5		Ω
FS ADJUST Resistor	RSET		499		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	V
Voltage on any Signal Pin (Note 1)		AGND – 0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/8	LSB
Differential Linearity Error	DL			±1/16	LSB
Gray-Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	AGND – 0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH	–200		–1200	µA
Input Low Current (Vin = 0.4 V)	IIL	–200		–1200	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		16.88	19.05	20.69	mA
White Level Relative to Black		15.86	17.62	19.38	mA
Black Level Relative to Blank		1.02	1.19	1.31	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			1.175		mA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		20		pF
Internal Voltage Reference	VREF		1.2		V
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

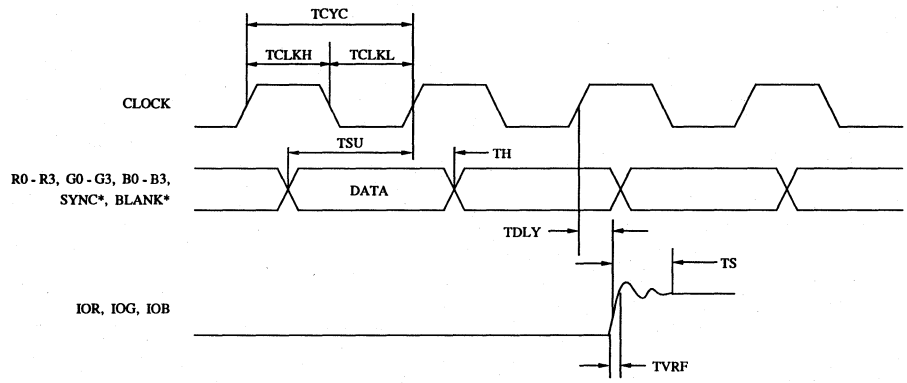
Parameter	Symbol	75 MHz Devices			30 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			75			30	MHz
Data and Control Setup Time	TSU	4			10			ns
Data and Control Hold Time	TH	1			2			ns
Clock Cycle Time	TCYC	13.3			33.3			ns
Clock Pulse Width High Time	TCLKH	5			10			ns
Clock Pulse Width Low Time	TCLKL	5			10			ns
Analog Output Delay	TDLY		12			12		ns
Analog Output Rise/Fall Time	TVRF			4			9	ns
Analog Output Settling Time (Note 1)	TS		12			15		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			50			50		pV - sec
DAC-to-DAC Crosstalk			–25			–25		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		2	2	2	2	2	2	Clocks
VAA Supply Current (Note 2)	IAA			175			110	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 Ω. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. COMP resistor = 22 Ω. Output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (max) at VAA = 5.25 V.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1/8 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

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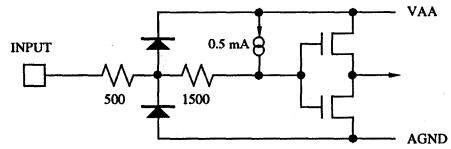
Figure 4. Input/Output Timing.

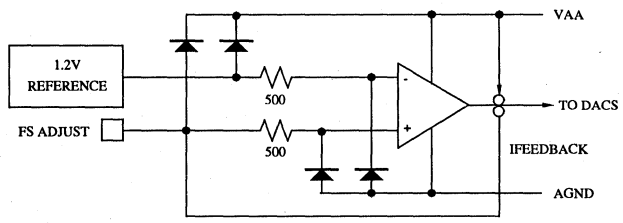
Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt103BC	75 MHz	28-pin 0.6" CERDIP	–25° to +85° C
Bt103KC30	30 MHz	28-pin 0.6" CERDIP	0° to +70° C
Bt103EVM	Evaluation Board for the Bt103		

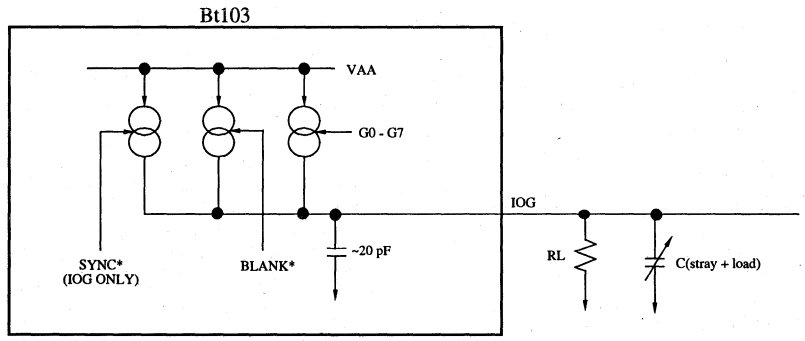


High-speed operation is accomplished with pipelining and a unique (patent-pending) TTL input buffer. This input buffer features a resistive level shifter that uses a temperature and process-compensated current source.

Equivalent Circuit of the Digital Inputs.



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output (IOG).

Bt106

50 MHz Monolithic CMOS Single 8-bit VIDEODAC™

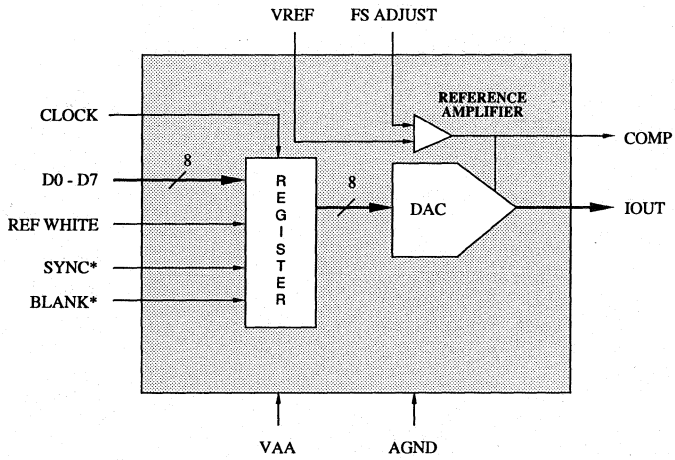
Distinguishing Features

- 50, 30 MHz Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170-Compatible Output
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 20-pin DIP Package
- Typical Power Dissipation: 400 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Functional Block Diagram



Product Description

The Bt106 is an 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog output to the reference white level, regardless of the data inputs.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt106 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load, and RS-170-compatible video signals into a singly- terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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L106001 Rev. H

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt106 contains an 8-bit D/A converter, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown in Figure 1, 8 bits of data are latched into the device and presented to the 8-bit D/A converter. The REF WHITE input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog output, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output level.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 Ω for generation of RS-343A video into a 37.5 Ω load. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and should provide a low-impedance output.

The D/A converter on the Bt106 uses a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt106 can directly drive a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

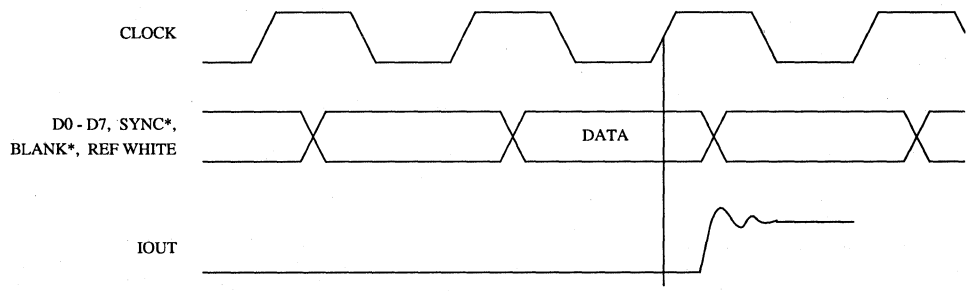
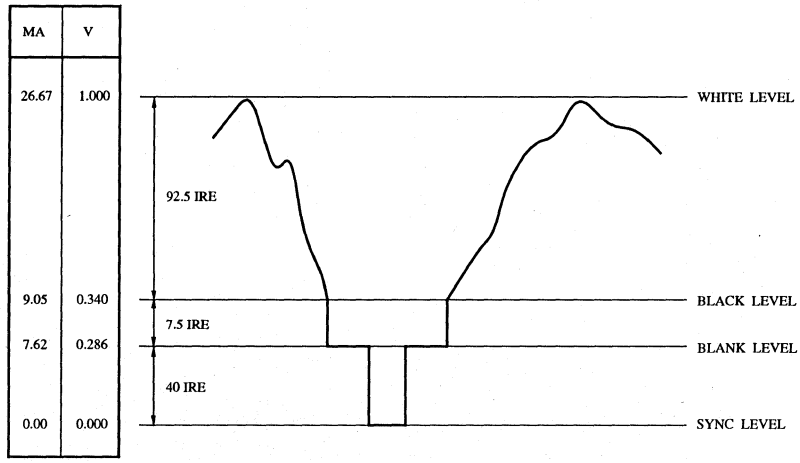


Figure 1. Input/Output Timing.

Circuit Description *(continued)*



Note: 75 Ω doubly-terminated load, RSET = 542 Ω, and VREF = 1.2 V. RS-343A levels and tolerances are assumed on all levels.

Figure 2. Composite Video Output Waveform.

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Description	IOUT (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	1	$xx
WHITE	26.67	0	1	1	$FF
DATA	data + 9.05	0	1	1	data
DATA - SYNC	data + 1.44	0	0	1	data
BLACK	9.05	0	1	1	$00
BLACK - SYNC	1.44	0	0	1	$00
BLANK	7.62	x	1	0	$xx
SYNC	0	x	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 542 Ω and VREF = 1.2 V.

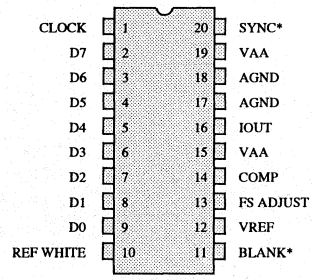
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOUT output to the blanking level, as specified in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0–D7 and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the output (see Figure 2). SYNC* does not override any other control or data input, as specified in Table 1; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the output to the white level, regardless of the D0–D7 inputs. It is latched on the rising edge of CLOCK (see Table 1).
D0–D7	Data inputs (TTL compatible). D0 is the least significant data bit. D0–D7 are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the D0–D7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOUT	Current output. This high-impedance current source can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 3).
AGND	Analog ground. All AGND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
FSADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: RSET (Ω) = 12,046 * VREF (V) / IOUT (mA)

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as that shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The Bt106 has an internal pullup resistor between VAA and VREF. As the value of this resistor may vary slightly because of process variations, the use of a resistor network to generate the reference is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to AGND, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.



6

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt106 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated VIDEODAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt106 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt106 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt106. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each VAA pin to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 3 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

To optimize the settling time of the Bt106, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time. An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

The COMP pin and series resistor must also be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

To reduce low-frequency supply noise a larger COMP capacitor value may be required.

PC Board Layout Considerations *(continued)*

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt106 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt106 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the VIDEODAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Analog Signal Interconnect

The Bt106 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt106 to minimize reflections. Unused analog outputs should be connected to GND.

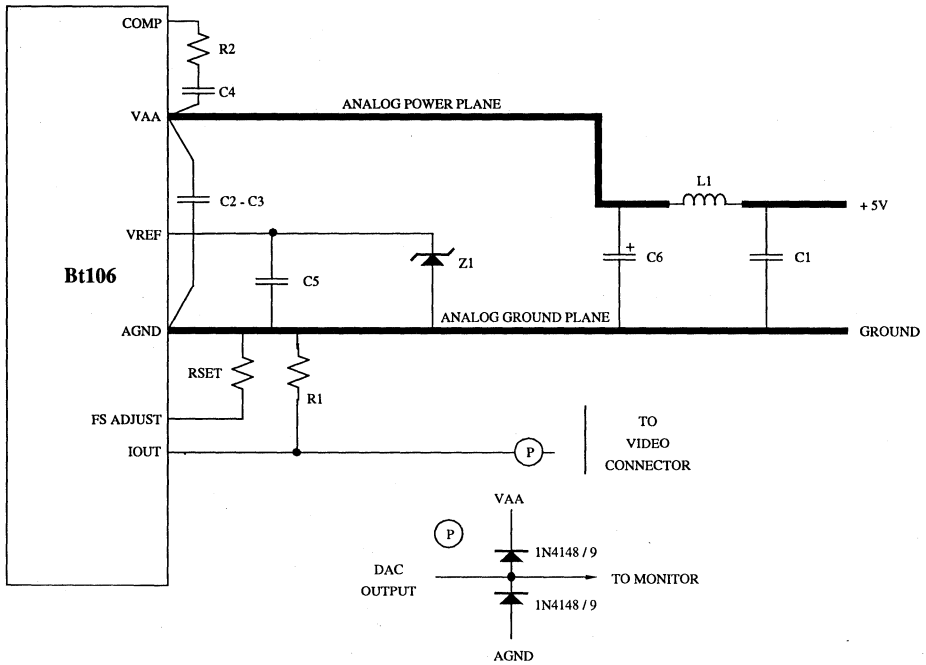
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt106 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	12 Ω 1% metal film resistor	Dale CMF-55C
RSET	542 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt106.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170-compatible video, it is recommended that a singly-terminated 75 Ω load be used with an RSET value of about 774 Ω. If the Bt106 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75 Ω and singly-terminated 75 Ω loads.

If the user is driving a large capacitive load [i.e., if load RC > 1/(20 fcπ) (where fc = clock frequency)], it is recommended that an output buffer be used to drive a doubly-terminated 75 Ω load.

Color Applications

In color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may be logical zeros. If SYNC* is always logical zeros, the relationship between RSET and the full-scale output current is:

$$IOUT\ (mA) = 8{,}604 * VREF\ (V) / RSET\ (\Omega)$$

Using Multiple Devices

If they are close together on the same PC board, multiple Bt106 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt106 must still have its own RSET resistor, IOUT termination resistor (R1 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R2 in Figure 3).

Nonvideo Applications

The Bt106 may be used in nonvideo applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be logical zeros and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}958 * VREF\ (V) / IOUT\ (mA)$$

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 650 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a force-to-full-scale control.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA				
Bt106KC30		0		+70	°C
Bt106BC		–25		+85	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.14	1.20	1.26	V
FS ADJUST Resistor	RSET		542		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	V
Voltage on Any Signal Pin (Note 1)		AGND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	AGND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω and VREF = 1.200 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

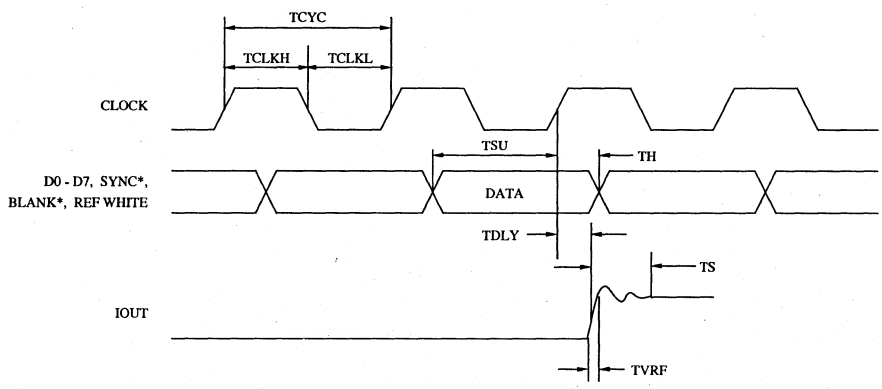
		50 MHz Devices			30 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time Data and Control Hold Time	TSU TH	8 2			8 2			ns ns
Clock Cycle Time Clock Pulse Width High Time Clock Pulse Width Low Time	TCYC TCLKH TCLKL	20 8 8			33.3 10 10			ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time (Note 1) Clock and Data Feedthrough (Note 1) Glitch Impulse (Note 1)	TDLY TVRF TS		25 20 –33 50	 8 		25 25 –33 50	 9 	ns ns ns dB pV - sec
Differential Gain Error Differential Phase Error	DG DP		1.8 1.2			1.8 1.2		% Gray Scale Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current (Note 2)	IAA		80	100		60	75	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω and VREF = 1.200 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. COMP resistor = 12 Ω. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 4. Input/Output Timing.

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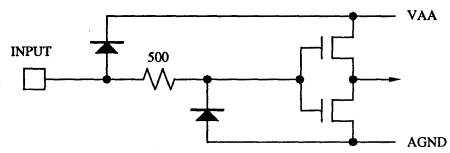
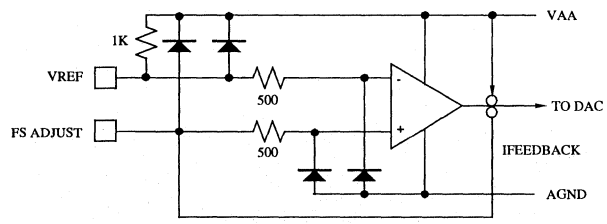
Ordering Information

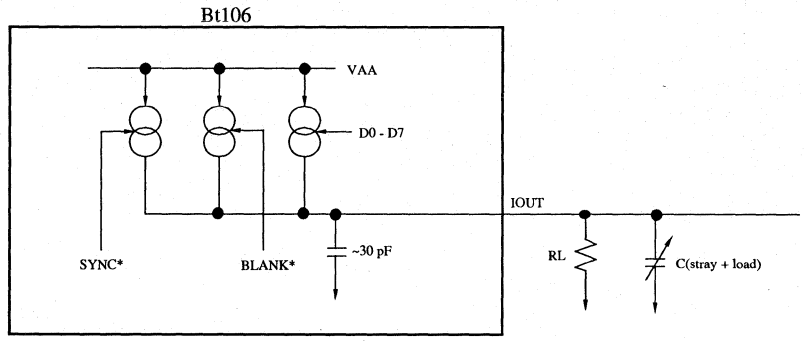
Model Number	Speed	Package	Ambient Temperature Range
Bt106BC	50 MHz	20-pin 0.3" CERDIP	–25° to +85° C
Bt106KC30	30 MHz	20-pin 0.3" CERDIP	0° to +70° C
Bt106EVM	Evaluation Board for the Bt106		



Equivalent Circuit of the Digital Inputs.



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output.

Bt107

400 MHz 10KH/100K ECL 8-bit Multiplexed Input VIDEODAC™

Distinguishing Features

- 400 MHz Pipelined Operation
- ±1/2 LSB Differential Linearity Error
- ±1/2 LSB Integral Linearity Error
- 500 ps Typical Rise/Fall Time
- RS-343A-Compatible Output
- 0 or 7.5 IRE Blanking Pedestal
- Ability to Handle 25 Ω Output Loads
- 10KH and 100K ECL-Compatible I/O
- 2:1 Multiplexed Pixel Inputs
- 32-pin Flatpack Package
- Typical Power Dissipation: 1 W

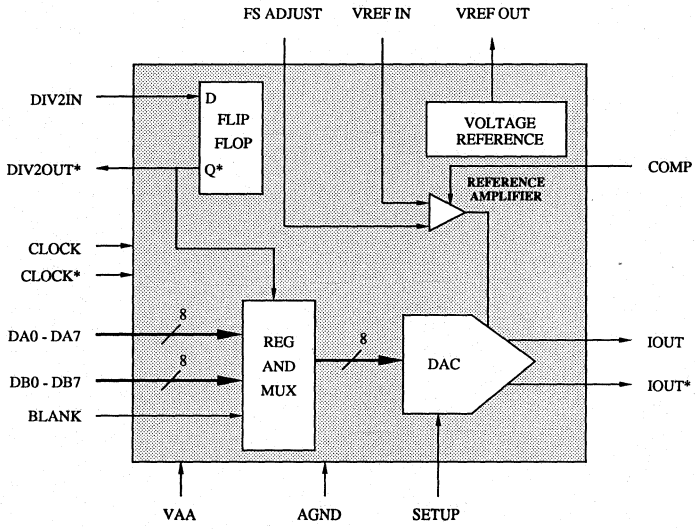
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Radar Processing
- Instrumentation

Related Products

- Bt109
- Bt401/403
- Bt424
- Bt492

Functional Block Diagram



Product Description

The Bt107 is an 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

Multiplexed pixel inputs enable pixel data to be latched into the Bt107 at a 200 MHz data rate while maintaining the 400 MHz output rate necessary for high-resolution graphics. On-chip circuitry divides the pixel clock by 2, generating the 200 MHz clock signal.

An on-chip voltage reference is available, or an external reference may be used. A single external resistor controls the full-scale output current.

The Bt107 generates an RS-343A-compatible video signal, and can drive either doubly-terminated 75 Ω or 50 Ω coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1/2 LSB over the full temperature range.

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L107001 Rev. G

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt107 contains a single 8-bit D/A converter, 2:1 multiplexed input register, a voltage reference, and a reference amplifier.

Pixel data on the DA0–DA7 (even data) and DB0-DB7 (odd data) are latched on the falling edge of DIV2OUT*, as illustrated in Figure 1.

DIV2IN is defined to be 1/2 the CLOCK rate. To simplify system design, the Bt107 outputs a DIV2OUT* signal which, when connected to the DIV2IN pin, generates a clock equal to one half the CLOCK rate. For a color system requiring three Bt107s, the DIV2OUT* signals may be synchronized by connecting the DIV2OUT* signal on one of the devices to the DIV2IN pins of all three devices. Signal paths must remain short and equal for each connection. The unused DIV2OUT* signals from the remaining Bt107s can be used to clock external lookup table RAMs.

The BLANK input is also latched on the falling edge of DIV2OUT*, and overrides the DA0–DA7 and DB0–DB7 data. Blanking information is output synchronously with the even pixel data.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 1092 Ω for generation of RS-343A video into a 37.5 Ω load, or 729 Ω for generation of RS-343A video into a 25 Ω load. Specific video output levels are shown in Figure 2. The on-chip voltage reference (VREF OUT) may be used to provide the reference for the VREF IN pins of up to three Bt107s, or an external reference may be used.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOUT output through a 25 Ω resistor to AGND (assuming a doubly-terminated 50 Ω load). The IOUT* output is used to generate the video signal. Table 1 specifies the video output truth table.

The D/A converter on the Bt107 uses a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt107 can directly drive either a 37.5 Ω or 25 Ω load, such as a doubly-terminated 75 Ω or 50 Ω coaxial cable.

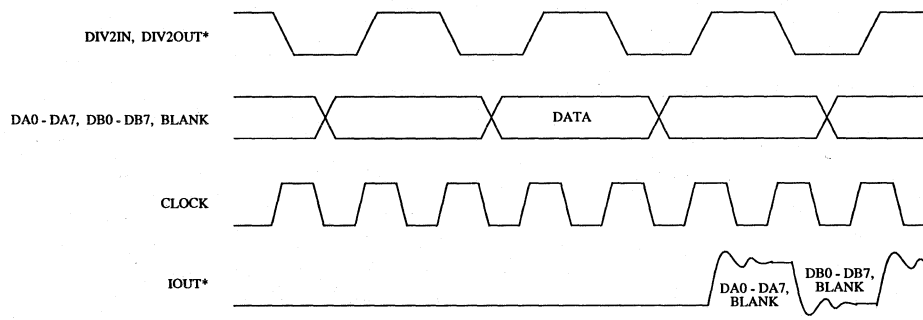
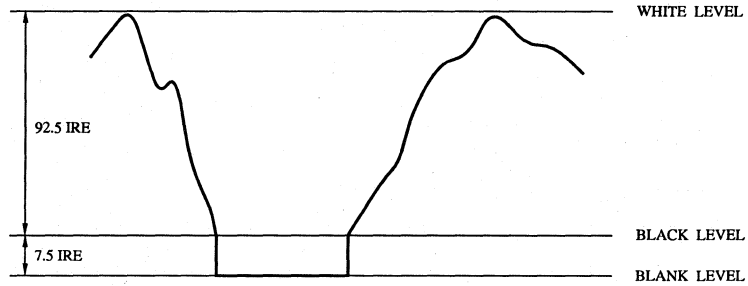


Figure 1. Input/Output Timing (DIV2IN connected to DIV2OUT).*

Circuit Description *(continued)*

MA RSET = 729	MA RSET = 1092	V
00.00	00.00	0.000
- 26.40	- 17.60	- 0.660
- 28.56	- 19.05	- 0.714



Note: RSET = 729 Ω (50 Ω doubly-terminated load) or 1092 Ω (75 Ω doubly-terminated load), and VREF IN = –1.21 V. RS-343A levels and tolerances are assumed on all levels.

Figure 2. Composite Video Output Waveform (IOUT*).

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Description	RSET = 729 Ω IOUT* (mA)	RSET = 1092 Ω IOUT* (mA)	BLANK	DAC Input Data
WHITE	0	0	0	$FF
DATA	data	data	0	data
BLACK	–26.40	–17.62	0	$00
BLANK			1	$xx
SETUP = AGND	–26.40	–17.62		
SETUP = float	–28.56	–19.05		

Note: Typical with VREF IN = –1.21 V.

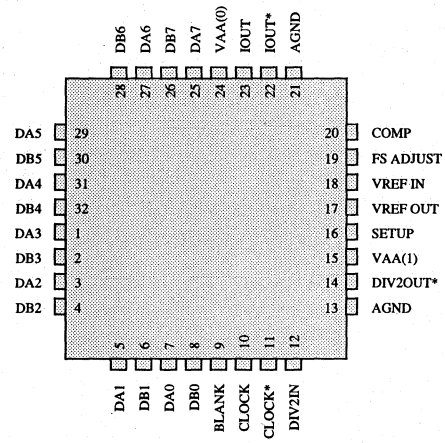
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logical one drives the analog output to the blanking level, as specified in Table 1. It is latched on the falling edge of DIV2OUT*. When BLANK is a logical one, the DA0–DA7 and DB0–DB7 inputs are ignored. Blanking information is output synchronously with the even pixel data.
DA0–DA7, DB0–DB7	Even and odd pixel data inputs (ECL compatible). D0 is the least significant data bit. They are latched on the falling edge of DIV2OUT*. Even data represents the first (leftmost) pixel on the display screen. DAx represent the even pixel data, and DBx represent the odd pixel data. Coding is binary.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The CLOCK input is typically the pixel clock rate of the video system. The Bt107 may be operated with a single-ended clock by connecting CLOCK* to a –1.3 V VBB; however, common mode noise immunity at high clock rates may degrade.
DIV2IN	CLOCK/2 input (ECL compatible). This clock must be one half the CLOCK rate. It is used to latch the BLANK, DAx, and DBx inputs (see Figure 1).
DIV2OUT*	CLOCK/2 output (ECL compatible). When connected to the DIV2IN pin, this output is one half the CLOCK rate. When not connected to DIV2IN, this output generates a signal that is DIV2IN-synchronized to CLOCK and inverted. DIV2OUT* must be terminated to –2 V.
IOUT, IOUT*	Differential video current outputs. These high impedance current sources can directly drive either a doubly-terminated 50 Ω or 75 Ω coaxial cable (Figure 3). Both outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected. *Warning: A ferrite bead must be used to connect the VAA(1) power pin to the analog power plane, as illustrated in Figure 3. Connecting the decoupling capacitors directly to the VAA (1) pin will result in unstable operation.*
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 ceramic chip capacitor must be connected between this pin and VAA(0) (Figure 3). Connecting the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.
SETUP	Pedestal control input. If SETUP is connected to AGND, the blanking pedestal on the output is disabled, making the black and blanking levels the same (0 IRE). If SETUP is left floating, the 7.5 IRE blanking pedestal is enabled (see Figure 2).

Pin Descriptions *(continued)*

Pin Name	Description
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 3). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: RSET (Ω) = K * VREF IN (V) / IOUT (mA) where K = 17,205 if SETUP = float or 15,915 if SETUP = AGND. *Note*: The RSET value may require adjustment to generate the specified video levels because of variations in processing and depending on whether the internal or an external reference is used.
VREF OUT	Voltage reference output. This output provides a –1.2 V (typical) reference, and may be connected to the VREF IN inputs of up to three Bt107s. When multiple Bt107s are driven, 100 Ω interconnect resistance should be used to minimize noise pickup. If it is not used to provide a voltage reference, it should remain floating.
VREF IN	Voltage reference input. An external voltage reference, such as the one shown in Figure 4, or the VREF OUT pin must supply this input with a –1.2 V (typical) reference. A 0.01 µF ceramic chip capacitor in parallel with a 0.001 µF ceramic chip capacitor must be connected between this pin and VAA(0), as shown in Figure 3. The decoupling capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt107 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The Bt107 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt107.

The analog ground plane area should encompass all Bt107 ground pins, power supply bypass circuitry for the Bt107, any external voltage reference circuitry, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading to the Bt107.

Power Planes

The Bt107 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt107.

The PCB power plane should provide power to all digital logic on the PC board. The analog power plane should provide power to all Bt107 power pins, any external voltage reference circuitry, and any output amplifiers.

Portions of the regular PCB power and ground planes must not overlay portions of the analog power or ground planes unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the VAA(1) power pin and the analog power plane, as illustrated in Figure 3. The ferrite bead must be located as close as possible to the VAA(1) pin.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the VAA(1) pin, as illustrated in Figure 3. Connecting the bypass capacitors directly to the VAA(1) pin will result in unstable operation caused by high-frequency oscillations.

Digital Signal Interconnect

The digital inputs to the Bt107 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

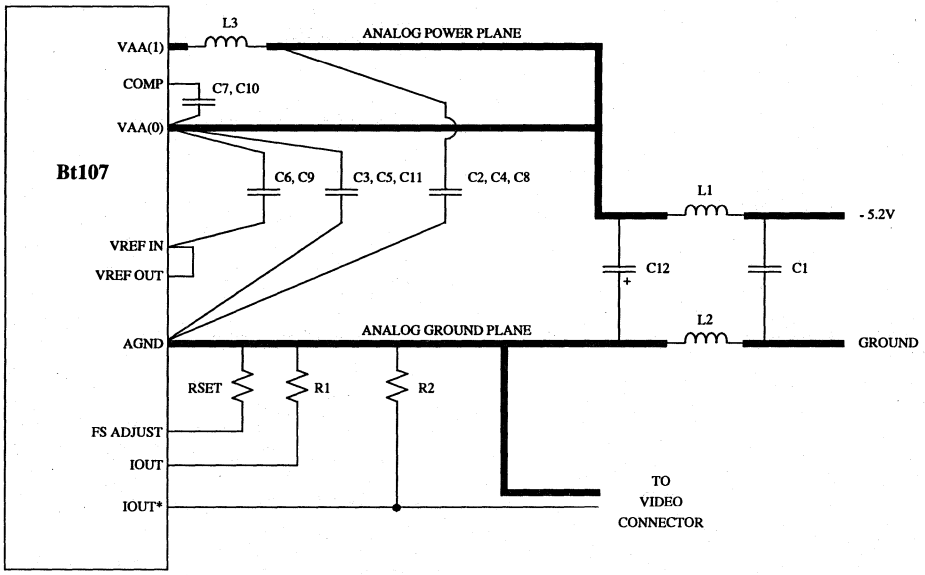
Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane rather than the analog power plane, to maximize the high-frequency power supply rejection.

The analog transmission lines must have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8–C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1	24.9 Ω 1% metal film resistor	Dale CMF-55C
R2	49.9 Ω 1% metal film resistor	Dale CMF-55C
RSET	732 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt107. R1, R2, and RSET values assume doubly-terminated 50 Ω load on IOUT*.

Figure 3. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

Terminated Inputs

All digital inputs of the Bt107 should be terminated with normal ECL termination practices. In addition, all of the digital inputs have internal pull-down junctions. Thus, if a digital input is left floating, it assumes the logical-zero state.

External Voltage Reference

An external voltage reference may be used with the Bt107, as shown in Figure 4. In this instance, the VREF OUT pin should be left floating.

The VREF IN pin still requires bypass capacitors to VAA(0) (C6 and C9 in Figure 3).

Package Heatsink

The stud heatsink is electrically isolated and should be connected to AGND for minimal noise.

Using Multiple Bt107s

For color applications, three Bt107s may be used, as illustrated in Figure 5. This example generates 256 simultaneous colors from a 16.8-million color palette and supports a 2k x 2k pixel resolution.

Both the even and odd pixel data require separate shift registers and color palette RAM. (Bt403s are used in Figure 5.) The Bt502s interface the color palette RAM to the TTL-compatible MPU bus. If more than 256 colors are desired, additional Bt403s may be wired in parallel to expand each color palette RAM to 1024 x 8.

The DIV2OUT*–DIV2IN connections generate CLOCK*/2 and ensure the three Bt107s operate in a synchronous fashion. When the timing window for DIV2IN is being analyzed, the propagation delay of the CLOCK and DIV2OUT* signals through the transmission lines of the physical layout on the PC board should be included.

When DIV2OUT is to be used for system CLOCK, it is recommended that DIV2OUT* be buffered before distribution to the rest of the system to allow for adequate noise margins.

The Bt107s may share the voltage reference and analog power/ground planes, but each Bt107 must have its own power supply decoupling, COMP decoupling, VREF IN decoupling, VAA(1) ferrite bead, RSET resistor, and IOUT termination resistors.

Optimum layout should minimize CLOCK and DIV2* line length. Low E stripline is recommended, and the propagation delays between CLOCK and DIV2* should match as closely as possible.

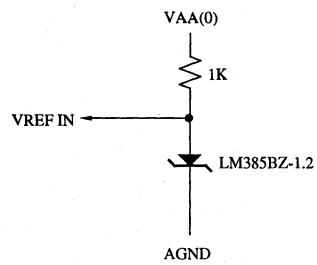


Figure 4. External Voltage Reference.

Application Information *(continued)*

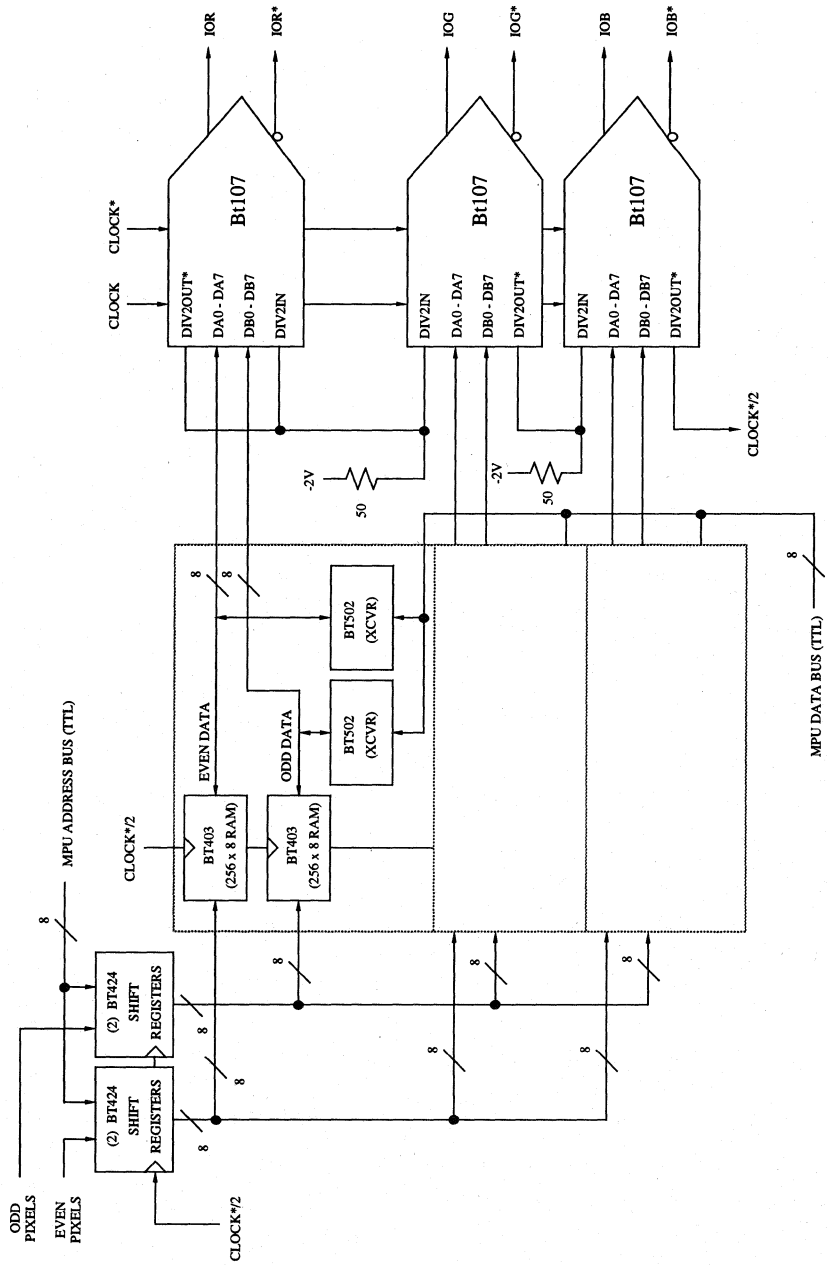


Figure 5. Using Multiple Bt107s.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	–4.2	–5.2	–5.5	V
Ambient Operating Temperature	TA	–25		+85	°C
Output Load	RL		25		Ω
Reference Voltage	VREF IN	–1.13	–1.2	–1.3	V
FS ADJUST Resistor	RSET		729		Ω

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)	VAA			–6.5	V
Voltage on Any Digital Pin		AGND + 0.5		VAA –0.5	V
Analog Output Short Circuit Duration to Any Common			indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1/2	
Differential Linearity Error	DL			±1/2	
Gray Scale Error					LSB
Using Internal Reference				±10	
Using External Reference				±5	LSB
Monotonicity			guaranteed		
Coding					
Digital Inputs					% Gray Scale
Input High Voltage	VIH	–1160		–710	
Input Low Voltage	VIL	–1870		–1480	% Gray Scale
Input High Current	IIH				
(Vin = VIHmax)					
Data				30	
All Other Inputs				150	Binary
Input Low Current	IIL				
(Vin = VILmin)					
Blank				150	
All Other Inputs				5	
Input Capacitance	CIN			10	
(f = 1 MHz, Vin = VIHmax)					mV
Digital Output					mV
Output High Voltage	VOH	–1060	–955	–880	
Output Low Voltage	VOL	–1870	–1705	–1620	
Analog Output					
Gray Scale Current Range				–40	
Output Current (IOUT*)					µA
White Level		0	–5	–50	
Black Level Relative to White		–25.08	–26.40	–27.72	µA
Blank Level Relative to Black					
SETUP = AGND		0	0	0	
SETUP = float		–2.05	–2.16	–2.28	
LSB Size			–103.5		
Output Compliance	VOC	–1.2		+1.5	
Output Impedance	ROUT		10		µA
Output Capacitance	COUT		9		
(f = 1 MHz, IOUT = 0 mA)					µA
Reference Input Current	IREF IN			10	pF
Reference Output Voltage	VREF OUT	–1.14	–1.22	–1.3	
Reference Output Current	IREF OUT	–200			
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 kHz)	PSRR		0.03	0.5	

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full-scale output current, VREF IN = –1.21 V, and SETUP = float. All digital inputs have 50 Ω to –2.0 V. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

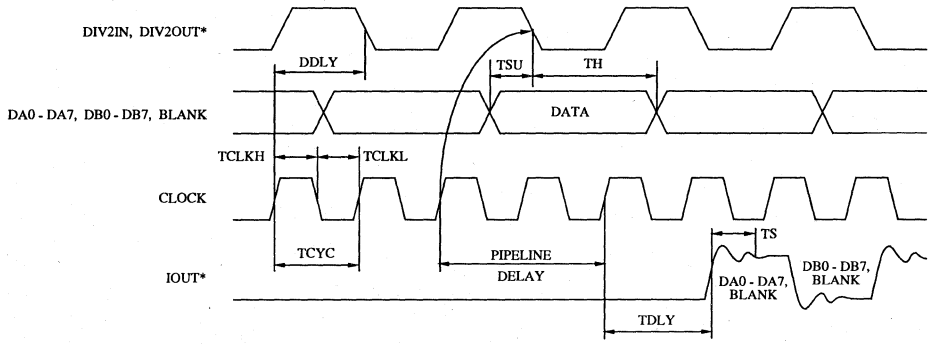
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			400	MHz
Data and Control Setup Time Data and Control Hold Time	TSU TH	1 0			ns ns
Clock Cycle Time Clock Pulse Width High Clock Pulse Width Low	TCYC TCLKH TCLKL	2.5 1 1			ns ns ns
DIV2OUT Delay (Note 1) DIV2IN Setup Time DIV2IN Hold Time	DDLY DSU DH	1.5 0 1		2.2	ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time (Note 2) Clock and Data Feedthrough Glitch Impulse (Note 3) Nonharmonic Spurious	TDLY TVRF TS		 350 tbd 10 –45	2 700 2	ns ps ns dB LSB - ns dBc
Pipeline Delay (Pixel A –EVEN)		2	2	2	Clocks
VAA Supply Current	IAA			225	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full-scale output current, VREF IN = –1.21 V, and SETUP = float. ECL input values are –0.95 to –1.69 V with input rise/fall times ≤ 1 ns, measured between the 20-percent and 80-percent points. Timing reference points are at 50 percent for inputs and outputs. All digital inputs have 50 Ω to –2.0 V, unless otherwise specified. Analog output load ≤ 10 pF. See timing notes in Figure 6. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Tested with one ECL load.
Note 2: Settling time does not include clock and data feedthrough.
Note 3: Glitch impulse includes clock and data feedthrough, at –3 dB test bandwidth = 800 MHz.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1/2 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 6. Input/Output Timing (DIV2IN connected to DIV2OUT*).

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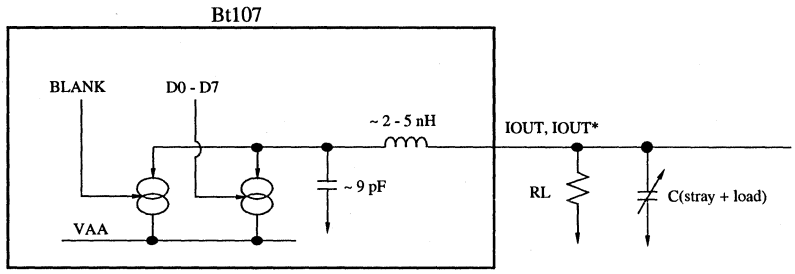
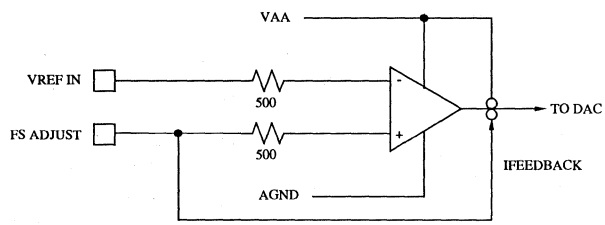
Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt107BF400	400 MHz	32-pin Ceramic Flatpack w/heatsink	–25° to +85° C



The output network of the Bt107 may be modeled as a three-pole low-pass filter. Settling time is tested on a sample basis with C(stray + load) tuned for optimum performance.

Equivalent Output Circuit of the Bt107.



Equivalent Circuit of the Reference Amplifier.

Bt109

250 MHz 10KH ECL Triple 8-bit VIDEODAC™

Distinguishing Features

- 250 MHz Pipelined Operation
- Triple 8-bit D/A Converters
- ±1/2 LSB Differential Linearity Error
- ±1/2 LSB Integral Linearity Error
- 350 ps Typical Rise/Fall Time
- RS-343A-Compatible Outputs
- 10KH ECL-Compatible Inputs
- 40-pin DIP Package
- Pin Compatible with TDC1318
- Typical Power Dissipation: 2 W

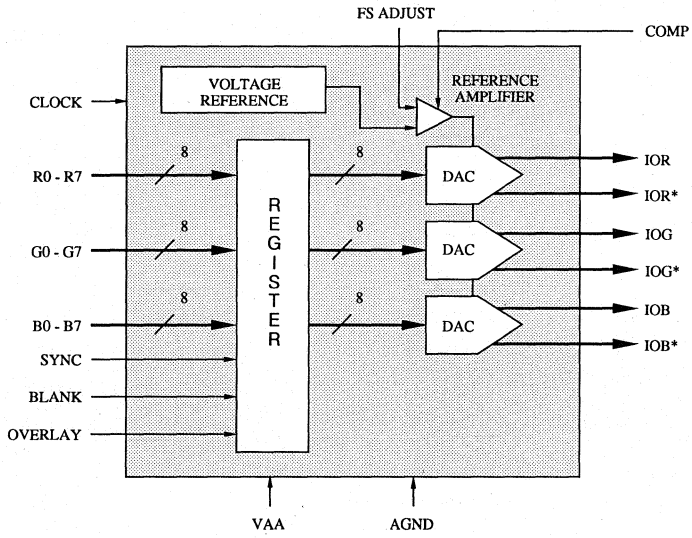
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt107
- Bt401/403
- Bt424
- Bt492

Functional Block Diagram



Product Description

The Bt109 is a triple 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and overlay, all registered to maintain synchronization with the pixel data.

An internal 1.2 V voltage reference and a single external resistor control the full-scale output current.

The Bt109 generates RS-343A-compatible red, green, and blue video signals and can drive doubly-terminated 75 Ω coax directly without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/2 LSB over the full temperature range.

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L109001 Rev. H

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt109 contains three 8-bit D/A converters, input registers, a voltage reference, and a reference amplifier.

On the rising edge of each clock cycle, as shown in Figure 1, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters.

The OVERLAY input, also latched on the rising edge of CLOCK, forces the analog outputs to the overlay level, regardless of the data inputs. This also permits blanking of the IOUT* outputs for analog summing.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC and BLANK inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC, BLANK, and OVERLAY inputs modify the output levels.

The full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 1100 Ω for generation of RS-343A video into a 37.5 Ω load.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOR, IOG, and IOB outputs through 37.5 Ω resistors to AGND (assuming IOR*, IOG*, and IOB* are driving a doubly-terminated 75 Ω load). The IOR*, IOG*, and IOB* outputs are then used to generate the video signals.

The D/A converters on the Bt109 use a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt109 can directly drive a doubly-terminated 75 Ω coaxial cable or a singly-terminated 50 Ω coaxial cable.

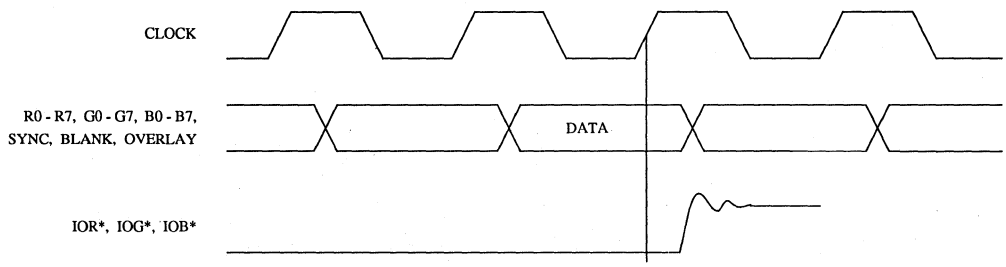
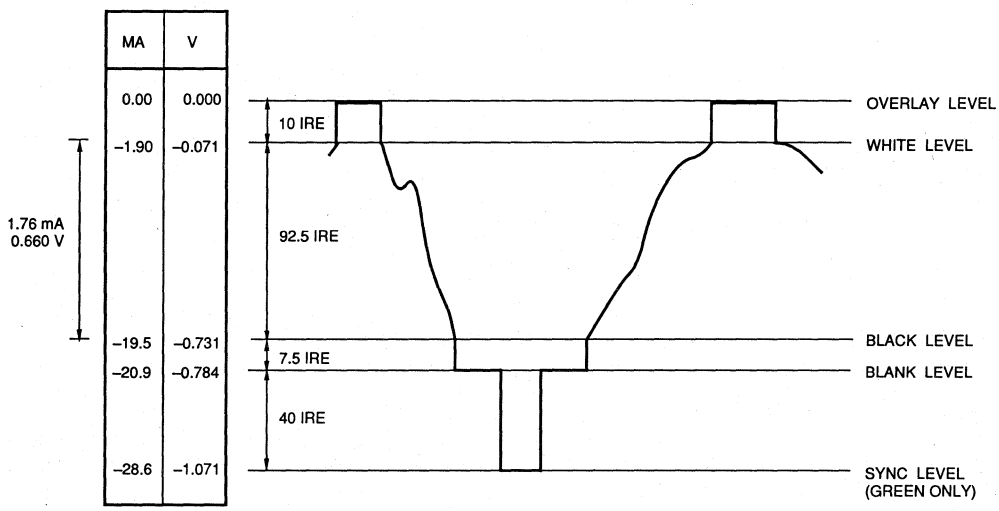


Figure 1. Input/Output Timing.

Circuit Description *(continued)*



Note: 75 Ω doubly-terminated load and RSET = 1100 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 2. Composite Video Output Waveforms (IOUT*).

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Description	IOG* (mA)	IOR*, IOB* (mA)	OVERLAY	SYNC	BLANK	DAC Input Data
OVERLAY	0	0	1	0	0	$xx
WHITE	–1.90	–1.90	0	0	0	$FF
DATA	data–1.90	data–1.90	0	0	0	data
BLACK	–19.50	–19.50	0	0	0	$00
BLANK	–20.90	–20.90	x	0	1	$xx
SYNC	–28.60	–20.90	x	1	1	$xx

Note: Typical values, RSET = 1100 Ω. SYNC does not override data, as with the TDC1318.

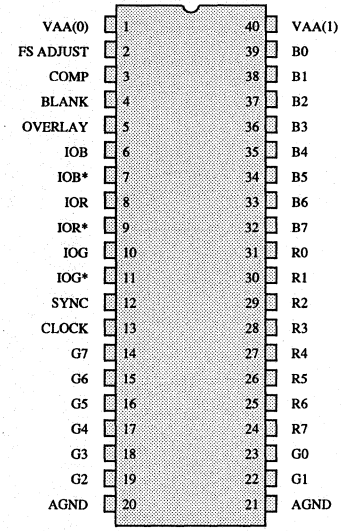
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logical one on this input drives the analog outputs to the blanking level, as specified in Table 1. It is latched on the rising edge of CLOCK. When BLANK is a logical one, the data and OVERLAY inputs are ignored.
SYNC	Composite sync control input (ECL compatible). A logical one on this input switches on a 40 IRE current source on the green output (see Figure 2). SYNC does not override any other control or data input, as specified in Table 1; therefore, SYNC should be asserted only during the blanking interval. SYNC is latched on the rising edge of CLOCK.
OVERLAY	Overlay control input (ECL compatible). A logical one on this input overrides the data inputs and forces the analog outputs to the overlay level. OVERLAY is latched on the rising edge of CLOCK.
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (ECL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (ECL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC, BLANK, and OVERLAY inputs. It is typically the pixel clock rate of the video system.
IOR, IOG, IOB, IOR*, IOG*, IOB*	Red, green, and blue differential video current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figure 3 in the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected. *Warning: A ferrite bead must be used to connect the VAA(1) power pin to the analog power plane, as illustrated in Figure 3. Connecting the decoupling capacitors directly to the VAA(1) pin will result in unstable operation.*
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 ceramic chip capacitor must be connected between this pin and VAA(0) (Figure 3). Connecting the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions *(continued)*

Pin Name	Description
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 3). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current (SYNC level) on IOG* is: RSET (Ω) = 31,460 / IOG (mA) The full-scale output current (BLANK level) on IOR* and IOB* for a given RSET is defined as: IOR, IOB (mA) = 22,990 / RSET (Ω) Note: The RSET value may require adjustment to generate the specified video levels because of variations in processing.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt109 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The Bt109 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt109.

The analog ground plane area should encompass all Bt109 ground pins, power supply bypass circuitry for the Bt109, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading to the Bt109.

Power Planes

The Bt109 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt109.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt109 power pins and any output amplifiers.

Portions of the regular PCB power and ground planes must not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the VAA(1) power pin and the analog power plane, as illustrated in Figure 3. The ferrite bead must be located as close as possible to the VAA(1) pin.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the VAA(1) pin, as illustrated in Figure 3. Connecting the bypass capacitors directly to the VAA(1) pin will result in unstable operation caused by high-frequency oscillations.

If a switching power supply is used, the designer should reduce power supply noise and consider using a three-terminal voltage regulator to supply power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt109 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

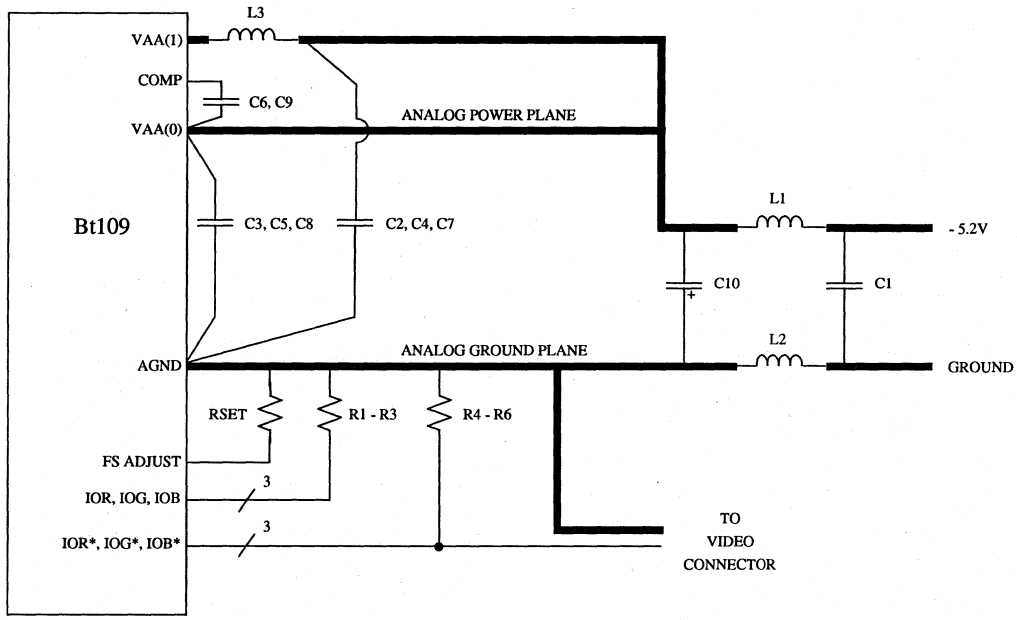
Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, rather than the analog power plane, to maximize the high-frequency power supply rejection.

The analog transmission lines must have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C6	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C7–C9	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C10	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	37.4 Ω 1% metal film resistor	Dale CMF-55C
R4, R5, R6	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1100 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt109.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Terminated Inputs

All digital inputs of the Bt109 should be terminated with normal ECL termination practices. In addition, all of the digital inputs have internal pull-down junctions. Thus, if a digital input is left floating, it assumes the logical zero state.

Nonvideo Applications

The Bt109 may be used in nonvideo applications by disabling the video-specific control inputs. The SYNC, BLANK, and OVERLAY inputs should be logical zeros. All three outputs will have the same full-scale output current.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 19{,}360 / Iout\ (mA)$$

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 2{,}090 / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	–4.9	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		37.5		Ω
FS ADJUST Resistor (Note 1)	RSET		1100		Ω

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Note 1: FS ADJUST is set to 1.125 mA.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)	VAA			–6.5	V
Voltage on Any Digital Pin		AGND + 0.5		VAA–0.5	V
Analog Output Short Circuit Duration to Any Common			indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	–1170 –1130 –1070		–840 –810 –735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	–1950 –1950 –1950		–1480 –1480 –1450	mV mV mV
Input High Current (Clock, Data, Sync) (Vin = VIHmax)	IIH	0 +25 +70			25 25 25	µA µA µA
Input High Current (Overlay) (Vin = VIHmax, VILmin)	IIH	0 +25 +70			210 210 210	µA µA µA
Input High/Low Current (Blank) (Vin = VIHmax, VILmin)	IIH / IIL	0 +25 +70			160 160 160	µA µA µA
Input Low Current (Clock, Data, Sync, Overlay) (Vin = VILmin)	IIL	0 25 +70			5 5 5	µA µA µA
Input Capacitance (f = 1 MHz, Vin = VIHmax) BLANK All Others	CIN				 20 7	 pF pF
Internal Voltage Reference	VREF			–1.2		V

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/2	LSB
Gray-Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Analog Outputs					
Gray Scale Current Range:					
Black Level Relative to White				–20	mA
Blank Level Relative to White				–30	mA
Output Current (IOUT*)					
Overlay Level		0	–5	–50	µA
White Level		–1.70	–1.90	–2.10	mA
Black Level Relative to White		–15.86	–17.62	–19.38	mA
Blank Level Relative to Black		–0.95	–1.44	–1.90	mA
Blank Level Relative to White		–16.81	–19.05	–21.28	mA
Sync Level Relative to Blank		–6.29	–7.62	–8.96	mA
LSB Size			–69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–1.2		+1.5	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –17.62 mA full-scale output current (gray scale, black-white). Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

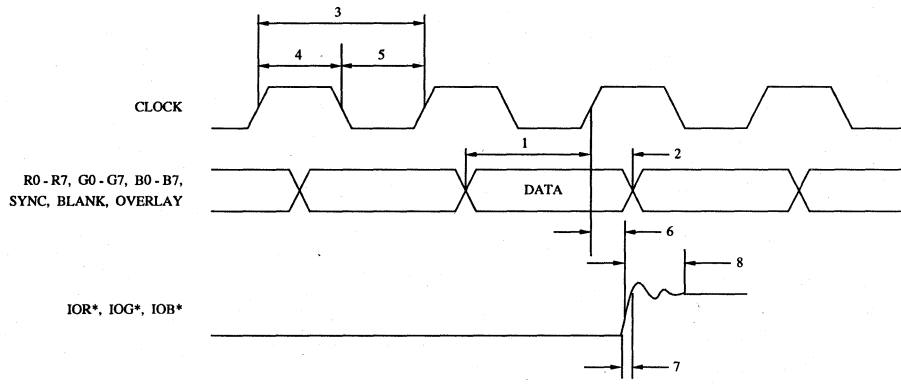
The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate				250	MHz
Data and Control Setup Time Data and Control Hold Time	1 2	1.5 0			ns ns
Clock Cycle Time Clock Pulse Width High Clock Pulse Width Low	3 4 5	4 1.6 1.6			ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time Glitch Impulse	6 7 8		 0.5 4 50	3 1	ns ns ns pV - sec
VAA Supply Current	IAA			400	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –17.62 mA full-scale output current (gray scale). ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1/2 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 4. Input/Output Timing.

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Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt109KC	250 MHz	40-pin 0.6" Ceramic Cavity Down DIP	0° to +70° C

Bt121

80 MHz Monolithic CMOS Triple 8-bit VIDEODAC™

Distinguishing Features

- 80, 50 MHz Operation
- Triple 8-bit D/A Converters
- Optional Internal Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt473

Product Description

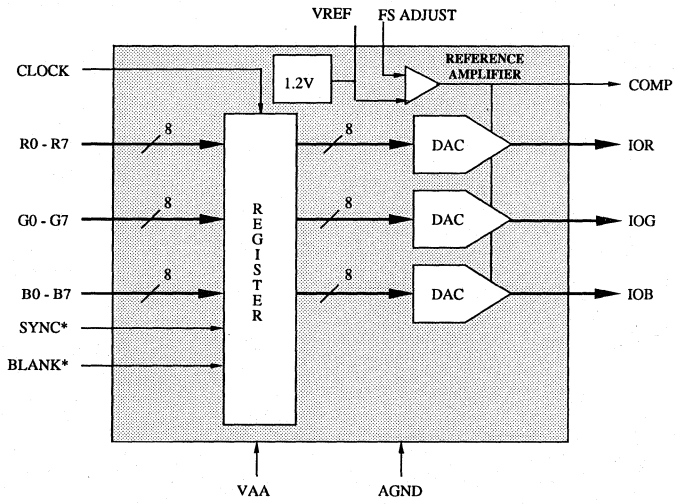
The Bt121 is a triple 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

This device offers a higher level of integration than previous VIDEODAC designs. Included is an on-chip voltage reference to simplify use of the device.

The Bt121 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load, and RS-170-compatible video signals into a singly- terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

6

Functional Block Diagram



Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
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L121001 Rev. F

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt121 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of CLOCK, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 1. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt121 use a segmented architecture in which bit currents are routed to either the output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt121 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

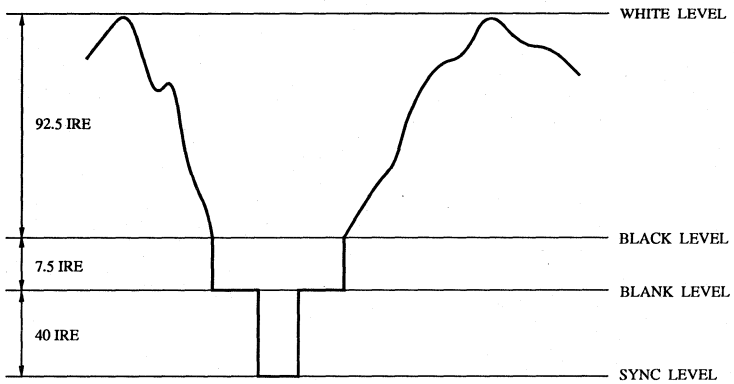
Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET ~ 143 Ω, and VREF = 1.23 V. RS-343A levels and tolerances are assumed on all levels.

6

Figure 1. Composite Video Output Waveforms.

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly-terminated load, SETUP = 7.5 IRE. VREF = 1.23 V and RSET ~ 143 Ω.

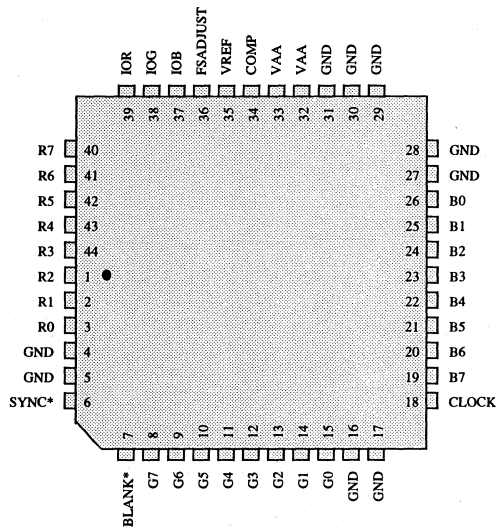
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as detailed in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R7, G0–G7, and B0–B7 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOR, IOG, IOB outputs (see Figure 1). SYNC* does not override any other control or data input, as shown in Table 1; therefore, SYNC* should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least-significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figures 2 and 3 in the PC Board Lay-out Considerations section). All outputs, whether used or not, should have the same output load.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 1). The IRE relationships in Figure 1 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOR, IOG and IOB is: RSET (Ω) = K * VREF (V) / IO (mA) Where; K = 2,295 with SYNC*=0 K = 3,195 with SYNC*=1

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor in series with a resistor should be connected between this pin and the nearest VAA pin (Figures 2 and 3) for optimum settling time. Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
VREF	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. A 0.1 µF ceramic capacitor must always be used to decouple this input to GND, as shown in Figures 2 and 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor (Figure 2).
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt121 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated VIDEODAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt121 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt121 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 2 and 3. This bead should be located within 3 inches of the Bt121. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the VAA pins to GND. For operations above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01µF chip capacitor is reccommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 2 and 3 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

To optimize the settling time of the Bt121, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time. An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

The COMP pin and series resistor must also be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

To reduce low-frequency supply noise a larger COMP capacitor value may be required.

PC Board Layout Considerations *(continued)*

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt121 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt121 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the VIDEODAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Analog Signal Interconnect

The Bt121 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt121 to minimize reflections. Unused analog outputs should be connected to GND.

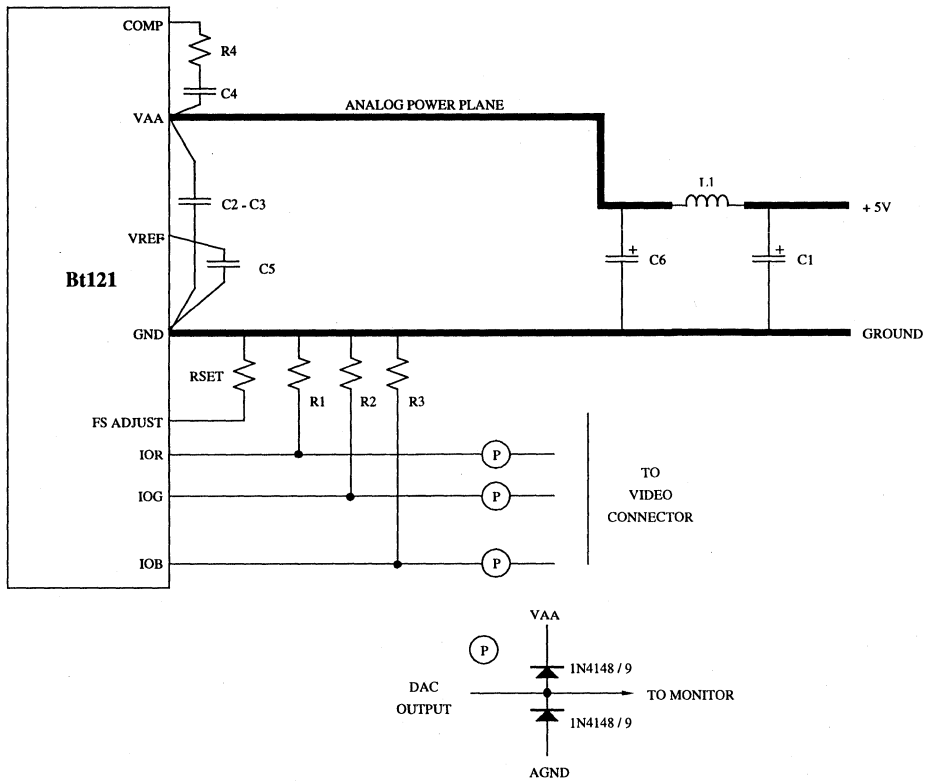
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt121 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 2 and 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



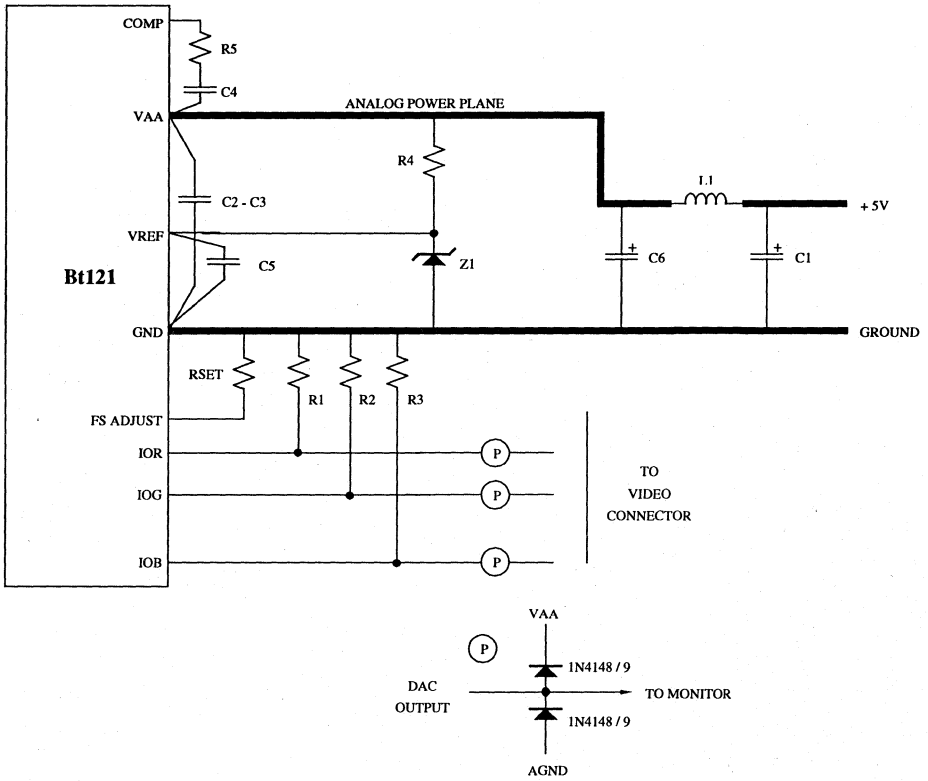
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C4, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	143 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt121.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C4, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 5% metal film resistor	
R5	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	143 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt121.

Figure 3. Typical Connection Diagram and Parts List (External Reference).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
External Reference Voltage	VREF	1.11	1.235	1.36	V
FS ADJUST Resistor	RSET		143		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND– 0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the absolute maximum ratings (especially relative to VAA or between VAA pins) can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
External Reference				±5	% Gray Scale
Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 400 µA)	VOL			0.4	V
Output Capacitance	CDOUT			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Sync Level on IOR, IOG, IOB		6.29	7.62	7.94	mA
LSB Size			69.72		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Internal VREF Voltage Range	INTVREF	1.08	1.2	1.32	V
Internal VREF Output Current	IVREF			10	µA
Power Supply Rejection Ratio (Note 1) (COMP = 0.01 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is being used, RSET may require adjustment to meet these limits.

Note 1: Guaranteed by characterization, not tested.

AC Characteristics

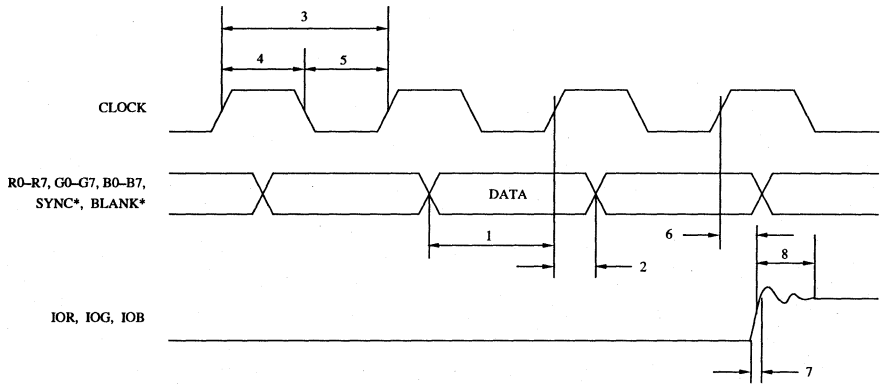
		80 MHz Devices			50 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			80			50	MHz
Data and Control Setup Time	1	3			3			ns
Data and Control Hold Time	2	3			3			ns
Clock Cycle Time	3	12.5			20			ns
Clock Pulse Width High Time	4	4			7			ns
Clock Pulse Width Low Time	5	4			7			ns
Analog Output Delay	6			30			30	ns
Analog Output Rise/Fall Time	7		3			3		ns
Analog Output Settling Time	8		12.5			15.5		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	3		0	3	ns
Pipeline Delay		2	2	2	2	2	2	Clock
VAA Supply Current (Note 2)	IAA		95	110		95	110	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 143 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and SENSE* output load ≤ 50 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 4. Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt121KPJ80	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt121KPJ50	50 MHz	44-pin Plastic J-Lead	0° to +70° C

Section 7

PERIPHERALS

Brooktree®

Contents

Bt110

100 ns Monolithic CMOS Octal 8-bit D/A Converter

Distinguishing Features

- Eight 8-bit D/A Converters
- 100 ns Settling Time to ±1 LSB
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- Guaranteed Monotonic
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 150 mW

Applications

- Instrumentation
- Test Equipment
- Waveform Synthesis
- Data Acquisition Systems

Product Description

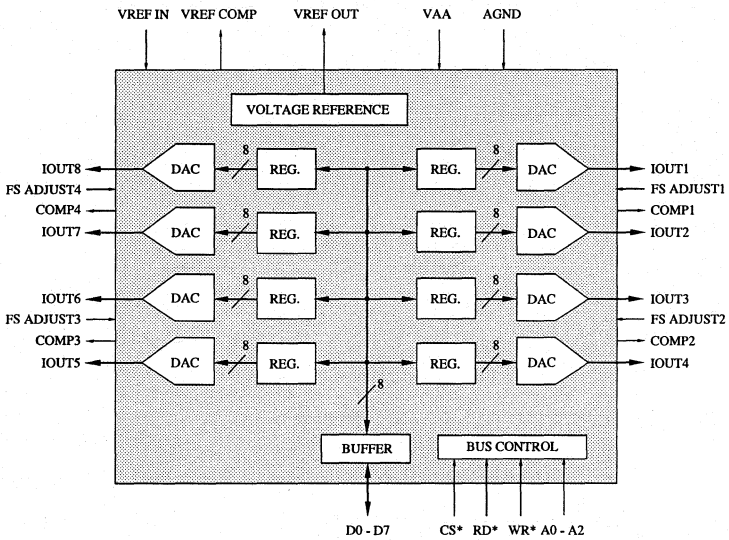
The Bt110 is an octal 8-bit D/A converter. It provides eight independent D/A converters and has a standard MPU interface.

The D/A converters are arranged in pairs with each pair sharing a common reference amplifier. This provides excellent matching and stability of the paired D/A converters.

An on-chip voltage reference is provided, or an external reference may be used. Differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

7

Functional Block Diagram



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L110001 Rev. I

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt110 contains eight 8-bit D/A converters, eight nontransparent (D-type) octal data registers, and MPU bus interface logic. Also included on chip are four reference amplifiers and a voltage reference.

The Bt110 supports a conventional MPU bus interface through the use of the CS*, RD*, WR*, D0–D7, and A0–A2 pins. A0–A2 specify which one of the eight internal data latches the MPU is accessing. These data latches may be written to or read by the MPU at any time. The input/output timing is illustrated in Figure 1.

The data contained in the data latches is presented to the associated D/A converter and used to specify the output current level. The MPU may read these data latches to determine what data is present at each D/A converter.

The full-scale output current of each pair of D/A converters is set by an external resistor (RSET) between the FS ADJUST pin and AGND. FS ADJUST1 controls the full-scale output current of IOUT1 and IOUT2, FS ADJUST2 controls the full-scale output current of IOUT3 and IOUT4, FS ADJUST3 controls the full-scale output current of IOUT5 and IOUT6, and FS ADJUST4 controls the full-scale output current of IOUT7 and IOUT8.

The on-chip voltage reference (VREF OUT) may be used to provide the reference voltage for the VREF IN pin, or an external reference circuit may be used. The on-chip reference should offer adequate performance for most applications.

Better temperature stability can be attained if an external voltage reference, such as the LM385BZ-1.2, is used. The use of a resistor network to generate the reference voltage is not recommended, as any low-frequency power supply noise on VREF IN will be directly coupled onto the analog outputs.

The D/A converters on the Bt110 use a segmented architecture in which bit currents are routed to either IOUT or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. The on-chip operational amplifiers stabilize the full-scale output currents against temperature and power supply variations.

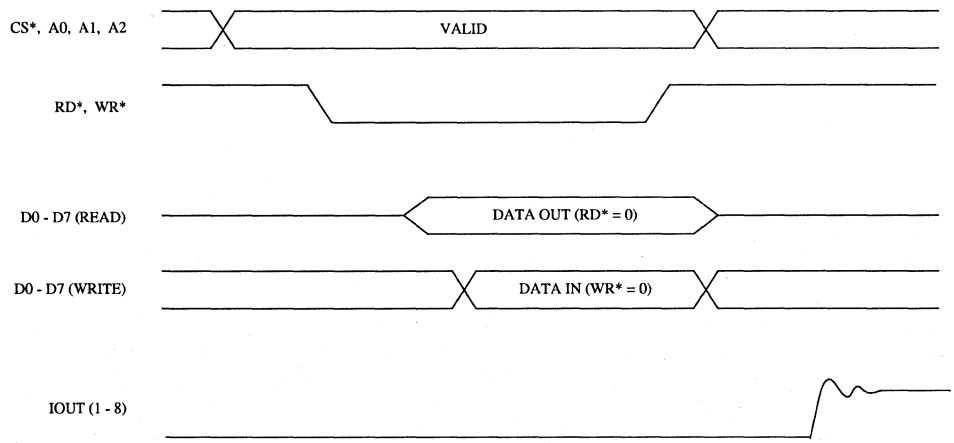


Figure 1. Input/Output Timing.

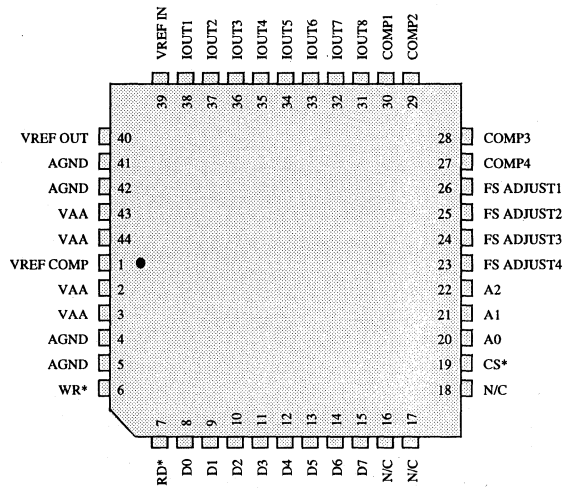
Pin Descriptions

Pin Name	Description
FS ADJUST (1–4)	Full-scale adjust controls. A resistor (RSET) between each of these pins and AGND controls the full-scale output currents. FS ADJUST1 controls the full-scale output current for IOUT1 and IOUT2, FS ADJUST2 controls the full-scale output current for IOUT3 and IOUT4, FS ADJUST3 controls the full-scale output current for IOUT5 and IOUT6, and FS ADJUST4 controls the full-scale output current for IOUT7 and IOUT8. The relationship between the full-scale output current of each D/A and RSET is defined as follows: RSET (Ω) = 1000 * VREF IN (V) / IOUT (mA)
COMP (1–4)	Compensation pins. These pins provide compensation for the internal reference amplifiers. A 0.1 µF ceramic capacitor should be connected between each compensation pin and VAA, as illustrated in Figure 2 (in the PC Board Layout Considerations section). Decoupling the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. COMP1 provides compensation for IOUT1 and IOUT2, COMP2 provides compensation for IOUT3 and IOUT4, COMP3 provides compensation for IOUT5 and IOUT6, and COMP4 provides compensation for IOUT7 and IOUT8. Refer to the PC Board Layout Considerations section for critical layout criteria.
IOUT (1–8)	High-impedance current outputs. These current outputs are designed to drive into a virtual ground, such as an operational amplifier.
VREF OUT	Voltage reference output. This output provides a 1.2 V (typical) reference and may be directly connected to the VREF IN pin. When VREF OUT is used to provide a reference voltage to VREF IN, an external 1000 Ω resistor must be connected between VREF OUT and AGND.
VREF IN	Voltage reference input. Either an external voltage reference circuit or the VREF OUT pin is used to supply this input with a 1.2 V (typical) reference. A 0.1 µF ceramic capacitor must be connected between this pin and VREF COMP.
VREF COMP	VREF IN compensation pin. A 0.1 µF ceramic capacitor must be connected between this pin and VREF IN. Refer to the PC Board Layout Considerations section for critical layout criteria.
AGND	Analog ground. All AGND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
CS*	Chip select control input (TTL compatible). To enable data to be written to or read from the device, this input must be a logical zero. While it is a logical one, D0–D7 are three-stated. The Bt110 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
RD*	Read control input (TTL compatible). To enable data to be read from the device, both CS* and RD* must be a logical zero (see Figure 1).

Pin Descriptions *(continued)*

Pin Name	Description
A0, A1, A2	Select control inputs (TTL compatible). These inputs specify which internal D/A latch will be written to or read, as follows:
WR*	Write control input (TTL compatible). To enable data to be written to the device, both CS* and WR* must be a logical zero. Data is internally latched on the rising edge of WR* or CS*, whichever occurs first (see Figure 1).
D0–D7	Bidirectional data bus (TTL compatible). Data is transferred into and out of the Bt110 over this 8-bit data bus. D0 is the least significant bit.

A2, A1, A0	D/A Output
000	IOUT1
001	IOUT2
010	IOUT3
011	IOUT4
100	IOUT5
101	IOUT6
110	IOUT7
111	IOUT8



Note: N/C pins may be left floating without affecting the performance of the Bt110.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt110 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated device pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt110 to be located as close as possible to the power supply connector and the IOUT connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt110 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt110. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above 100 MHz.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 22 µF capacitor shown in Figure 2 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pins must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. The COMP capacitors must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

To reduce low-frequency supply noise a larger COMP capacitor value may be required.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt110 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

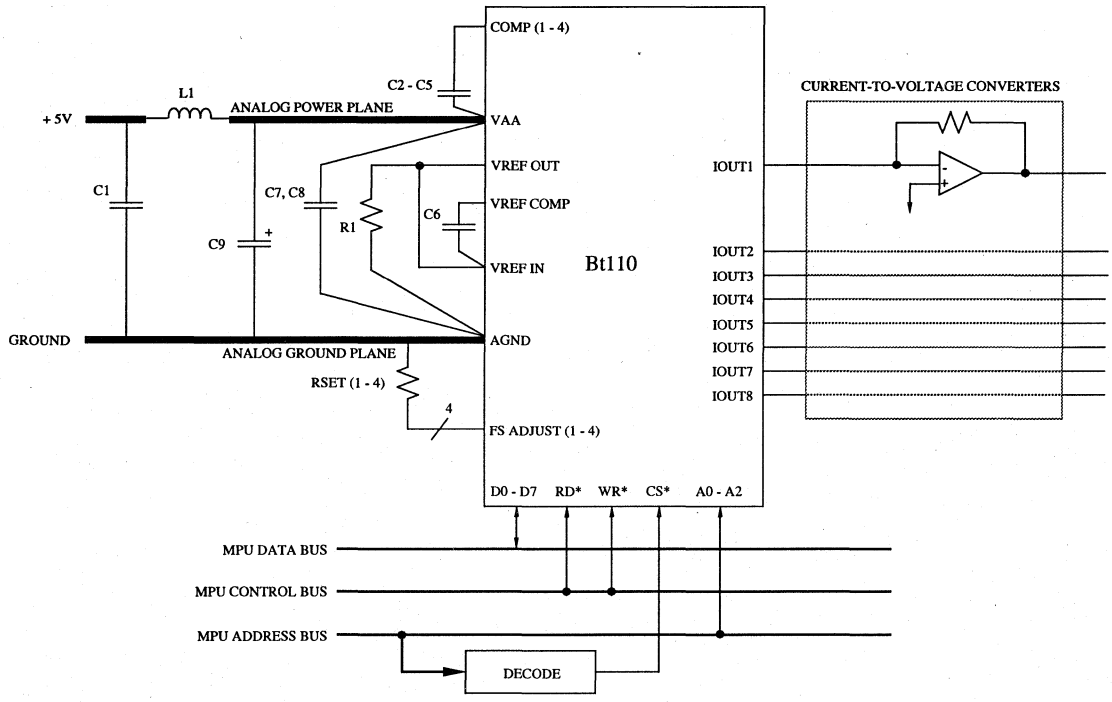
Analog Signal Interconnect

The Bt110 should be located as close as possible to the IOUT terminations to minimize noise pickup.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the output signals should not overlay the analog power plane.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1–C8	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C9	22 µF tantalum capacitor	Mallory CSR13G226KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET (1–4)	1% metal film resistors	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt110.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

External Voltage Reference

For improved temperature stability, an external voltage reference may be used with the Bt110, as shown in Figure 3. In this instance, the VREF OUT pin should remain floating. The temperature stability of the internal reference is equivalent to about 1/4 LSB.

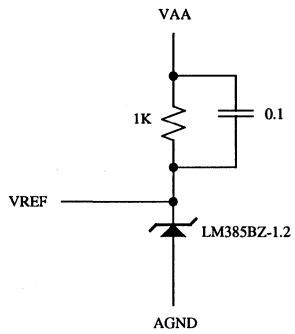


Figure 3. External Voltage Reference.

Programmable Window Comparator

The window comparator of Figure 4 is a circuit that can be used to determine whether the input voltage (Vin) lies within predefined limits. When the Bt110 is used, up to four programmable window comparators may be implemented.

One DAC of the matched pair is used to set the low limit, and the other DAC is used to set the high limit. Thus, each pair of DACs forms a window of programmable size. The output will be high while Vlow ≤ Vin ≤ Vhigh.

For a RSET value of 1200 Ω and a VREF IN of 1.2 V, the Bt110 outputs a full-scale output current of approximately 1 mA onto IOUT1 and IOUT2. The 1 kΩ resistor generates a 0–1 V output (for DAC codes $00 to $FF), which is amplified to 0–5 V (5x) by the LM358 dual operational amplifier. In this configuration, the LM358 is operating from a single +5 V power supply.

The LM319 dual comparator is also operating from a single +5 V power supply and compares the Vlow and Vhigh voltage levels to Vin. The 500 Ω pullup resistor is necessary, as the LM319 has open-collector outputs.

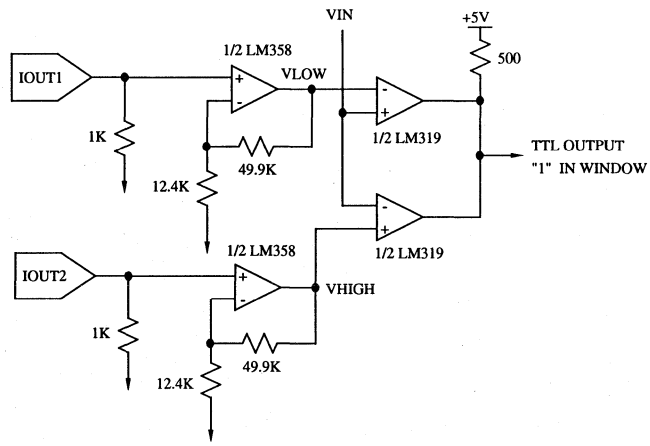


Figure 4. Programmable Window Comparator.

Application Information *(continued)*

Programmable Power Supply

The Bt110, when used with an external operational amplifier and power transistor, generates voltages and currents outside its normal capability. Figure 5 illustrates a 0–10 V programmable power supply.

For an RSET value of 1200 Ω and a VREF IN of 1.2 V, the Bt110 outputs a full-scale output current of approximately 1 mA onto IOUT1. The 1 kΩ resistor is used to generate a 0–1 V output from the Bt110 (for DAC codes $00 to $FF). One of the operational amplifiers in the LM358 (A1) is used to multiply the voltage at IOUT1 by 10x, resulting in a 0–10 V range. In this configuration, the LM358 is operating from a single +15 V power supply.

The other operational amplifier in the LM358 (A2) is used as a buffer and driver for the TIP31 transistor. RS is the current-limiting resistor to shut down the output in case of an overload. The correct value for RS is determined as follows:

$$RS = 0.7 / IOUTmax$$

For output voltages down to or near 0 V, it is necessary to use a CMOS operational amplifier with a very low saturation voltage, or a plus/minus power supply and a bipolar operational amplifier to allow for output saturation, which is typically 2–3 V below the supply voltage.

Driving Active Devices

If the Bt110 is driving an active device whose supply is outside the 0–5 V range, the analog output(s) should be clamped to VAA (see Figure 5).

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

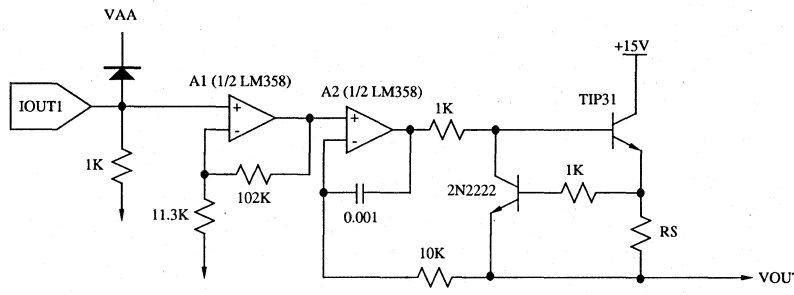


Figure 5. Programmable Power Supply.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Reference Voltage	VREF IN	1.0	1.2	1.3	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	V
Voltage on any Signal Pin (Note 1)		AGND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Full-Scale (Gain) Error	EG				
Using Internal Reference				±10	% of FSR
Using External Reference				±5	% of FSR
Zero Error	EZ			5	µA
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	AGND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			1	µA
Output Capacitance	CDOUT		10		pF
Analog Outputs					
Output Current				1	mA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–1.5		+1.2	V
Output Impedance	RAOUT		125		kΩ
Output Capacitance (IOUT1–IOUT8 = 0 mA)	CAOUT		20		pF
Reference Output Voltage	VREF OUT	1.05	1.17	1.29	V
Reference Output Current	IREF OUT		1.2		mA
Reference Input Current	IREF IN			10	µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.3		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1000 Ω and VREF IN = 1.0 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

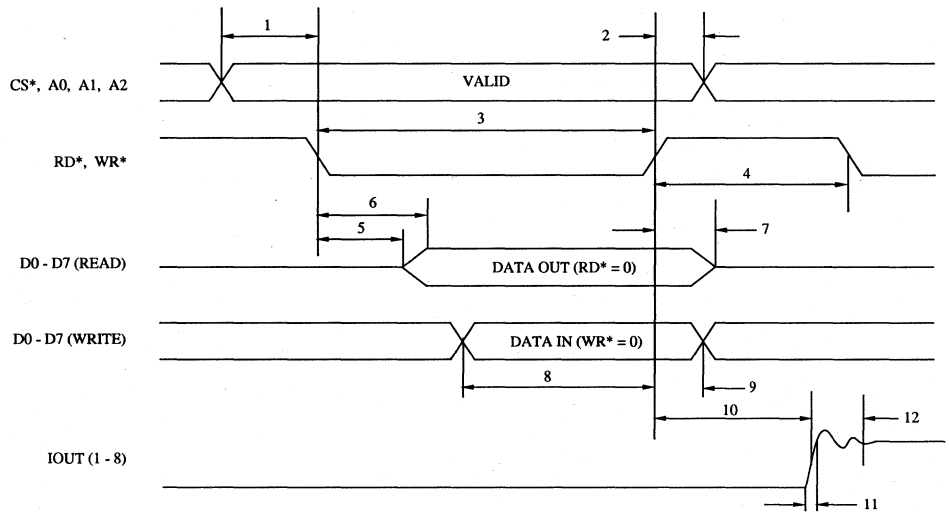
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Tmax			100	ns
CS*, A0, A1, A2 Setup Time	1	30			ns
CS*, A0, A1, A2 Hold Time	2	5			ns
WR* Low Time	3	30			ns
RD*, WR* High Time	4	20			ns
RD* Asserted to Data Bus Driven	5	10			ns
RD* Asserted to Data Valid	6			60	ns
RD* Negated to Data Bus 3-Stated	7			40	ns
Write Data Setup Time	8	20			ns
Write Data Hold Time	9	10			ns
Analog Outputs					
Analog Output Delay	10		15		ns
Analog Output Rise/Fall Time	11				
into 50 Ω				10	ns
into 1 kΩ			350		ns
Analog Output Settling Time	12				
into 50 Ω				100	ns
into 1 kΩ			800		ns
Data Feedthrough			–30		dB
Glitch Impulse			75		pV–sec
DAC-to-DAC Crosstalk			–25		dB
VAA Supply Current (Note 1)	IAA		30	38	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1000 Ω and VREF IN = 1.0 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF into a virtual ground, and D0–D7 output load ≤ 130 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms



Note 1: Output delay is measured from the rising edge of WR* to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 6. Input/Output Timing.

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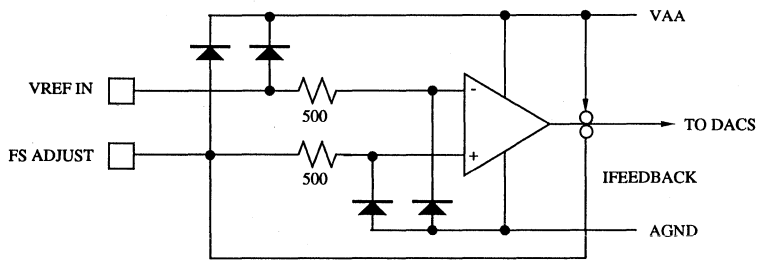
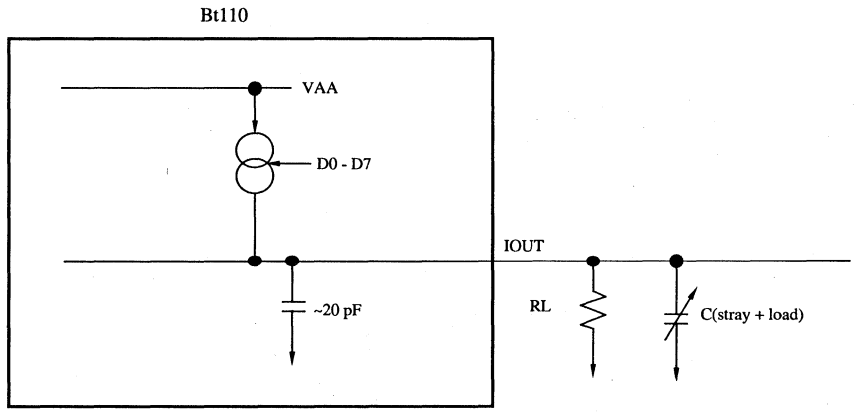
Ordering Information

Model Number	Package	Ambient Temperature Range
Bt110KPJ	44-pin Plastic J-Lead	0° to +70° C



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Outputs.

Bt401

Bt403

250 MHz
10KH ECL
256 x 8 Pipelined
Static RAM

Distinguishing Features

- 250 MHz Pipelined Operation
- Optional 3 x 8 Overlay Registers
- 10KH ECL Compatibility
- Synchronous or Asynchronous Reading
- Asynchronous Writing
- 28-pin, 0.6" or 24-pin, 0.3" DIP Package
- Typical Power Dissipation: 1100 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Microcode Storage

Related Products

- Bt424, Bt501, Bt502

Product Description

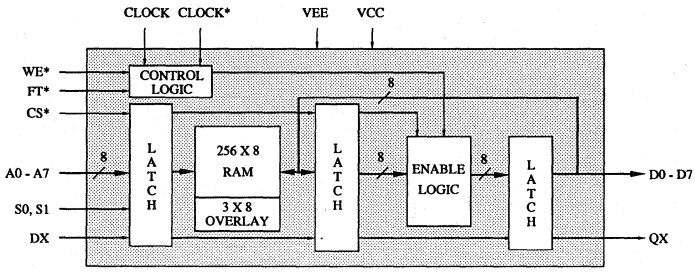
The Bt401 is a pipelined 256 x 8 RAM designed for high-speed graphics applications. In addition to the 256 colors supported by the RAM, three additional colors are available through the internal overlay registers, allowing, for example, cursor support and highlighting. Also incorporated is an input/output pipe to maintain synchronization of video control signals.

Both the Bt401 and Bt403 are 10KH ECL compatible.

The Bt403 does not have the three overlay registers and input/output pipe.

The devices may be read either synchronously or asynchronously and written to asynchronously. The asynchronous modes of operation simplify interface to an MPU.

Functional Block Diagram



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L401001 Rev. G

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt401 and Bt403 each contain a pipelined 256 x 8 RAM and control logic.

The Bt401 has three 8-bit overlay registers, that can be used, for example, to overlay menus and cursors onto the display screen, and as a pipe consisting of DX and QX to facilitate pipelining of control signals. Regardless of the value of FT*, the DX value is latched on the rising edge of CLOCK and output onto QX two clock cycles later.

The device operates in either a synchronous read, asynchronous read, or asynchronous write mode, as determined by the state of the FT* input. The synchronous read mode is typically used only for high-speed (250 MHz) read operations, while the asynchronous read and write modes are used to enable the MPU to read and write to the device at relatively slower data rates.

Table 1 summarizes the various modes of operation.

A0–A7	S0	S1	FT*	WE*	CS*	Operation	Mode
$00	0	0	1	x	0	read RAM location $00	synchronous
:	:	:	:	:	:	:	:
$FF	0	0	1	x	0	read RAM location $FF	synchronous
$xx	0	1	1	x	0	read overlay register 1	synchronous
$xx	1	0	1	x	0	read overlay register 2	synchronous
$xx	1	1	1	x	0	read overlay register 3	synchronous
$xx	x	x	1	x	1	D0–D7 = 0	synchronous
$xx	x	x	0	x	1	D0–D7 = 0	asynchronous
$00	0	0	0	1	0	read RAM location $00	asynchronous
:	:	:	:	:	:	:	:
$FF	0	0	0	1	0	read RAM location $FF	asynchronous
$xx	0	1	0	1	0	read overlay register 1	asynchronous
$xx	1	0	0	1	0	read overlay register 2	asynchronous
$xx	1	1	0	1	0	read overlay register 3	asynchronous
$00	0	0	0	0	0	write RAM location $00	asynchronous
:	:	:	:	:	:	:	:
$FF	0	0	0	0	0	write RAM location $FF	asynchronous
$xx	0	1	0	0	0	write overlay register 1	asynchronous
$xx	1	0	0	0	0	write overlay register 2	asynchronous
$xx	1	1	0	0	0	write overlay register 3	asynchronous

Table 1. Control Truth Table.

Circuit Description *(continued)*

Synchronous Read Operation

The A0–A7, S0, S1, and CS* inputs are latched on the rising edge of CLOCK. S0 and S1 are used to specify whether the RAM or one of the overlay registers is to provide data, as specified in Table 1. When accessing the RAM, the A0–A7 inputs are used to specify which one of the 256 locations is to provide the data. When accessing the overlay registers, the A0–A7 inputs are ignored.

During synchronous operation, the WE* input is ignored.

CS* must be a logical zero to enable the device to output data during synchronous operation. If CS* is a logical one, the D0–D7 pins are forced to a logical zero, and the A0–A7, S0, S1, and WE* inputs are ignored.

During synchronous read operation, the CS* may have the same timing as A0–A7 and is pipelined to maintain synchronization with these signals.

Figure 1 illustrates the read timing for synchronous operation.

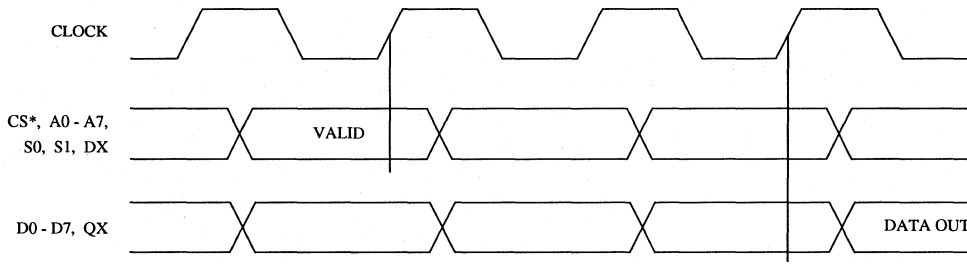

Figure 1. Read Timing (Synchronous Mode).

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Asynchronous Read/Write Operation

During asynchronous operation, the part may be both written to and read. In this instance, the internal input and output latches for the data and address paths are configured to be transparent.

The S0 and S1 inputs are used to specify whether the MPU is accessing the RAM or one of the overlay registers, as specified in Table 1. When accessing the RAM, A0–A7 specify which RAM location is being accessed. Otherwise, A0–A7 are ignored.

The WE* input specifies whether the MPU is reading (WE* = 1) or writing (WE* = 0) to the RAM or overlay registers.

Figure 2 illustrates the read timing and Figure 3 illustrates the write timing during asynchronous operation.

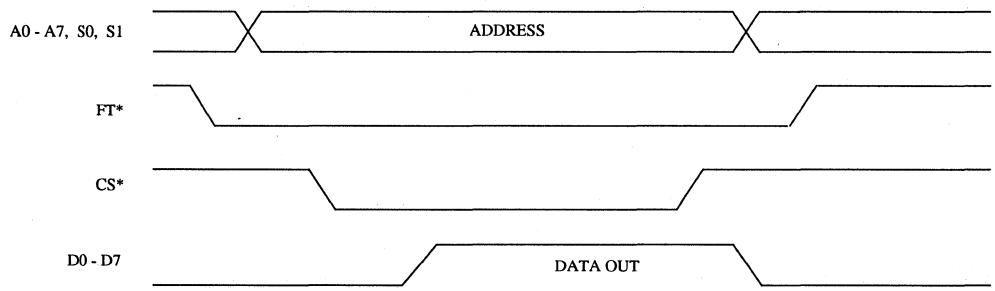


Figure 2. Read Timing (Asynchronous Mode, WE = 1).*

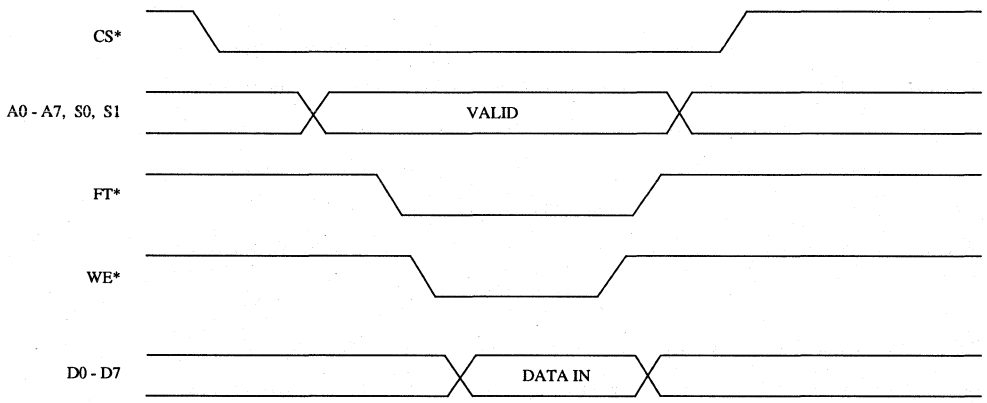
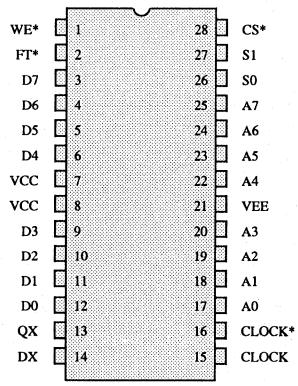


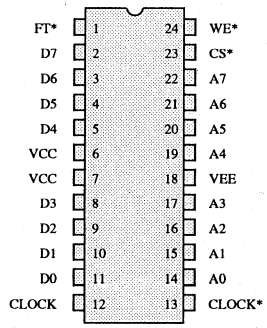
Figure 3. Write Timing (Asynchronous Mode).

Pin Descriptions

Pin Name	Description
CS*	Chip select control input (ECL compatible). A logical zero on this input enables data to be written to or read from the device. A logical one forces the D0–D7 pins to a logical zero. CS* is latched on the rising edge of CLOCK.
WE*	Write enable control input (ECL compatible). A logical zero on this input enables data to be written into the device. Data is internally latched on the rising edge of WE* (see Figure 1).
D0–D7	Bidirectional data bus (ECL compatible). D0 is the least significant bit. Data is transferred into and out of the device over this 8-bit data bus.
FT*	Feedthrough control input (ECL compatible). A logical one configures the device for synchronous operation, and a logical zero configures the device for asynchronous operation. The setup and hold times must be met when switching between synchronous and asynchronous operation. While FT* is a logical one, the rising edge of CLOCK latches the CS*, A0–A7, S0, and S1 inputs, and data is output onto D0–D7 following the rising edge of CLOCK. While FT* is a logical zero, the internal latches for these signals are transparent.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The device may be driven by a single-ended clock by connecting CLOCK* to VBB (–1.3 V).
A0–A7	Address inputs (ECL compatible). A0–A7 are used to specify which location in the RAM is being accessed, if both S0 and S1 are a logical zero. If either S0 or S1 is a logical one, A0–A7 are ignored (see Table 1).
S0, S1	Select control inputs (ECL compatible). On the Bt401, the S1 and S0 inputs specify whether the RAM or one of the overlay registers is being accessed. S0 and S1 are not incorporated on the Bt403 (see Table 1).
DX, QX	Pipe input and output (ECL compatible). The value of the DX input is latched on the rising edge of CLOCK and output onto QX two clock cycles later, regardless of the state of FT*. They are typically used to maintain synchronization of data and control signals. DX and QX are not incorporated on the Bt403.
VEE	Device power. All VEE pins must be connected.
VCC	Device ground. All VCC pins must be connected.



Bt401



Bt403

Bt401/403—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	V
Power Supply	VEE	–4.9	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+70	°C

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Bt401/403—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				–8.0	V
Voltage on any Pin (except D0–D7, QX)		0		VEE	V
Output Current				–30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bt401/403—DC Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	-1170 -1130 -1070		-840 -810 -735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	-1950 -1950 -1950		-1480 -1480 -1450	mV mV mV
Output High Voltage	VOH	0 +25 +70	-1020 -980 -920		-840 -810 -735	mV mV mV
Output Low Voltage	VOL	0 +25 +70	-1950 -1950 -1950		-1630 -1630 -1600	mV mV mV
Input Current High S0, S1, and CS* (Vin = VILmax)	IIH	0 +25 +70			200 200 200	µA µA µA
Input Current Low S0, S1, and CS* (Vin = VILmin)	IIL	0 +25 +70			150 150 150	µA µA µA
Input Current High All other pins (Vin = VIHmax)	IIH	0 +25 +70			20 20 20	µA µA µA
Input Current Low All other pins (Vin = VIHmin)	IIL	0 +25 +70			5 5 5	µA µA µA
VEE Supply Current	IEE	0 +25 +70			280 280 280	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with output loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Bt401/403—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			250	MHz
Read (Synchronous Mode) (Figure 4)					
Clock Cycle Time	1	4			ns
Clock Pulse Width High	2	1			ns
Clock Pulse Width Low	3	1			ns
Clock to Output Valid	4	0.5		2.5	ns
Input Setup Time	5	0			ns
Input Hold Time	6	2.0			ns
Pipeline Delay	7	3	3	3	Clocks
Read (Asynchronous Mode) (Figure 5)					
A0–A7 Access Time	8			10	ns
CS* Access Time	9			5	ns
CS* Recovery Time	10			5	ns
FT* Setup Time	11	5			ns
Write (Asynchronous Mode) (Figure 6)					
WE* Pulse Width Low	12	75			ns
A0–A7 Setup Time	13	5			ns
A0–A7 Hold Time	14	20			ns
D0–D7 Setup Time	15	55			ns
D0–D7 Hold Time	16	5			ns
CS* Setup Time	17	5			ns
CS* Hold Time	18	5			ns
FT* Setup Time	19	5			ns
FT* Hold Time	20	5			ns
Output Rise/Fall Time			2		ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with output loading of 50 Ω to –2.0 V. ECL input values are –0.89 to –1.69 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Output rise/fall time is measured between the 20-percent and 80-percent points. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Timing Waveforms

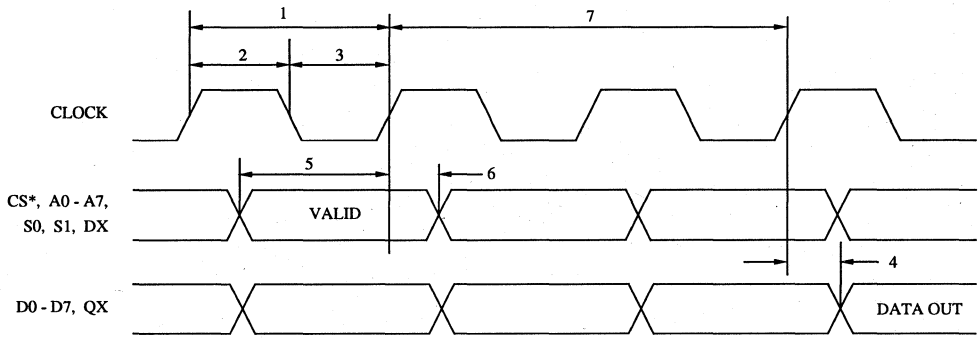


Figure 4. Read Timing (Synchronous Mode).

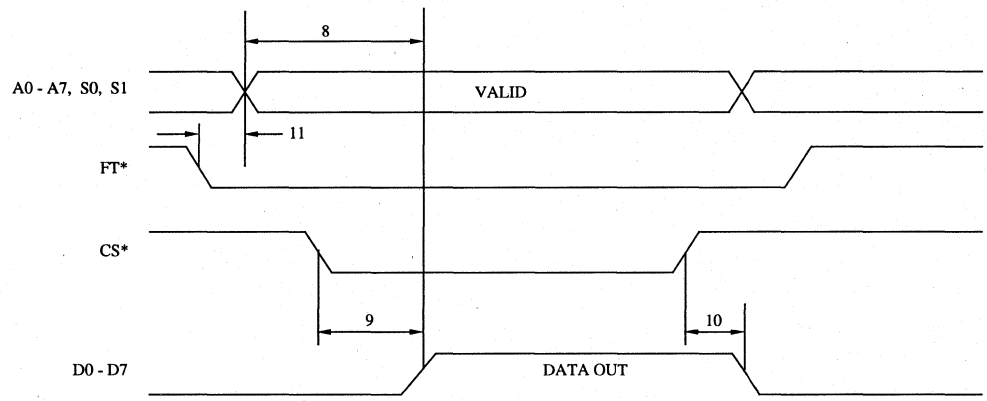


Figure 5. Read Timing (Asynchronous Mode, WE = 1).*

Timing Waveforms *(continued)*

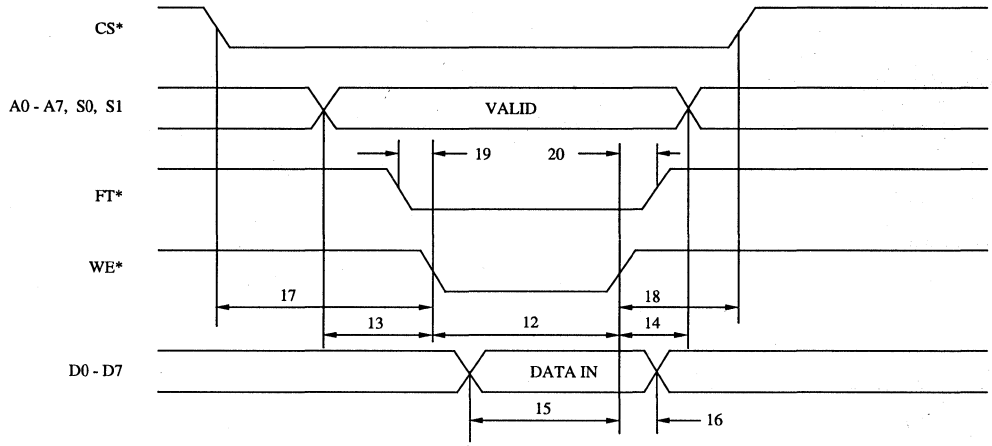


Figure 6. Write Timing (Asynchronous Mode).

Ordering Information

Model Number	Overlays	Compatibility	Package	Ambient Temperature Range
Bt401KC	3 x 8	10KH ECL	28-pin 0.6" CERDIP	0° to +70° C
Bt403KC	none	10KH ECL	24-pin 0.3" CERDIP	0° to +70° C

Bt424

250 MHz 40-bit Multitap TTL/ECL-Compatible Video Shift Register

Distinguishing Features

- 250 MHz Operation
- Overlay Support
- TTL Pixel Inputs
- TTL MPU Address Interface
- ECL Shift Register Outputs
- Shift-Enable and Output-Enable Controls
- Optional Single +5 V Operation
- 68-pin PGA Package with Alignment Pin
- Typical Power Dissipation: 1.25 W

Customer Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplifies PCB Layout
- Reduces PCB Interconnect
- Low Bus Loading
- Increases System Reliability

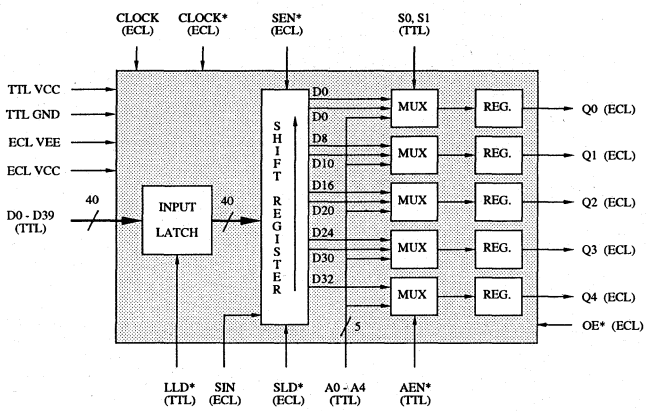
Configurations

- One 40-bit Shift Register
- Two 16-bit or 20-bit Shift Registers
- Five 8-bit Shift Registers
- Four 10-bit Shift Registers

Related Products

- Bt401/403
- Bt107
- Bt109
- Bt492

Functional Block Diagram



Product Description

The Bt424 is a 40-bit multitap shift register. It is designed specifically for high-resolution graphics systems.

TTL pixel data from the frame buffer is typically loaded at either one eighth or one tenth the clock rate (up to about 32 MHz) with the TTL-compatible LLD* signal. Data is then transferred from the input latch to the shift register using the ECL-compatible load signal (SLD*). The double-buffering of incoming pixel data simplifies system timing.

The shift register is clocked by the ECL-compatible CLOCK and CLOCK* inputs, and features ECL-compatible serial input (SIN) and shift-enable (SEN*) controls.

The Bt424 performs TTL-to-ECL translation of the MPU address (A0–A4), eliminating external address translators. The MPU address interface enables output of the MPU address (A0–A4) onto the Q0–Q4 pins, overriding the shift register data. This interface is controlled by the TTL-compatible address-enable (AEN*) signal.

The Bt424 has separate TTL and ECL supply pins, enabling operation from a single +5 V supply, or a +5 V and –5.2 V supply.

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Circuit Description

As illustrated in the functional block diagram, the Bt424 contains a 40-bit input latch, a 40-bit shift register, and control logic.

General Shift Register Operation

The 40-bit shift register has multiple taps, as illustrated in the functional block diagram. As illustrated in Figure 3 (Figures 3, 4, 5, 6, and 7 appear in the Timing Waveforms section, following AC characteristics), on the rising edge of LLD*, D0–D39 are latched into the input latch. Data is transferred from the input latch to the shift register synchronously on the rising edge of CLOCK while SLD* is a logical zero. While LLD* is a logical zero, the input latch is transparent, as illustrated in Figure 4.

The multiplexers select one of two taps from the 40-bit shift register or an MPU address input. The output of the multiplexers is registered synchronously to CLOCK and output onto the Q0–Q4 pins.

The SEN* input may be used to synchronously enable (logical zero) or disable (logical one) clocking of the shift register. This is useful for implementing hardware zooming in a graphics application. Figure 5 shows the shift timing and SEN* timing.

The OE* input is used to enable (logical zero) or disable (logical one) the outputs asynchronously to CLOCK, as shown in Figure 6.

Single 40-bit Shift Register Operation

When the Bt424 is used as a 40-bit shift register, only the Q0 output is used. The Q1–Q4 outputs are ignored. D0 is the first bit output, followed by D1, then D2, then D3, etc. SLD* and LLD* should occur once every 40 clock cycles. The state of the S0 and S1 inputs is not important, and they may be connected to TTL GND.

Single shift registers of any length (up to 40 bits) may be implemented by loading the parallel data at the appropriate time. For example, a 32-bit shift register may be implemented by loading parallel data once every 32 clock cycles.

Dual 20-bit Shift Register Operation

When the Bt424 is used as a dual 20-bit shift register, only the Q0 and Q2 outputs are used. The Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, then D2, then D3, etc. For Q2, D20 is the first bit output, followed by D21, then D22, etc. SLD* and LLD* should occur once every 20 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Dual 16-bit Shift Register Operation

When used as a dual 16-bit shift register, only the Q0 and Q2 outputs are used, and the Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, etc. For Q2, D16 is the first bit output, followed by D17, etc. SLD* and LLD* should occur once every 16 clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

Quad 10-bit Shift Register Operation

When the Bt424 is used as a quad 10-bit shift register, all output except Q4 (which is ignored) are used. For Q0, D0 is the first bit output, followed by D1, then D2, etc. For Q1, D10 is the first bit output, followed by D11, then D12, etc. For Q2, D20 is the first bit output, followed by D21, then D22, etc. For Q3, D30 is the first bit output, followed by D31, then D32, etc. SLD* and LLD* should occur once every 10 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Quint 8-bit Shift Register Operation

When the Bt424 is used as a quint 8-bit shift register, all outputs are used. For Q0, D0 is the first bit output, followed by D1, then D2, etc. For Q1, D8 is the first bit output, followed by D9, then D10, etc. For Q2, D16 is the first bit output, followed by D17, then D18, etc. For Q3, D24 is the first bit output, followed by D25, then D26, etc. For Q4, D32 is the first bit output, followed by D33, then D34, etc. SLD* and LLD* should occur once every eight clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

MPU Address Interface

The Bt424 accepts TTL-compatible MPU addresses (A0–A4) and translates them to ECL-compatible levels, eliminating the need for external TTL/ECL translators along the address path.

While AEN* is a logical one, pixel data from the shift register is output onto the Q0–Q4 pins. While AEN* is a logical zero, A0–A4 are output onto the Q0–Q4 pins. Figure 7 illustrates the MPU address timing. Q0–Q4 are always output following the rising edge of CLOCK regardless of the value of AEN*.

S0, S1 Select Inputs

S0 and S1 specify the configuration of the Bt424 as shown in Table 1.

S1	S0	Function
0	0	quad 10-bit
x	1	quint 8-bit
1	0	quad 8-bit, 8-bit overlay port

Table 1. S0, S1 Control Inputs.

Figure 1 shows use of the Bt424 in a typical graphics system. In this instance, the RAMDAC has separate (nonmultiplexed) pixel and overlay data inputs. Therefore, all three Bt424s are configured for the same mode of operation (either quad 10 bit or quint 8 bit, depending on the specific application).

Figure 2 shows a basic configuration of the Bt424 used with a RAMDAC that has multiplexed pixel and overlay inputs. The OL input of the RAMDAC specifies whether pixel (OL = 0) or overlay (OL = 1) data is present on P0–P7.

The Bt424s interfaced to bit planes 0–7 are configured to support overlays (S1 = 1 and S0 = 0). D0–D7, D8–D15, D16–D23, and D24–D31 are configured as four 8-bit pixel input ports, while D32–D39 are configured as an 8-bit overlay active input port. If D32–D39 contain a logical one on any bit, the Q0–Q3 outputs are disabled and forced to a logical zero. This enables overlay information to be wire-ORed onto the Q0–Q3 outputs.

The Bt424 interfaced to the overlay bit planes is configured as a quint 8-bit shifter and serializes the overlay information. The Q0–Q3 outputs are wire-ORed onto the pixel data bus to the RAMDAC. The D32–D39 inputs are serialized to generate the overlay enable (OL) control signal for the RAMDAC. If no overlay information is being displayed, the Q0–Q4 outputs are a logical zero, allowing normal pixel data to be displayed.

Eight four-input TTL OR gates are required to generate the overlay active signals to the Bt424s. D0, D8, D16, and D24 are ORed together to generate D32, D33, D34, etc.

Power Supply Operation

The Bt424 may operate from a +5 V and –5.2 V power supply, or from a single +5 V power supply, as called out in Table 2.

	Nominal Voltages Applied	
Supply Pin	Single Supply System	Dual Supply System
TTL VCC	+5.0 V	+5.0 V
TTL GND	0 V	0 V
ECL VCC	+5.0 V	0 V
ECL VEE	0 V	–5.2 V

Table 2. Power Supply Operation.

Inputs and outputs are temperature and voltage compensated.

Circuit Description *(continued)*

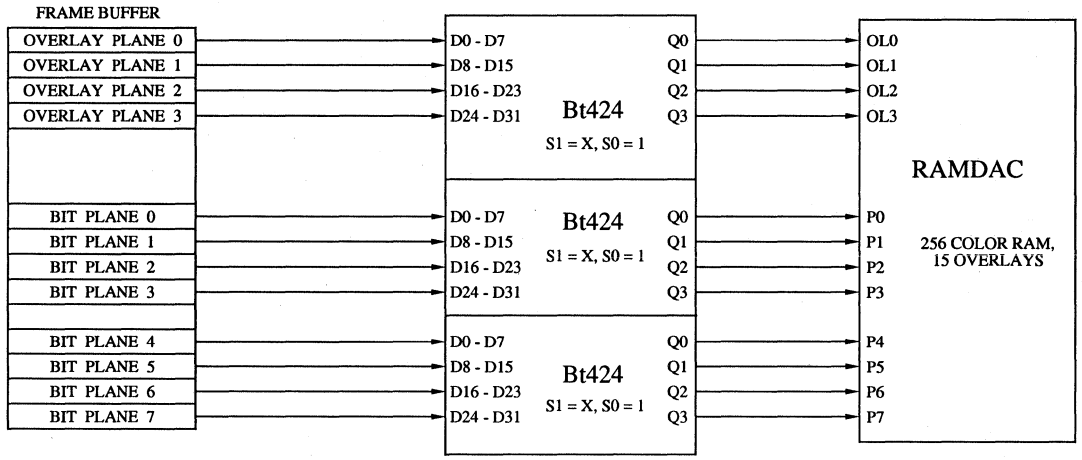


Figure 1. Using the Bt424 with Separate Pixel and Overlay Inputs (256 Colors, 15 Overlays).

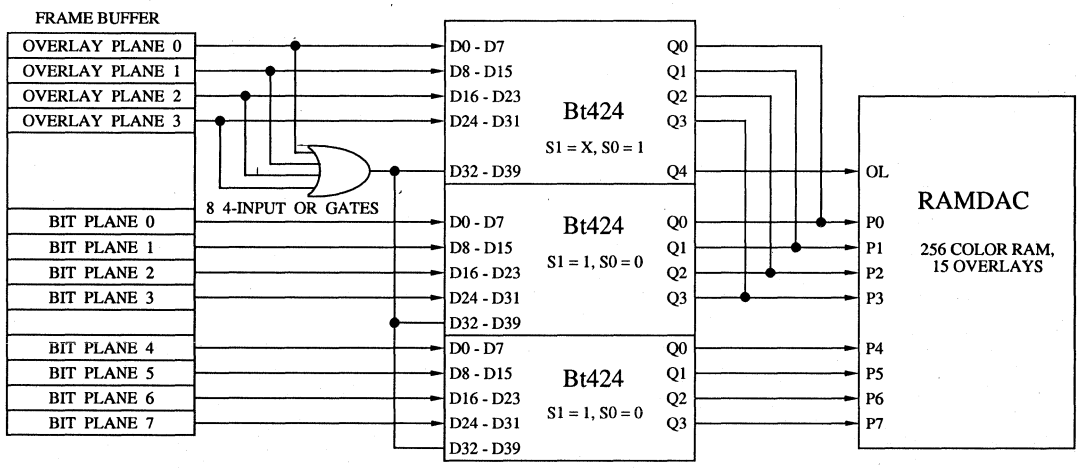


Figure 2. Using the Bt424 with Multiplexed Pixel/Overlay Inputs (256 Colors, 15 Overlays).

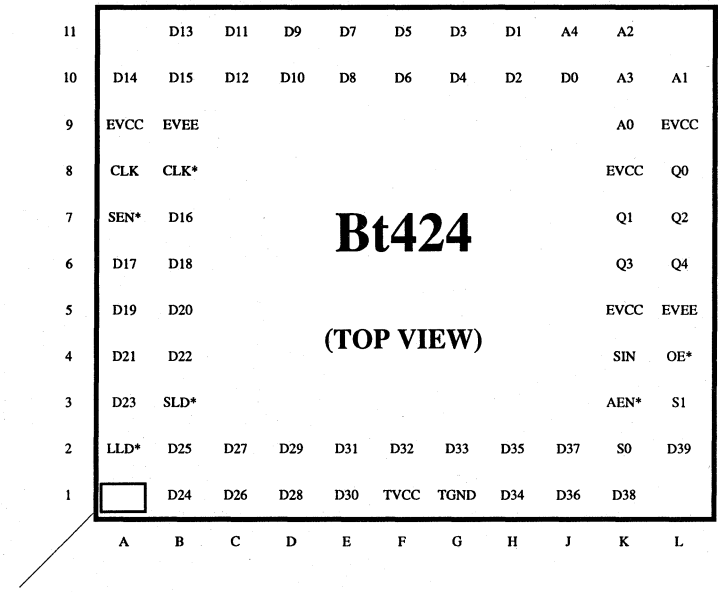
Pin Descriptions

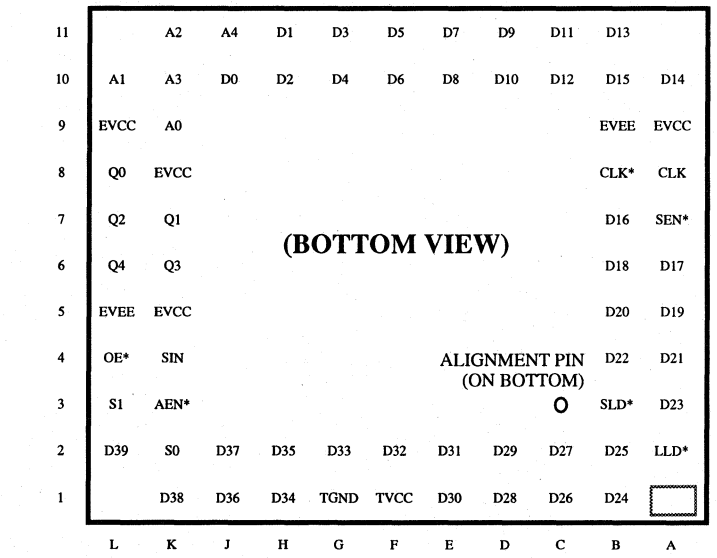
Pin Name	Description
D0–D39	Parallel data inputs (TTL compatible). These inputs are latched into the input latch on the rising edge of LLD*, asynchronous to CLOCK.
SIN	Shift data input (ECL compatible). This input is latched on the rising edge of CLOCK and may be used to serially load the shift register. If not used, it should be connected to ECL GND.
SEN*	Shift enable control input (ECL compatible). This input may be used to synchronously start or stop the shift register from clocking. A logical zero enables shifting, and a logical one disables shifting.
LLD*	Input latch load control input (TTL compatible). The rising edge of LLD* is used to latch D0–D39 into the input latch. While LLD* is a logical zero, the input latch is transparent.
SLD*	Shift register load control input (ECL compatible). SLD* is used to transfer data from the input latch to the shift register synchronously to CLOCK. Data is transferred on the rising edge of CLOCK while SLD* is a logical zero.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The clock rate is typically the pixel clock rate of the video system. The Bt424 may be used with a single-ended clock by connecting CLOCK* to VBB (–1.3 V)
Q0–Q4	Shift register outputs (ECL compatible). These pins output either D0–D39 data (AEN* = logical one) or A0–A4 data (AEN* = logical zero). Data is output following the rising edge of CLOCK.
OE*	Output enable control input (ECL compatible). A logical one forces the Q0–Q4 outputs to a logical zero, while a logical zero enables data to be output onto Q0–Q4. The Q0–Q4 outputs are enabled and disabled asynchronously to CLOCK.
S0, S1	Select control inputs (TTL compatible). These inputs control the operation of the device as specified in Table 1.
A0–A4	Address inputs (TTL compatible). These address inputs from the MPU are used to address the color palette RAM during MPU read/write cycles to the color palette RAM.
AEN*	Address enable control input (TTL compatible). While AEN* is a logical zero, A0–A4 are output onto Q0–Q4 following the rising edge of CLOCK. If AEN* is a logical one, A0–A4 are ignored.
TTL VCC	Power supply pins for the TTL-compatible circuitry.
TTL GND	Ground pins for the TTL-compatible circuitry.
ECL VEE	Power supply pins for the ECL-compatible circuitry.
ECL VCC	Ground pins for the ECL-compatible circuitry.

Pin Descriptions *(continued)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
CLOCK	A8	D0	J10	D25	B2
CLOCK*	B8	D1	H11	D26	C1
		D2	H10	D27	C2
LLD*	A2	D3	G11	D28	D1
SLD*	B3	D4	G10	D29	D2
SEN*	A7				
SIN	K4	D5	F11	D30	E1
S0	K2	D6	F10	D31	E2
S1	L3	D7	E11	D32	F2
		D8	E10	D33	G2
AEN*	K3	D9	D11	D34	H1
A0	K9				
A1	L10	D10	D10	D35	H2
A2	K11	D11	C11	D36	J1
A3	K10	D12	C10	D37	J2
A4	J11	D13	B11	D38	K1
		D14	A10	D39	L2
Q0	L8				
Q1	K7	D15	B10	TTL VCC	F1
Q2	L7	D16	B7		
Q3	K6	D17	A6	TTL GND	G1
Q4	L6	D18	B6		
		D19	A5	ECL VEE	B9
OE*	L4			ECL VEE	L5
		D20	B5		
		D21	A4	ECL VCC	A9
		D22	B4	ECL VCC	K5
		D23	A3	ECL VCC	K8
		D24	B1	ECL VCC	L9

Pin Descriptions *(continued)*





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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	V
ECL Device Ground	ECL VCC	0	0	0	V
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	V
ECL Power Supply	ECL VEE	–4.2	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+70	°C

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	V
TTL VCC (measured to TTL GND)				+7.0	V
Voltage on Any ECL Pin		0		ECL VEE	V
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	V
Q0–Q4 Output Current				–30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 1) Input Low Voltage (Note 1)	VIH VIL	–1165 –1810		–880 –1475	mV mV
Output High Voltage (Note 1) Output Low Voltage (Note 1)	VOH VOL	–1025 –1810		–880 –1620	mV mV
Input High Current (Vin = VIHmax) Input Low Current (Vin = VILmin)	IIH IIL			500 400	µA µA
ECL VEE Supply Current	IEE			240	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Note 1: Relative to ECL VCC.

TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 1)	VIH	2.0		TTL VCC +0.5	V
Input Low Voltage (Note 1)	VIL	TTL GND –0.5		0.8	V
Input High Current (Vin = 2.4 V) Input Low Current (Vin = 0.4 V)	IIH IIL			70 –0.7	µA mA
TTL VCC Supply Current	ICC			100	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Relative to TTL GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			250	MHz
Clock Cycle Time	1	4			ns
Clock Pulse Width High Time	2	1.5			ns
Clock Pulse Width Low Time	3	1.5			ns
LLD* Pulse Width Low Time	4	7			ns
LLD* Setup Time	5	8			ns
SLD Setup Time	6	2			ns
SLD Hold Time	7	0.5			ns
D0–D39 Setup Time to LLD*	8	7			ns
D0–D39 Setup Time to Clock	9	10			ns
D0–D39 Hold Time to LLD*	10	0			ns
D0–D39 Hold Time to Clock	11	0			ns
Q0–Q4 Output Delay	12	1.5		4	ns
SEN* Setup Time	13	2			ns
SEN* Hold Time	14	1			ns
SIN Setup Time	15	2.5			ns
SIN Hold Time	16	1.5			ns
OE* Pulse Width Low Time	17	4			ns
OE* Enable Time	18			3.5	ns
OE* Disable Time	19			4	ns
A0–A4 Setup Time	20	12			ns
A0–A4 Hold Time	21	0			ns
AEN* Setup Time	22	5			ns
AEN* Hold Time	23	0			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are –0.89 to –1.69 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Timing Waveforms

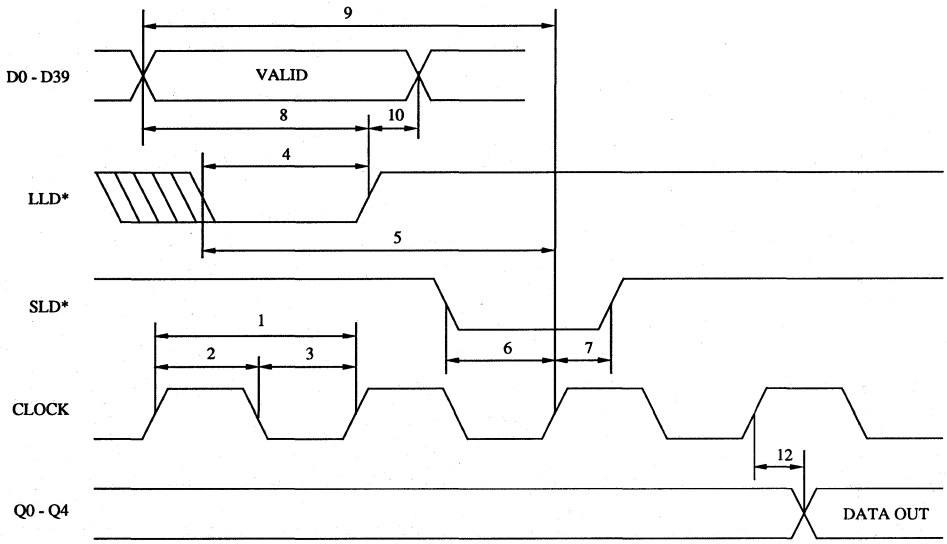


Figure 3. Load Latch and Register Timing.

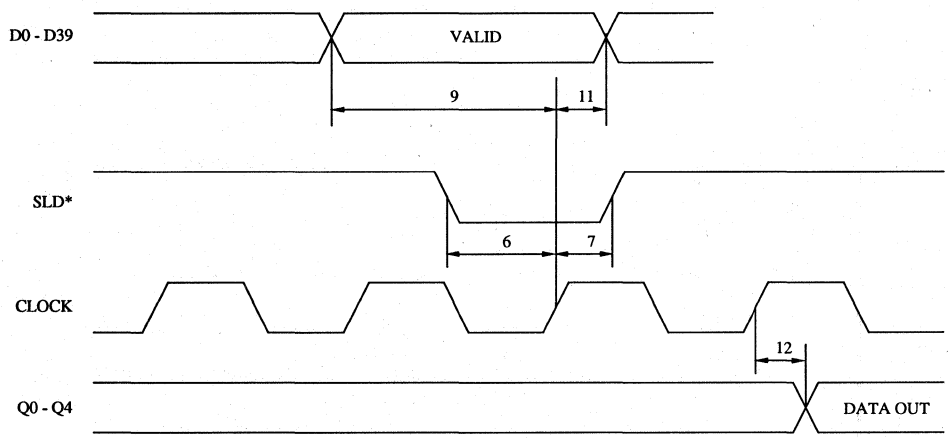


Figure 4. Transparent Latch Timing (LLD = Logical Zero).*

Timing Waveforms *(continued)*

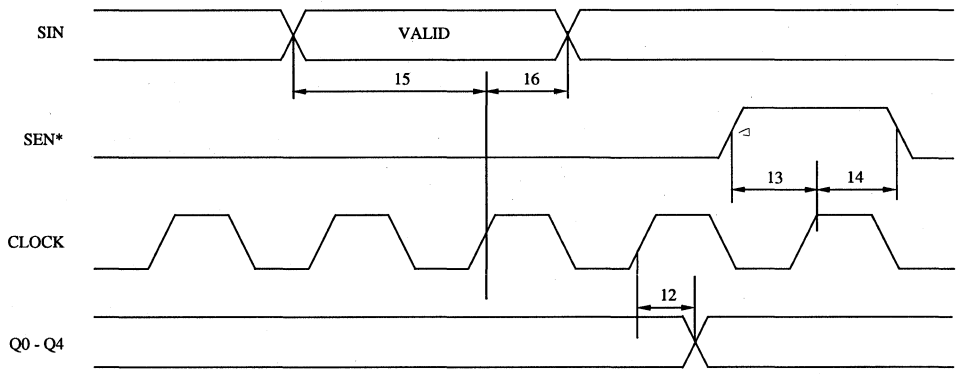


Figure 5. Shift Timing (SLD* = Logical One).

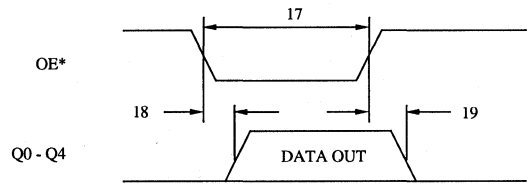


Figure 6. Output Enable Timing.

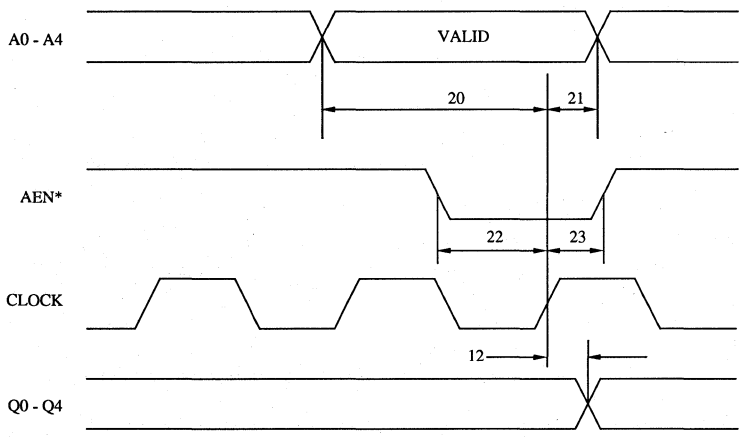


Figure 7. Address Enable Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt424KG	68-pin Ceramic PGA with Alignment Pin	0° to +70° C

Bt431

Monolithic CMOS 64 x 64 Pixel Cursor Generator

Distinguishing Features

- 64 x 64 Pixel User-Definable Cursor
- Full-Screen/Window Cross Hair Cursor
- Pixel Positioning of Cursors
- Supports Pixel Rates up to 175 MHz
- 1:1, 4:1, and 5:1 Output Multiplexing
- TTL-Compatible Inputs/Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 24-pin 0.3" DIP or 28-pin PLCC Package
- Typical Power Dissipation: 450 mW

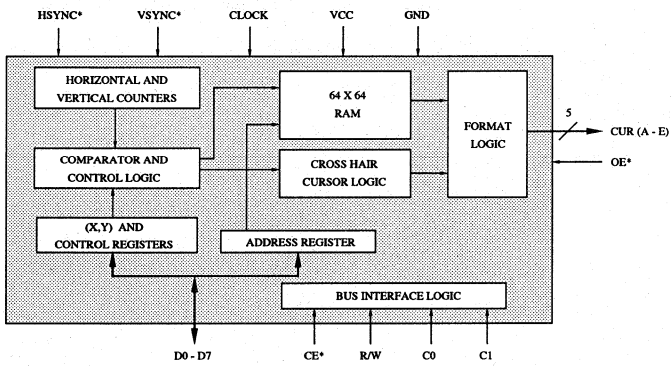
Applications

- High-Resolution Color Graphics
- Image Processing

Customer Benefits

- Reduces Component Count
- Reduces PCB Area Requirements
- Simplifies Cursor Implementation
- Allows Fast Cursor Movement
- Simplifies Software Interface

Functional Block Diagram



Product Description

The Bt431 cursor generator provides a 64 x 64 pixel user-definable cursor and a cross hair cursor for high-resolution, noninterlaced, monochrome or color graphics systems. The cross hair cursor may be implemented as a full-screen or full-window cross hair cursor. Both the user-definable cursor and the cross hair cursor may be displayed simultaneously with logical OR and exclusive-OR operations supported. Either cursor may be moved off the top, bottom, left, or right side of the display without wraparound.

The cursors may be positioned with pixel resolution, and their display may be individually enabled or disabled. A standard MPU bus interface is supported, simplifying system design.

The Bt431 may be programmed to output cursor information for 1, 4, or 5 horizontally consecutive pixels, enabling it to be interfaced to either the multiplexed or nonmultiplexed overlay inputs of Brooktree RAMDACs.

The 5:1 output multiplex mode enables support of pixel rates up to 175 MHz.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt431 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and cursor RAM.

The MPU interface signals consist of D0–D7, CE*, R/W, C0, and C1. Table 1 is the truth table for the control inputs, and Figure 1 illustrates the MPU read/write timing of the device.

Two 8-bit address registers (address register0 and address register1), cascaded to form a 16-bit address pointer register, are used to address the internal control registers and cursor RAM, as specified in Table 2. During read/write cycles to the cursor RAM, the 9 least significant bits of the address pointer register (ADDR0–ADDR8) are incremented following each read or write cycle to the cursor RAM. Thus, the MPU may load the address pointer register with the desired starting cursor RAM address and burst load new cursor RAM data by writing up to 512 bytes of data to the device. Following a read or write cycle to RAM location $01FF, the address pointer register resets to $0000.

During accesses to the control registers, ADDR0–ADDR8 are incremented after any read or write cycle to a register. While accessing the control registers, the address pointer register will reset to $0000 only following a write cycle to location $01FF. The address register is not incremented when read or written to.

RAMDAC Interface

The Bt431 is designed to generate cursor information with the overlay input ports of Brooktree RAMDACs.

The Bt431 may be interfaced directly to RAMDACs with 4:1 or 5:1 multiplexed overlay ports, supporting display resolutions up to 1280 x 1024 pixels. In this instance, the CUR (A–E) outputs of the Bt431 will connect directly to the overlay inputs of the RAMDAC, and the CLOCK input of the Bt431 would typically be connected directly to the LD* or LDOUT pin of the RAMDAC. The Bt431 must be programmed to output either 4 or 5 horizontally consecutive pixels of cursor information each CLOCK cycle. This enables the Bt431 to output cursor information at an effective 175 MHz rate (in 5:1 mode).

To support RAMDACs with nonmultiplexed overlay inputs, the Bt431 may be programmed to output a single pixel of cursor information each CLOCK cycle. In this configuration, the CURA output of the Bt431 will connect directly to one of the overlay inputs of the RAMDAC. This configuration limits the cursor information to an effective 35 MHz rate. The CLOCK input of the Bt431 is typically connected directly to the CLOCK input of the RAMDAC.

The Bt431 may be configured for 4:1 or 5:1 output multiplexing, and an external shift register may be used (with appropriate control logic) to interface to RAMDACs whose input pixel rate is greater than 35 MHz. In this configuration, the CLOCK must be driven at one fourth or one fifth the pixel clock rate. Pixel rates up to 175 MHz may be supported by this technique.

R/W	C1	C0	
0	0	0	write address register0
0	0	1	write address register1
0	1	0	write to RAM location specified by address pointer register
0	1	1	write to control register specified by address pointer register
1	0	0	read address register0
1	0	1	read address register1
1	1	0	read RAM location specified by address pointer register
1	1	1	read control register specified by address pointer register

Table 1. MPU Control Truth Table.

Circuit Description *(continued)*

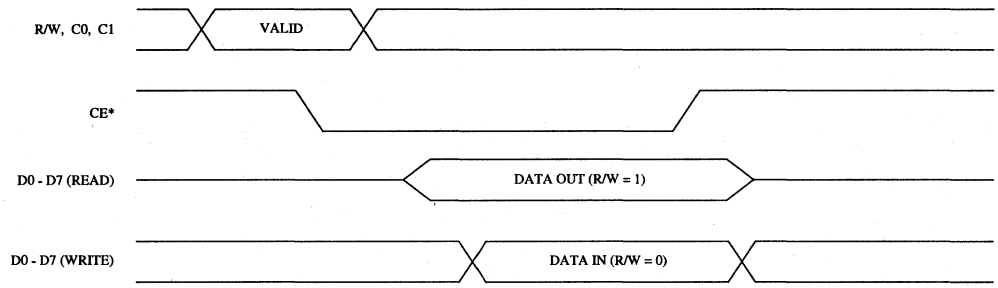


Figure 1. MPU Read/Write Timing.

	Address Pointer Register (ADDR15–ADDR0)		
C0	**Address Register1 (D7–D0)**	**Address Register0 (D7–D0)**	**Register/RAM Location Addressed**
0	0000 0000	0000 0000	cursor RAM location $000
0	0000 0000	0000 0001	cursor RAM location $001
:	:	:	:
0	0000 0000	1111 1111	cursor RAM location $0FF
0	0000 0001	0000 0001	cursor RAM location $100
0	0000 0001	0000 0001	cursor RAM location $101
:	:	:	:
0	0000 0001	1111 1111	cursor RAM location $1FF
1	xxxx xxxx	xxxx 0000	command register
1	xxxx xxxx	xxxx 0001	cursor (x) low register
1	xxxx xxxx	xxxx 0010	cursor (x) high register
1	xxxx xxxx	xxxx 0011	cursor (y) low register
1	xxxx xxxx	xxxx 0100	cursor (y) high register
1	xxxx xxxx	xxxx 0101	window (x) low register
1	xxxx xxxx	xxxx 0110	window (x) high register
1	xxxx xxxx	xxxx 0111	window (y) low register
1	xxxx xxxx	xxxx 1000	window (y) high register
1	xxxx xxxx	xxxx 1001	window width low register
1	xxxx xxxx	xxxx 1010	window width high register
1	xxxx xxxx	xxxx 1011	window height low register
1	xxxx xxxx	xxxx 1100	window height high register

Table 2. Address Pointer Register.

Circuit Description *(continued)*

64 x 64 Cursor Positioning

When the cursor RAM is being displayed, its contents are output onto the CUR (A–E) outputs. A logical one in the cursor RAM causes output of a logical one onto the appropriate CUR (A–E) output during the appropriate clock cycle. The cursor pattern may be changed by changing the contents of the cursor RAM (see Figure 2).

The 64 x 64 cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the thirty-first column of the 64 x 64 RAM (assuming the columns start with 0 for the leftmost pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the thirty-first row of the 64 x 64 RAM (assuming the rows start with 0 for the topmost pixel and increment to 63).

The Bt431 expects (x) to increase to the right and (y) to increase down, as shown on the display screen.

The cursor (x) position is relative to the first rising edge of CLOCK following the falling edge of HSYNC*. The software must take into account the internal pipeline delays, the amount of skew between the output cursor data and external pixel data, and whether output multiplexing is 1:1, 4:1, or 5:1.

The cursor (y) position is relative to the first falling edge of HSYNC* that is at two or more clock cycles after the falling edge of VSYNC* (see Figure 2).

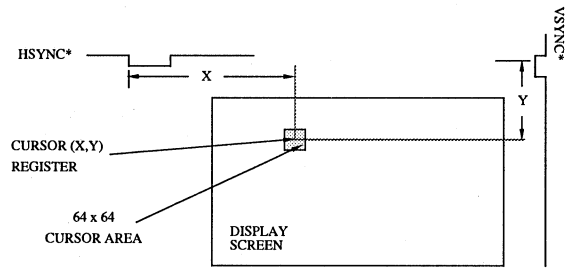


Figure 2. 64 x 64 Cursor Positioning.

Circuit Description *(continued)*

Cross Hair Cursor Positioning

The cross hair cursor is also positioned through the cursor (x,y) register (see Figure 3).

The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than 1 pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, a logical one is output onto the appropriate CUR (A–E) output during the appropriate clock cycle.

The cross hair cursor can be displayed only within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, the software must ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000, and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of CLOCK following the falling edge of HSYNC*. The software must take into account the internal pipeline delays, the amount of skew between the output cursor data and the external pixel data, and whether output multiplexing is 1:1, 4:1, or 5:1.

The cursor (y) position is relative to the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC*.

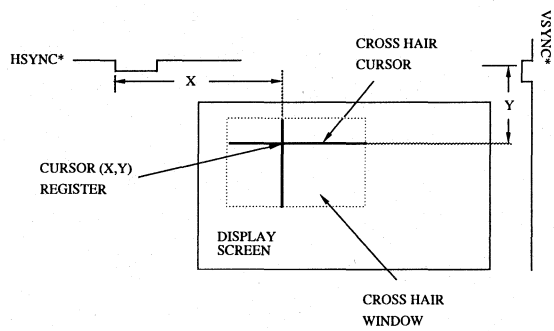


Figure 3. Cross Hair Cursor Positioning.

Circuit Description *(continued)*

Dual Cursor Positioning

Both the 64 x 64 cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

During the 64 x 64 pixel area in which the user-definable cursor will be displayed, the contents of the cursor RAM may be logically ORed or exclusive-ORed with the cross hair cursor information.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31,31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical directions, there will be a 1-pixel offset from the true center of the cross hair cursor.

Figure 4 illustrates dual cursor display, and Figure 5 illustrates the video input/output timing of the Bt431.

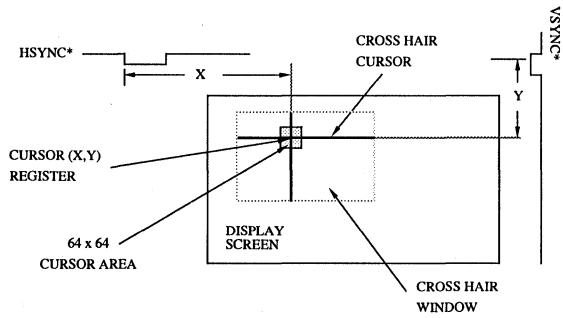


Figure 4. Dual Cursor Positioning.

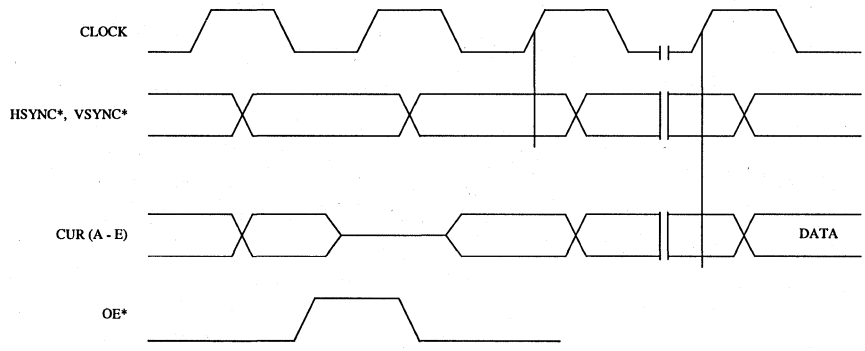


Figure 5. Video Input/Output Timing.

Cursor (x,y) Register

These registers are used to specify either the (x,y) coordinate of the center of the 64 x 64 pixel cursor window or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + D + H–P

where

P = 37 if 1:1 output multiplexing, 52 if 4:1 output multiplexing, and 57 if 5:1 output multiplexing
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of CLOCK following the falling edge of HSYNC* to active video

The P value is one-half cursor RAM width + (internal pipeline delay in clock cycles * one, four, or five, depending on multiplex selection)

Values from $0000 to $0FFF may be written into the cursor (x) register.

Internal Registers *(continued)*

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC* to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used when V < 32, and the cursor must be moved off the top of the screen.

The cursor (x,y) registers should be written to only during the vertical retrace interval. A falling edge of VSYNC* should not occur between the time the MPU writes the first byte of (x,y) and the last (fourth) byte of (x,y) information. Otherwise, temporary tearing of the cursor may occur.

Cursor RAM

This 64 x 64 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window. It is not initialized and may be written to or read by the MPU at any time. As MPU accesses to the cursor RAM have priority over the cursor display process, the cursor RAM should not be accessed during the horizontal sync intervals to minimize contention of the cursor updating and displaying processes.

During MPU accesses to the cursor RAM, the address pointer register is used to address the cursor RAM, as shown below. Figure 6 illustrates the internal format of the cursor RAM as it appears on the display screen.

Address Pointer Register Value	Address RAM Location
$0000	byte $000
$0001	byte $001
:	:
$01FF	byte $1FF

As shown in Figure 6, bit D7 is the leftmost pixel within a segment of 8 pixels. This enables the software generation of cursor patterns without bit swapping to obtain the desired pattern.

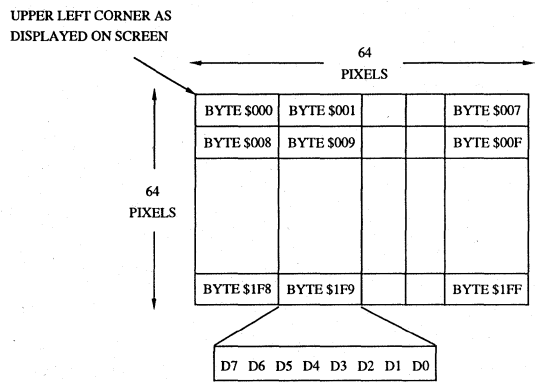


Figure 6. Cursor RAM as Displayed on the Screen.

Window (x,y) Register

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always logical zeros.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + D + H–P

where

P = 5 if 1:1 output multiplexing, 20 if 4:1 output multiplexing, and 25 if 5:1 output multiplexing
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of CLOCK following the falling edge of HSYNC* to active video

The P value is the number of internal pipeline delays times one, four, or five, depending on the multiplex selection.

Internal Registers *(continued)*

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC* to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair cursor is implemented by loading the window (x,y) registers with $0000, and the window width and height registers with $0FFF.

The window (x,y) registers should be written to only during the vertical retrace interval. A falling edge of VSYNC* should not occur between the time the MPU writes the first byte of (x,y) and the last (fourth) byte of (x,y) information. Otherwise, temporary repositioning of the cross hair cursor may occur.

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always logical zeros.

	Window Width High (WWHR)				**Window Width Low (WWLR)**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				**Window Height Low (WHLR)**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 output multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels for 1:1, 4:1, and 5:1 multiplexing, respectively; and the minimum window height is 2 pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

The window width and height registers should be written to only during the vertical retrace interval. A falling edge of VSYNC* should not occur between the time the MPU writes the first byte and the last (fourth) byte of information. Otherwise, temporary resizing of the cross hair cursor may occur.

Internal Registers *(continued)*

Command Register

The command register is used to control various functions of the Bt431. It is not initialized and may be written to or read by the MPU at any time.

D7 — Reserved. This bit should always be a logical zero.

D6 — 64 x 64 cursor enable. A logical one enables output of the contents of the cursor RAM during times that user-definable cursor information is to be displayed. A logical zero disables output of the cursor RAM information.

D5 — Cross hair cursor enable. A logical one enables output of cross hair cursor information. A logical zero disables output of the cross hair cursor information.

D4 — Cursor format control. If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.

D3, D2 — Multiplex control. These 2 bits specify whether 1, 4, or 5 bits of cursor information are output every clock cycle, as follows:

(00) 1:1 multiplexing
(01) 4:1 multiplexing
(10) 5:1 multiplexing
(11) reserved

D1, D0 — Cross hair cursor thickness. These 2 bits specify whether the horizontal and vertical thickness of the cross hair is 1, 3, 5, or 7 pixels, as follows:

(00) 1 pixel
(01) 3 pixels
(10) 5 pixels
(11) 7 pixels

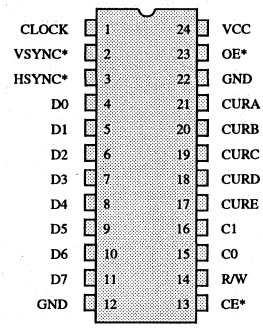
The horizontal and vertical segments are centered about the value in the cursor (x,y) register.

Pin Descriptions

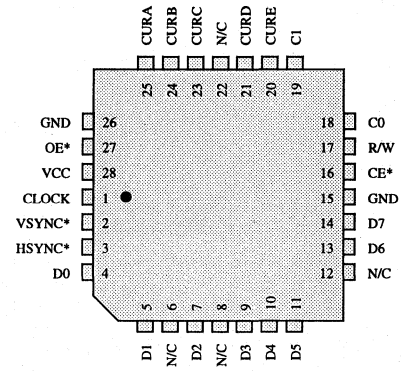
Pin Name	Description
VSYNC*	Vertical sync control input (TTL compatible). A logical zero indicates that the display is currently in the vertical sync interval. It is latched on the rising edge of CLOCK.
HSYNC*	Horizontal sync control input (TTL compatible). A logical zero indicates that the display is currently in the horizontal sync interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK is used to latch the VSYNC* and HSYNC* inputs, and to output cursor information onto the CUR (A–E) outputs. It is recommended that the CLOCK input be driven by a dedicated TTL buffer. If programmed for 1:1 output multiplexing, CLOCK should be the pixel clock rate. When programmed for 4:1 or 5:1 output multiplexing, CLOCK should be one fourth or one fifth the pixel clock rate, respectively.
CUR (A–E)	Cursor outputs (TTL compatible). During the pixel times that cursor information is to be displayed, either cross hair cursor information or the contents of the cursor RAM are output onto these pins. If programmed for 4:1 output multiplexing, the CURE output will be a logical zero. If programmed for 1:1 output multiplexing, the CURB, CURC, CURD, and CURE outputs will always be logical zeros. When programmed for 4:1 or 5:1 multiplexing, CURA corresponds to the leftmost pixel, followed by CURB, then CURC, etc., repeating every 4 or 5 pixels.
OE*	Output enable control input (TTL compatible). A logical one asynchronously three-states the CUR (A–E) outputs, and a logical zero asynchronously enables output of cursor data on the cursor outputs.
R/W	Read/write control input (TTL compatible). A logical zero indicates that the MPU is writing data to the device, and a logical one indicates that the MPU is reading data from the device (see Figure 1).
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (see Figure 1).
C0, C1	Control inputs (TTL compatible). These inputs specify the operation the MPU is performing (see Tables 1 and 2).
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VCC	Power.
GND	Ground.

Pin Descriptions *(continued)*

24-pin DIP Package



28-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt431.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information

Power-up Initialization

Following a power-up sequence, the Bt431 must be initialized. The following sequence is recommended:

1. Write $0000 to address pointer register.
2. Do 13 write cycles to control registers.
3. Write $0000 to address pointer register.
4. Do 512 write cycles to the cursor RAM.

Prior to the above sequence, the MPU may perform diagnostic checks on the device, such as a check that the RAM and control registers may be written to and read back.

Loading the Cursor RAM

When changing the cursor pattern, it is recommended that the following sequence be used to load the cursor RAM:

1. Write $0000 to address pointer register.
2. Do 512 write cycles to the cursor RAM.

Moving the Cursor

It is recommended that the following sequence be used to update the cursor (x,y) register:

1. Write $0001 to address pointer register.
2. Read cursor (x) low.
3. Read cursor (x) high.
4. Read cursor (y) low.
5. Read cursor (y) high.
6. Calculate new (x,y) value.
7. Write $0001 to address pointer register.
8. Write new cursor (x) low.
9. Write new cursor (x) high.
10. Write new cursor (y) low.
11. Write new cursor (y) high.

The above sequence also applies to updating the window (x,y) register, except $0005 should be written to the address pointer register.

Changing the Window Size

To change the size of the cross hair window, it is recommended that the following sequence be used:

1. Write $0009 to address pointer register.
2. Read window width low.
3. Read window width high.
4. Read window height low.
5. Read window height high.
6. Calculate new window width/height.
7. Write $0009 to address pointer register.
8. Write new window width low.
9. Write new window width high.
10. Write new window height low.
11. Write new window height high.

Using Multiple Devices

Multiple Bt431s may be used to generate more than one cursor, or to generate a multicolor cursor.

If multiple devices are being used to generate more than one cursor, the cursor outputs may be logically gated together, or each Bt431 may interface to a separate overlay input of the RAMDAC. If separate overlay inputs are used, the cursors will be automatically prioritized depending on which overlay is used for each cursor.

To generate a multicolor cursor with more than one Bt431 (for example, to generate a three-color cursor with two Bt431s), each Bt431 must interface to a separate overlay input of the RAMDAC. Either a separate cursor (x,y) calculation for each Bt431 may be performed, or the same cursor (x,y) calculation may be used with the cursor information appropriately offset in the cursor RAM.

Interfacing to the Bt453 and Bt458

Figure 7 illustrates interfacing a single Bt431 to the Bt453 RAMDAC, and Figure 8 illustrates interfacing to the Bt458 RAMDAC.

Interfacing to the Bt451, Bt454, Bt457, and Bt461/462 RAMDACs is similar to interfacing to the Bt458 because of the multiplexed overlay inputs of these devices. When the Bt431 is interfaced to the Bt454, the CLOCK pin of the Bt431 should be connected to the LDOUT pin of the Bt454, and the Bt431 should be configured for 4:1 output multiplexing. Interfacing to the Bt450, Bt473, Bt475/477, Bt479, and Bt471/476/478 RAMDACs is similar to interfacing to the Bt453.

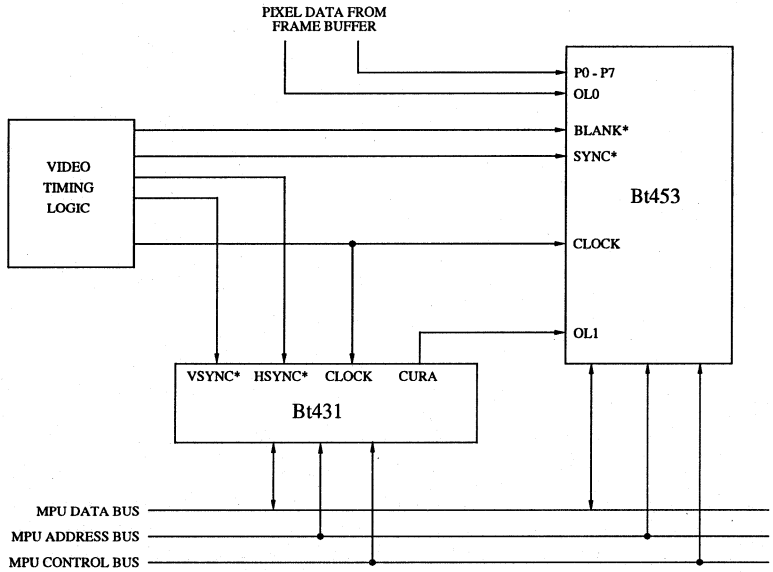


Figure 7. Interfacing to the Bt453.

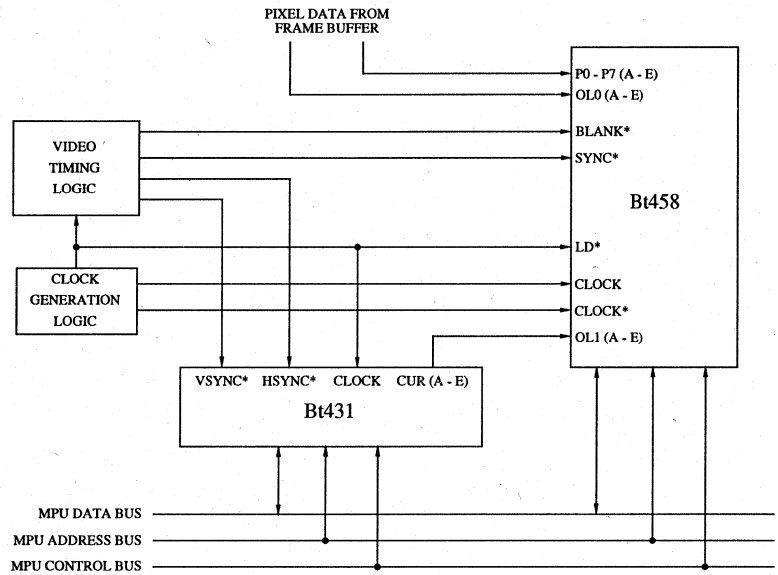


Figure 8. Interfacing to the Bt458.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VCC + 0.5	V
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	COUT		20		pF
Digital Outputs (CURA–CURE)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate (per 1, 4, or 5 pixels)	Fmax			35	MHz
C0, C1, R/W Setup Time	1	10			ns
C0, C1, R/W Hold Time	2	15			ns
CE* Low Time	3	50			ns
CE* High Time	4	25			ns
CE* Asserted to Data Bus Driven	5	6			ns
CE* Asserted to Data Valid	6			100	ns
CE* Negated to Data Bus 3-Stated	7			15	ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	4	2.5		ns
VSYNC*, HSYNC* Setup Time	10	10			ns
VSYNC*, HSYNC* Hold Time	11	5			ns
VSYNC*, HSYNC* Low Time		4			Clocks
VSYNC*, HSYNC* High Time		4			Clocks
Clock Cycle Time	12	28.6			ns
Clock Pulse Width High	13	10			ns
Clock Pulse Width Low	14	10			ns
Pipeline Delay	15			5	Clocks
Output Delay	16			20	ns
Three-State Disable Time	17			15	ns
Three-State Enable Time	18			15	ns
VCC Supply Current (Note 1)	ICC			100	mA

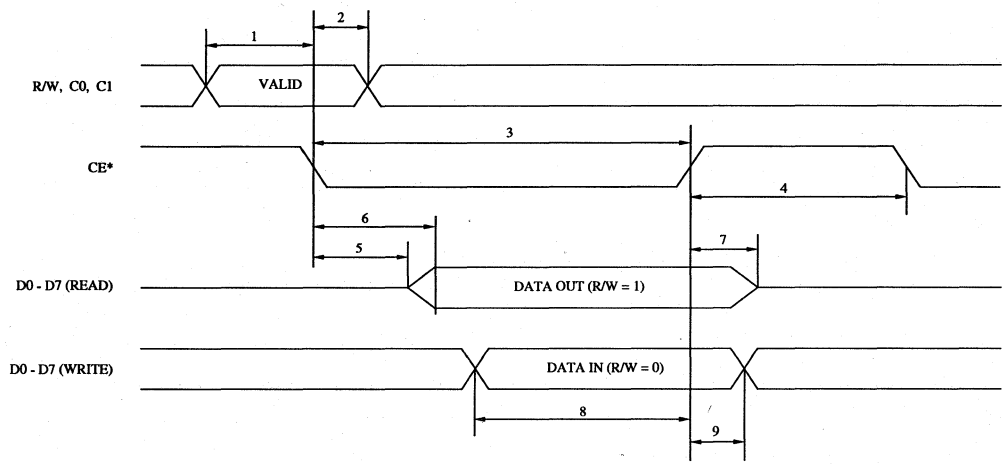
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. CURA–CURE output load ≤ 10 pF and D0–D7 output load ≤ 130 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: At Fmax. ICC (typ) at VAA = 5.0 V. ICC (max) at VAA = 5.25 V.

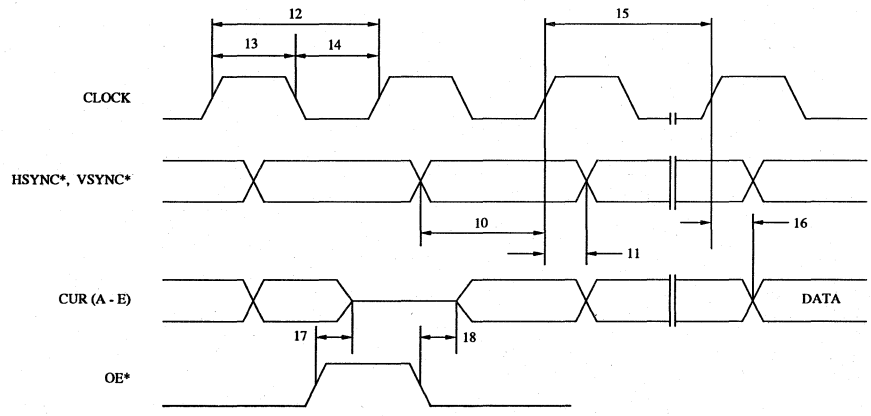
Ordering Information

Model Number	Package	Ambient Temperature Range
Bt431KC	24-pin 0.3" CERDIP	0° to +70° C
Bt431KPJ	28-pin Plastic J-Lead	0° to +70° C

Timing Waveforms



MPU Read/Write Timing.



Video Input/Output Timing.

Bt438

250 MHz Clock Generator Chip for CMOS RAMDACs™

Distinguishing Features

- 250 MHz Operation
- Differential ECL Clock Generation
- Ability to Divide by 3, 4, 5, or 8 of the Clock
- Ability to Divide by 2 and 4 of the Load
- Ability to Reset Pipeline Delay of the RAMDAC
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 20-pin DIP or 28-pin PLCC Package
- Typical Power Dissipation: 325 mW

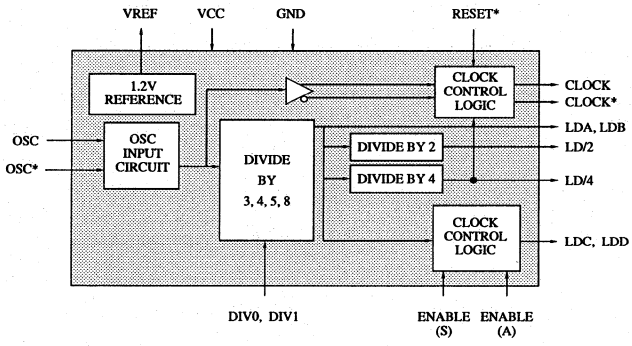
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Reduces Cost over Discretes
- Increases System Reliability

Related Products

- Bt439
- Bt440

Functional Block Diagram



Product Description

The Bt438 is a clock generator for the high-speed Brooktree CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5 V supply to the RAMDAC, generating the necessary clock and control signals.

The clock output can be divided by 3, 4, 5, or 8 to generate the load signal. The load signal can also be divided by 2 and 4 to, for example, clock video timing logic.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt438 optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2 V voltage reference is also provided, and may be used to provide the reference voltage for up to four RAMDACs.

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L438001 Rev. M

Brooktree®

Circuit Description

The Bt438 is designed to interface to a 10KH ECL crystal oscillator and generate the clock signals required by the RAMDACs. The OSC and OSC* inputs are designed to interface to a 10KH ECL oscillator operating from a single +5 V power supply.

The CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5 V power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by 3, 4, 5, or 8 to generate the LDA and LDB signals. LDA is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros.

ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were in when the ENABLE (A) input went to a logical zero.

ENABLE (A) and ENABLE (S) should not be a logical zero simultaneously. If this occurs, synchronous control of LDC and LDD by ENABLE (S) is not guaranteed.

While both ENABLE (S) and ENABLE (A) are logical ones, LDC and LDD will be free running, and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally nonclocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt438, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt438 to set the pipeline delay of the RAMDACs to a specified number of clock cycles. (The exact number depends on the RAMDAC.) Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt438 also generates a 1.2 V (typical) voltage reference that may be used to drive the VREF input of up to four RAMDACs.

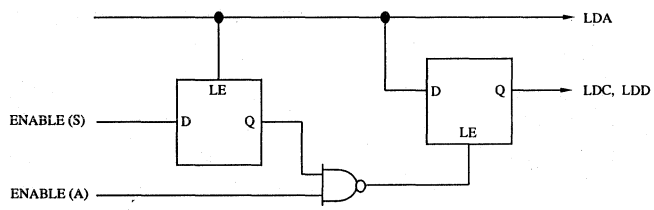


Figure 1. ENABLE Control Implementation.

Circuit Description *(continued)*

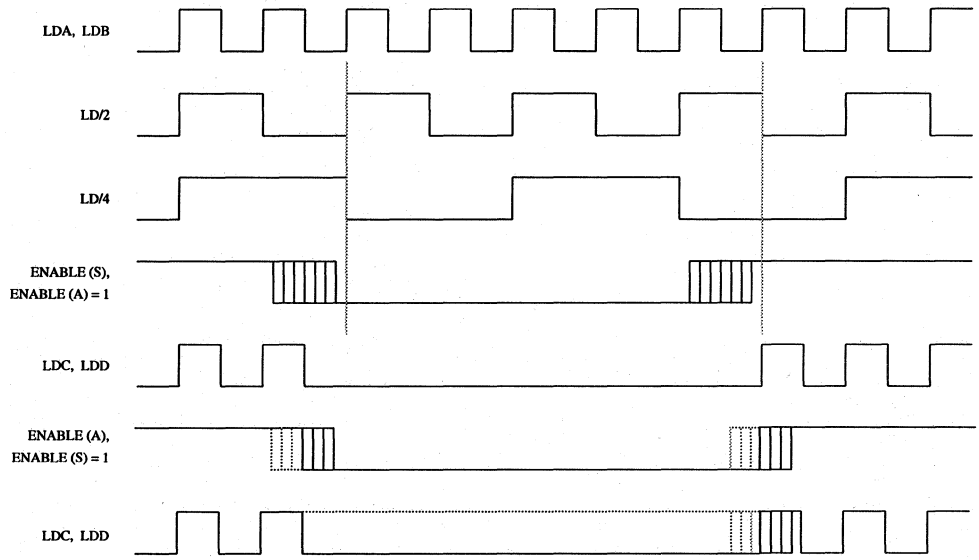


Figure 2. Load Output Timing.

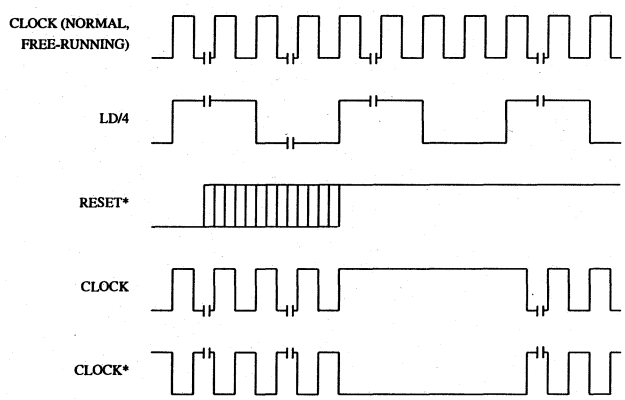


Figure 3. RESET* Timing.

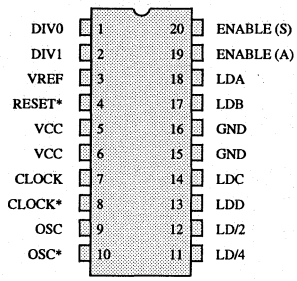
Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>VREF</td><td>Voltage reference output. This output provides a 1.2 V (typical) reference and may be used to drive the VREF input of up to four RAMDACs.</td></tr>
<tr><td>OSC, OSC*</td><td>Differential ECL oscillator inputs. These inputs are designed to interface to a 10KH ECL crystal oscillator operating from a single +5 V supply.</td></tr>
<tr><td>CLOCK,
CLOCK*</td><td>Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the OSC rate, and these outputs can drive up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply.</td></tr>
<tr><td>DIV0, DIV1</td><td>Divide control inputs (TTL compatible). These inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals, as specified below:
<table>
<tr><th>DIV1</th><th>DIV0</th><th>Division Factor</th><th>Clock Cycles Low</th><th>Clock Cycles High</th></tr>
<tr><td>0</td><td>0</td><td>÷3</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>÷4</td><td>2</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>÷5</td><td>2</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>÷8</td><td>4</td><td>4</td></tr>
</table></td></tr>
<tr><td>LDA, LDB</td><td>Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by 3, 4, 5, or 8, as determined by the DIV0 and DIV1 inputs.</td></tr>
<tr><td>LD/2</td><td>Load output (TTL compatible). LD/2 is generated by dividing LDA by 2.</td></tr>
<tr><td>LD/4</td><td>Load output (TTL compatible). LD/4 is generated by dividing LDA by 4.</td></tr>
<tr><td>LDC, LDD</td><td>Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs.</td></tr>
<tr><td>ENABLE (S)</td><td>Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA, and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros. While both ENABLE (A) and ENABLE (S) are logical ones, LDC and LDD are free-running and in phase with the LDA and LDB outputs.</td></tr>
<tr><td>ENABLE (A)</td><td>Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were in when the ENABLE (A) input went to a logical zero. While both ENABLE (A) and ENABLE (S) are logical ones, LDC and LDD are free running and in phase with the LDA and LDB outputs. Glitches should be avoided on this asynchronous input.</td></tr>
</table>

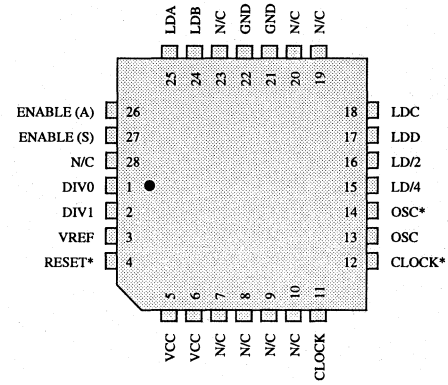
Pin Descriptions *(continued)*

Pin Name	Description
RESET*	Reset control input (TTL compatible). Following the first rising edge of LD/4 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are set to be free running. Glitches should be avoided on this edge-triggered input.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.

A 20-pin DIP Package



A 28-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt438.

Application Information

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt438 to a RAMDAC when using a differential ECL oscillator. The Bt438 should be located as close as possible to the RAMDAC. The 220 Ω resistors at the oscillator should be located as close as possible to the OSC and OSC* outputs. The 150 Ω resistor at the Bt438 should be located as close as possible to the Bt438 OSC and OSC* inputs.

The 220 Ω resistors at the Bt438 should be located as close as possible to the Bt438 CLOCK and CLOCK* outputs. The 150 Ω resistor at the RAMDAC should be as close as possible to the CLOCK and CLOCK* inputs.

Figure 5 illustrates interfacing to a single-ended ECL oscillator.

Figure 6 shows interfacing to a TTL clock for applications less than 80 MHz. The +5 V of the resistor divider should be tied directly to the device +5 V. At VCC max, noise margin is at the minimum (100 mV).

Because of the inability to ensure proper synchronization between Bt438s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1 kΩ resistor must be used to isolate the VREF output between multiple RAMDACs. This keeps noise on the Bt438 voltage reference from being coupled into the RAMDAC's VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA or GND, as specified in the RAMDAC's datasheet.

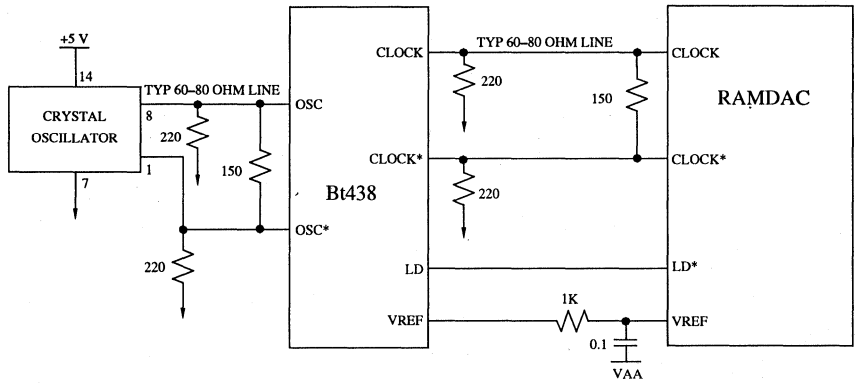


Figure 4. Interfacing to a Differential Crystal Oscillator.

Application Information *(continued)*

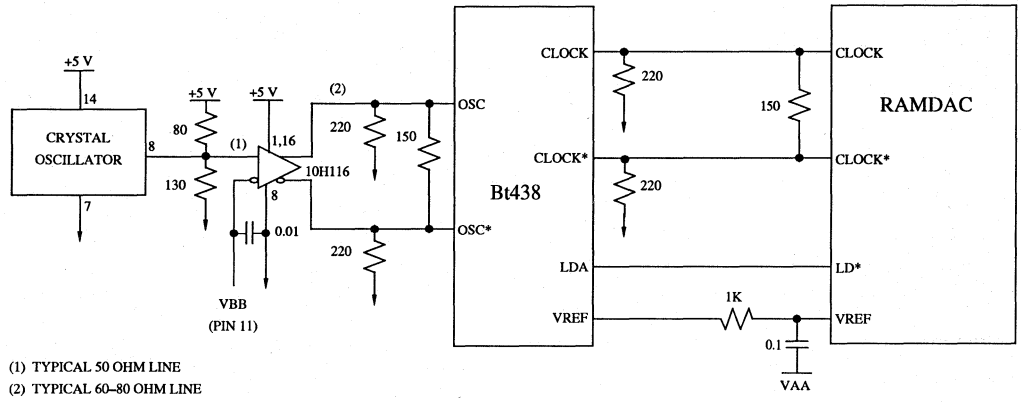


Figure 5. Interfacing to a Single-Ended Crystal Oscillator.

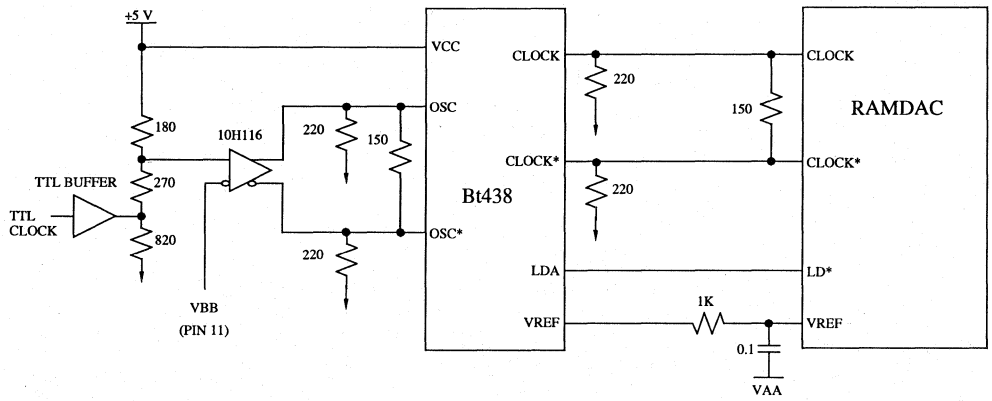


Figure 6. Interfacing to a TTL Clock.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
OSC/OSC* Duty Cycle		40			%

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Pin		GND–0.5		VCC + 0.5	V
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow		0			l.f.p.m.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification isnot implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage (general)	VIH	2.0		VCC + 0.5	V
DIV0, DIV1		2.2		VCC + 0.5	V
RESET* (at 0 °C)		2.2		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4		pF
ECL Inputs					
Input High Voltage	VIH	VCC–1.1		VCC–0.8	V
Input Low Voltage	VIL	GND–0.5		VCC–1.5	V
Input High Current (Vin = 4.0 V)	IIH			15	µA
Input Low Current (Vin = 0.4 V)	IIL			15	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CIN		4		pF
Load Outputs					
Output High Voltage (IOH =–2 mA)	VOH	2.4			V
Output Low Voltage (IOL = 20 mA)	VOL			0.65	V
Output Capacitance			10		pF
Clock Outputs					
Differential Output Voltage	ΔVOUT	0.6			V
Output Capacitance	COUT		7		pF
Voltage Reference					
Output Voltage (Bt438 Rev. C) (Note 1)	VREF	1.12	1.2	1.27	V
Output Current	IREF		100		µA
VCC Supply Current (Note 2)	ICC		65	85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: RSET of the RAMDAC should be adjusted because the output voltage of the Bt438 Rev. C is lower than the recommended VREF for the RAMDAC. IOG (mA) = $\frac{11294 \text{ VREF}}{\text{RSET}}$, IOG (typ) = 26.7 mA.

Note 2: Measured without 50 Ω to VCC–2 V on CLOCK and CLOCK*.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

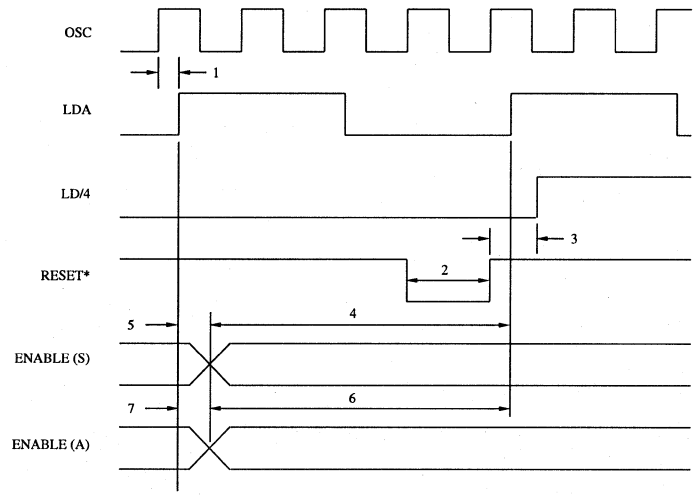
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate	Fmax			250	MHz
LDA Output Delay (Note 1)	1		4	10	ns
LDA, LDB Pulse Width Low (Note 2)		5			ns
LDA to LDB Output Skew (Note 3)		–2.0	0	2.0	ns
LDA to LDC Output Skew (Note 3)		–1.0	1.5	4.0	ns
LDA to LD/2 Output Skew (Note 3)		0	1.5	5.0	ns
LDA to LD/4 Output Skew (Note 3)		0	1.5	6.0	ns
LDC to LDD Output Skew (Note 3)		–2.0	0	2.0	ns
RESET* Active Low Time	2	15			ns
RESET* Setup Time	3	12			ns
ENABLE (S) Setup Time	4	12			ns
ENABLE (S) Hold Time	5	–2			ns
ENABLE (A) Setup Time	6	12			ns
ENABLE (A) Hold Time	7	–2			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 Ω to VCC–2 V. TTL outputs have –2 mA/20 mA load applied with 1.5 V switching point. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between 10-percent and 90-percent points. ECL input values are VCC–1.8 to VCC–0.8 V with input rise/fall times ≤ 1 ns, measured between 20-percent and 80-percent points. Timing reference points at 50-percent for inputs and outputs, except TTL outputs measured at 1.5 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Output load = 50 pF.
Note 2: LD outputs not used in ÷3 over 200 MHz.
Note 3: LD outputs equally loaded. Unequal loading may result in additional output skew.

Timing Waveforms



Input/Output Timing

Ordering Information

7

Model Number	Package	Ambient Temperature Range
Bt438KC	20-pin 0.3" CERDIP	0° to +70° C
Bt438KPJ	28-pin Plastic J-Lead	0° to +70° C

Bt439

200 MHz Clock Generator and Synchronizer Chip for CMOS RAMDACs™

Distinguishing Features

- 200 MHz Operation
- 4 Differential ECL Clock Outputs
- Synchronizes Multiple CMOS RAMDACs
- Ability to Divide by 3, 4, 5, or 8 of the Clock
- Ability to Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- Reduces Skew Between Devices to < 2 ns
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 28-pin DIP Package

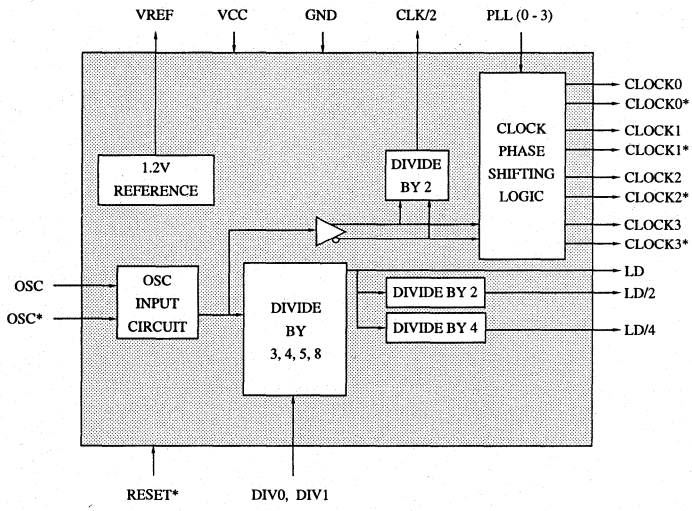
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Reduces Cost over Discretes
- Increases System Reliability
- Eases Design of True-Color Systems

Related Products

- Bt438
- Bt440

Functional Block Diagram



Product Description

The Bt439 is a clock generator chip for the high-speed Brooktree family of single-channel CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5 V supply to the RAMDACs, generating the necessary clock and control signals.

Up to four CMOS RAMDACs may be synchronized with subpixel resolution. The Bt439 accepts a PLL signal from each RAMDAC and adjusts the differential clocks to each RAMDAC to minimize the phase difference between the PLL signals.

The clock output can be divided by 3, 4, 5, or 8 to generate the load signal. The load signal can also be divided by 2 and 4 for clocking video timing logic, etc.

The Bt439 optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay. An on-chip voltage reference is provided and may be used to provide the reference voltage for up to four RAMDACs.

7

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L439001 Rev. I

Brooktree®

Circuit Description

The Bt439 is designed to interface to a 10K ECL crystal oscillator and generate the clock signals required by up to four CMOS RAMDACs. The OSC and OSC* inputs are designed to interface to a 10K ECL oscillator operating from a single +5 V power supply.

All of the CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are similar to 10KH ECL logic, operating from a single +5 V power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by 3, 4, 5, or 8 to generate the LD signal. LD is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively.

The RESET* input is designed to enable the Bt439 to set the pipeline delay of the RAMDACs to a fixed number of clock cycles. (The exact number is dependent on the RAMDAC.) Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 1 shows the operation of the RESET* input.

The Bt439 also generates a 1.2 V (typical) voltage reference, which may be used to drive the VREF input of up to four RAMDACs.

Synchronizing Multiple RAMDACs

The Bt439 is designed to synchronize multiple CMOS RAMDACs that generate a PLL output signal. Typically, only single-channel RAMDACs will generate the PLL signal. Because CMOS processing generates wide variations in output delays for CMOS devices, synchronization is necessary.

Following a reset input, the Bt439 sets the pipeline delay of all the RAMDACs. It then monitors the PLL inputs, PLL0–PLL3. On the rising edge of the last PLL input to go high, the Bt439 latches the relative time differences between the PLL inputs.

The Bt439 then stops the clocks to all the RAMDACs, with CLOCK low and CLOCK* high. The time differences between the PLL inputs are used to adjust the clock phases by selecting appropriate taps from internal delay lines (one set of delay lines for each clock signal). The Bt439 then restarts the clocks.

RESET Timing Sequence*

The following will occur when the RESET* input is asserted and remains low for at least 15 ns.

The LD, LD/2, and LD/4 outputs will be forced high (CLK/2 low) within 9 ns of the falling edge of RESET* and will remain so while RESET* is active low. Any programmed skew between the CLKx outputs will be zeroed at this point (anticipating a retiming sequence), which may result in some invalid CLKx pulses. Therefore, the RESET* input should be activated only during the blanking interval to avoid visible timing transients from the palette DACs.

When RESET* rises outside the prescribed setup/hold time before a rising OSC input, the LD output will toggle high to low after the fourth subsequent rising OSC input.

LD/2 will toggle high to low coincident with the first rising edge of LD. LD/4 will toggle high to low on the second rising edge of LD.

On the next rising edge of LD/4, all the ECL CLKx true outputs will be forced high (CLKx* low) for one cycle of the LD/4, and will fall generally (1.5*OSC period–6 ns) after the following rising LD/4 and resume toggling.

RESET* transitions occurring within the setup/hold interval will delay the corresponding response one cycle of OSC. In this way correct response to an asynchronous RESET* is ensured (see Figure 1).

The Bt439 requires a minimum of two reset signals to ensure clock operation and to correct pixel alignment operation immediately after power-up. The first reset signal is needed to start the CLK and CLK* signals. The system power-up RESET* can be used as CLK and CLK* initiators. The second reset signal must be applied to initiate pixel alignment sequence. Pixel Alignment Sequence contains proper timing requirements.

Should the multiplex factor change (as set by DIV0 and DIV1) after the initialization sequence, another reset timing sequence must be applied to the Bt439.

Circuit Description *(continued)*

Pixel Alignment Sequence

A RESET* timing sequence must precede each pixel alignment sequence and should be completed within a blanking interval to avoid corruption of the pixel alignment sequence, which is triggered by the beginning of the ensuing active line. A pixel alignment sequence proceeds as follows.

The first falling PLLx input after a RESET* timing sequence initiates a delay-sampling process for the duration of the active (i.e., nonblanked) interval, which terminates with the last rising PLLx input (i.e., beginning of subsequent blank interval). The CLKx outputs maintain minimal delay through the duration of this active line; hence, any systematic delays between the PLL generators will not be corrected during this active line. For those applications that call for asserting RESET* on a line-by-line basis, blank may be toggled in the back porch interval after normal blanking to maintain CLKx alignment on each line. (At least one LD* clock cycle should occur before the first rising PLL edge.)

The first rising edge of CLK/2 following the last rising PLLx input initiates a pixel alignment sequence, which takes up to two periods of CLK/2 to complete. During this sequence, the CLKx outputs are held low (false), and the toggling of TTL outputs is inhibited. No false or short CLKx pulses result because of controlled time delays on chip. The proper skew compensation for each CLKx channel is latched in the internal delay lines. Concluding this sequence, the CLKy corresponding to the last (slowest) PLLy input will resume toggling with about 2 ns delay relative to OSC. The CLKz associated with the first (fastest) PLLz will resume with up to (Δ + (err)) ns extra delay relative to CLKy. The TTL outputs resume toggling with a consistent relationship relative to the CLK, which is consistent with the palette DAC pipeline delay preservation requirement. This will stretch the low LD clock duration by up to 5 pixels, which may momentarily affect any dependent synchronization timing counters.

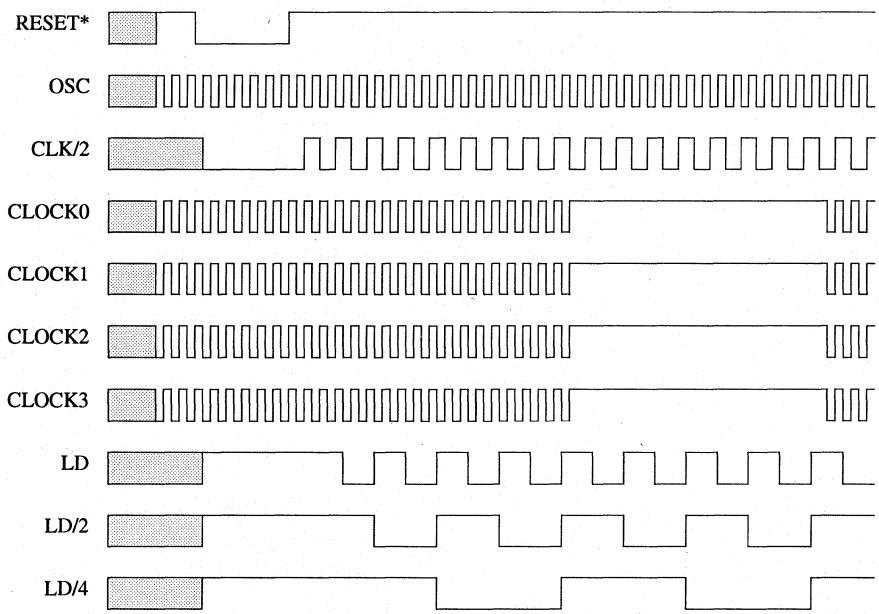


Figure 1. RESET* Timing Sequence.

Circuit Description *(continued)*

The slowest PLLy–CLKy channel defaults to the minimum delay setting. If the slowest PLLy input lags the other active PLLx inputs by an interval exceeding the alignment span of the Bt439, then the faster PLLx channels will default to the maximum delay setting. Hence, occurrence of any active PLLx input outside the alignment span will render skew compensation on the other channels inoperative. Unused PLLx inputs are internally pulled high and, hence, are not sampled, leaving their corresponding CLKx channel in the maximum delay condition (see Figure 2).

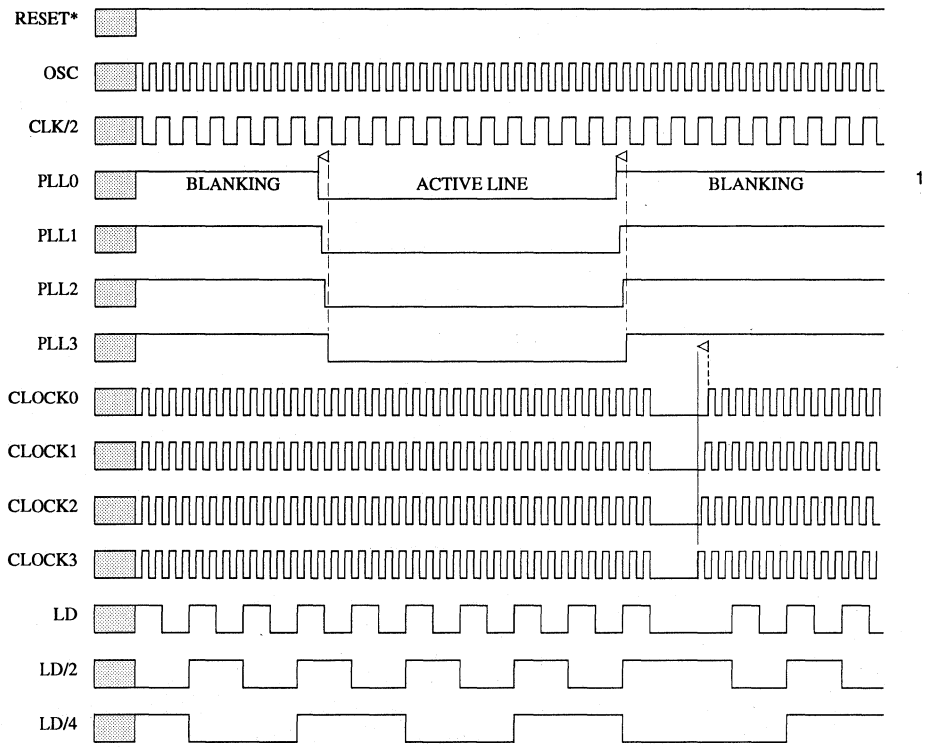


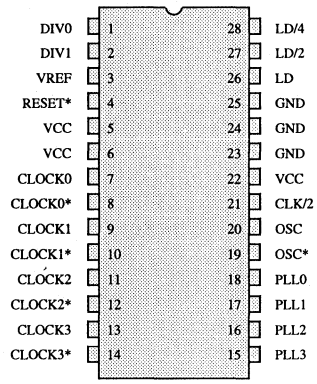
Figure 2. Pixel Alignment Sequence.

Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>VREF</td><td>Voltage reference output. This output provides a 1.2 V (typical) reference and may be used to drive the VREF input of up to four RAMDACs.</td></tr>
<tr><td>OSC, OSC*</td><td>Differential ECL oscillator inputs (+5 V ECL compatible). These inputs are designed to interface to a 10K ECL crystal oscillator operating from a single +5 V supply.</td></tr>
<tr><td>CLOCK(0–3),
CLOCK(0–3)*</td><td>Differential clock outputs (+5 V ECL compatible). These outputs connect directly to the CLOCK and CLOCK* inputs of up to four RAMDACs. The output levels are equivalent to 10K ECL logic operating from a single +5 V supply.</td></tr>
<tr><td>DIV0, DIV1</td><td>Divide control inputs (TTL compatible). These inputs specify the division factor for the generation of the LD signal, as specified below:
<table>
<tr><th>DIV1</th><th>DIV0</th><th>Division Factor</th><th>Clock Cycles Low</th><th>Clock Cycles High</th></tr>
<tr><td>0</td><td>0</td><td>÷3</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>÷4</td><td>2</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>÷5</td><td>2</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>÷8</td><td>4</td><td>4</td></tr>
</table></td></tr>
<tr><td>LD</td><td>Load output (TTL compatible). LD is generated by dividing CLOCK by 3, 4, 5, or 8 as determined by the DIV0 and DIV1 inputs.</td></tr>
<tr><td>LD/2</td><td>Load output (TTL compatible). LD/2 is generated by dividing LD by 2.</td></tr>
<tr><td>LD/4</td><td>Load output (TTL compatible). LD/4 is generated by dividing LD by 4.</td></tr>
</table>

Pin Descriptions *(continued)*

Pin Name	Description
RESET*	Reset control input (TTL compatible). RESET* Timing Sequence in the Circuit Description section contains more information. Glitches should be avoided on this edge-triggered input.
PLL0–PLL3	Phase inputs. These inputs are used to determine the relative phases of the RAMDAC outputs. Each RAMDAC to be synchronized must generate a unique PLL signal. Unused PLL inputs should be connected to VCC through a 1K pullup resistor.
CLK/2	Clock/2 output (+5 V ECL compatible). The OSC input is divided by 2 and output onto this pin. It may be used as a general-purpose clock for external circuitry.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.



Application Information

PLL Signal Interface

Because of the limited drive capability of the RAMDAC's PLL output, the buffer circuitry should be located as close as possible to the RAMDAC. If the distance between the transistor and the PLL input is 12 inches or more, 50 Ω microstrip lines should be used.

The Bt439 contains sensitive PLL circuitry that drives the clock output signals to allow proper deskew operations. Because of the large number of VRAM datalines switching in a true-color system, the noise generated by the VRAMs can affect the power supply of the Bt439. If difficulty is experienced in synchronization because of switching noise, the following VCC supply pin decoupling strategy is recommended (see Figure 3).

1. A 0.01 ceramic capacitor should be connected between VCC pins 5 and 6, and GND pins 23–25.
2. A ceramic chip capacitor (0.01–0.1) should be connected between GND pins 23–25, and VCC pin 22.

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt439 to a RAMDAC when using a differential ECL oscillator. The Bt439 should be located as close as possible to the RAMDAC. The 220 Ω resistors at the oscillator should be located as close as possible to the OSC and OSC* outputs. The 150 Ω resistor at the Bt439 should be located as close as possible to the Bt439 OSC and OSC* inputs.

The 220 Ω resistors at the Bt439 should be located as close as possible to the Bt439 CLOCK and CLOCK* outputs. The 150 Ω resistor at the RAMDAC should be as close as possible to the CLOCK and CLOCK* inputs.

Figure 5 illustrates interfacing to a single-ended ECL oscillator.

Figure 6 shows interfacing to a TTL clock for applications less than 80 MHz. The +5 V of the resistor divider should be tied directly to the device +5 V. At VCC max, noise margin is at the minimum (100 mV).

Because of the inability to ensure proper synchronization between Bt439s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1 kΩ resistor must be used to isolate the VREF output between multiple RAMDACs. This keeps noise on the Bt439 voltage reference from being coupled into the RAMDAC's VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA or GND, as specified in the RAMDAC's datasheet.

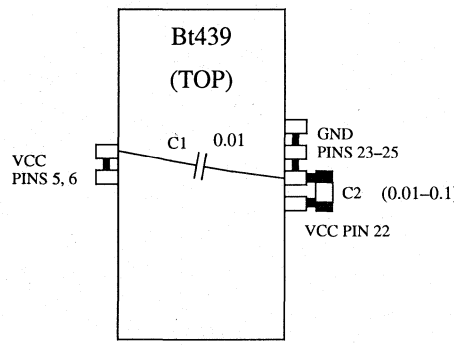


Figure 3. Switching Noise Decoupling Strategy.

Application Information *(continued)*

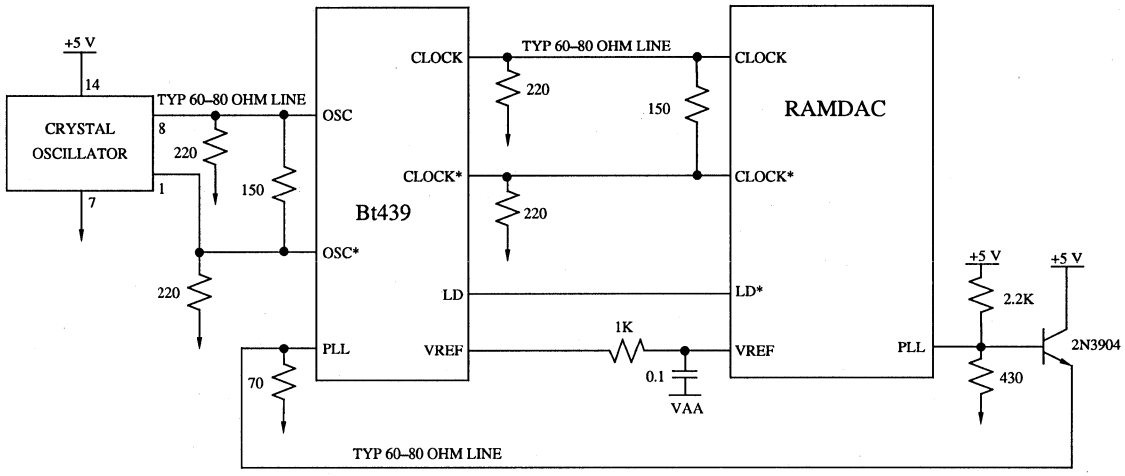


Figure 4. Interfacing to a Differential ECL Oscillator.

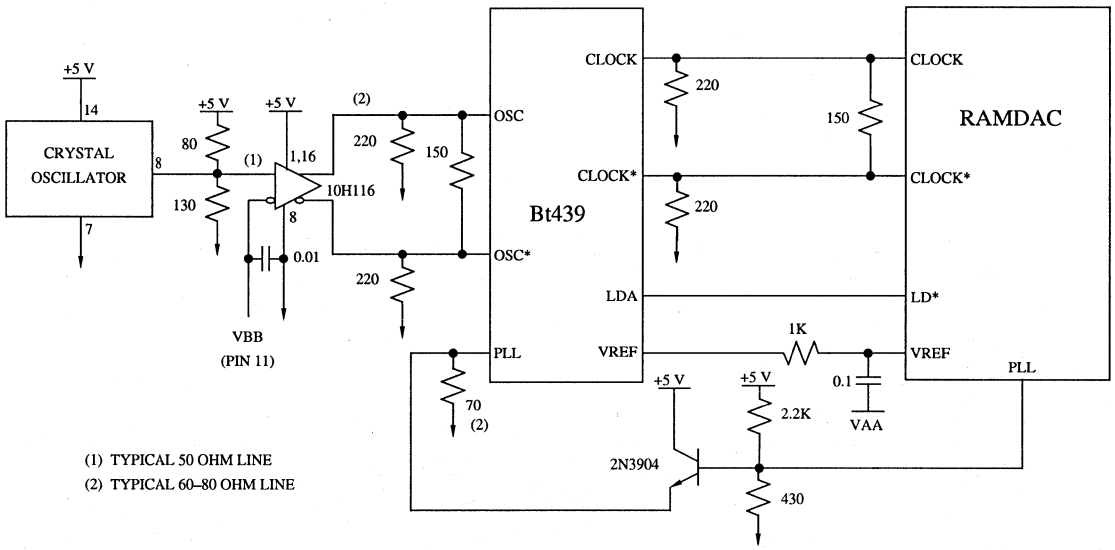


Figure 5. Interfacing to a Single-ended ECL Oscillator.

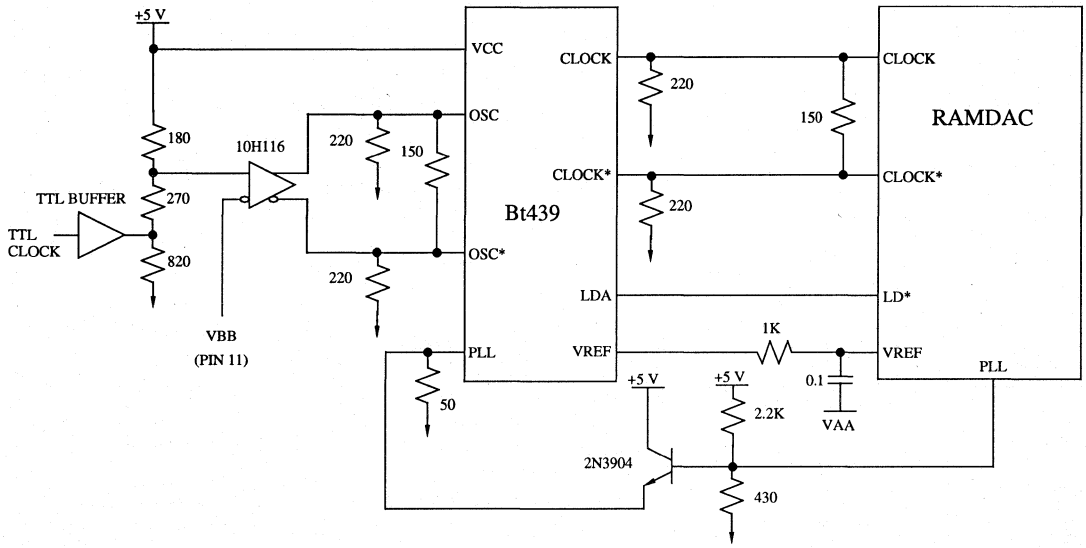


Figure 6. Interfacing to a TTL Clock. (For Applications Less Than 80 MHz.)

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature –Still Air	TA	0		+70	°C
OSC/OSC* Duty Cycle		40			%
Air Flow		50			l.f.p.m.

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 50 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Pin		GND–0.5		VCC + 0.5	V
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage (general)	VIH	2.0		VCC + 0.5	V
RESET*		2.2		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL	–0.7			mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
ECL Inputs					
Input High Voltage	VIH	VCC–1.1		VCC–0.8	V
Input Low Voltage	VIL	VCC–2		VCC–1.5	V
Input High Current (Vin = 4.0 V)	IIH		4	15	µA
Input Low Current (Vin = 0.4 V)	IIL	–15	0		µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CIN		10		pF
Load Outputs					
Output High Voltage (IOH = –2 mA)	VOH	2.4			V
Output Low Voltage (IOL = 20 mA)	VOL			0.65	V
Output Capacitance			10		pF
Clock Outputs					
Differential Output Voltage	ΔVOUT	0.6			V
Output Capacitance	COUT		10		pF
Voltage Reference					
Output Voltage @ IREF = –100 µA	VREF	1.17	1.235	1.31	V
PLL Inputs					
Input High Voltage	VIH	1.5		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.4	V
Input High Current (Vin = 1.2 V)	IIH		0	10	µA
Input Low Current (Vin = 0.5 V)	IIL	–700	–180		µA
Input Capacitance			10		pF
VCC Supply Current (Note 1)	ICC		275	300	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK, CLOCK*, and CLK/2 outputs have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Measured without 50 Ω to VCC–2 V on CLOCK, CLOCK*, and CLK/2. At VCC = 5.25 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 50 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

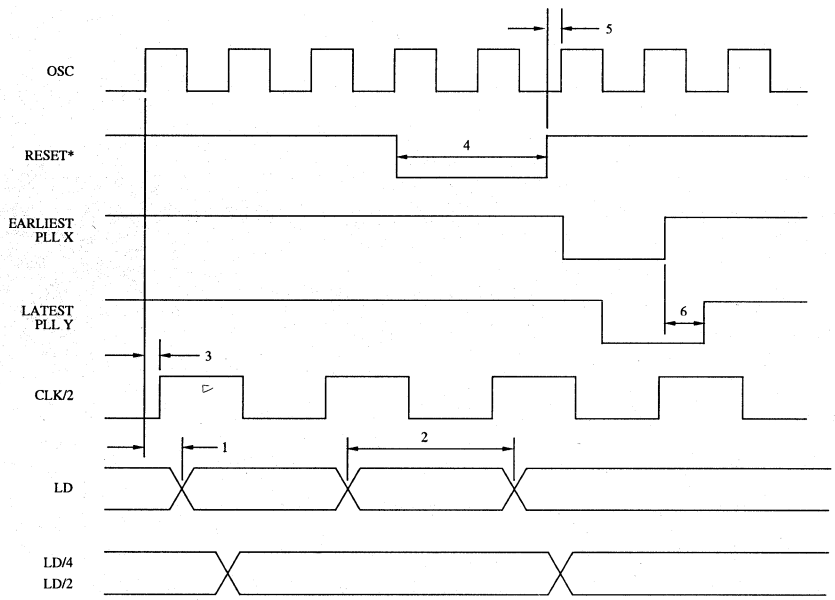
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate (Note 1)	Fmax			200	MHz
LD Output Delay (Note 2)	1	6	10	12	ns
LD Pulse Width	2	9			ns
LD to LD/2 Output Skew (Note 3)		0	1.5	3	ns
LD to LD/4 Output Skew (Note 3)		0	1.5	3	ns
CLK/2 Output Delay	3		2	4	ns
RESET* Active Low Time	4	15			ns
RESET* Setup Time	5	10			ns
Alignment Span	6	5			ns
Residual Alignment Error (Note 4)			1.5	2	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK, CLOCK*, and CLK/2 outputs have 50 Ω to VCC–2 V. TTL outputs have –2 mA/20 mA load applied, with 1.5 V switching point. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between 10-percent and 90-percent points. ECL input values are (VCC–0.9) to (VCC–1.6) V with input rise/fall times ≤ 1 ns, measured between 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs, except TTL outputs measured at 1.5 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Divide by 3 mode LD outputs valid only to 100 MHz without significant distortion.
Note 2: Output load = 50 pF. Derate 1 ns for each additional 50 pF loading.
Note 3: Load outputs equally loaded. Unequal loading may result in additional output skew.
Note 4: Maximum deviation of any two dependent PLL inputs after alignment sequence (PLL inputs within span before alignment).

Timing Waveforms



Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt439KC	28-pin 0.6" CERDIP	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt440

275 MHz PLL Clock Generator for CMOS RAMDACs™

Distinguishing Features

- 275 MHz Operation
- Phase Lock Loop (PLL) Capability
- Pixel Clock 8x, 16x, 20x, 32x Crystal
- Differential ECL Clock Generation
- Ability to Divide by 4 of the Clock
- Ability to Reset Pipeline Delay of the RAMDAC
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 28-pin PLCC Package
- Typical Power Dissipation: 800 mW

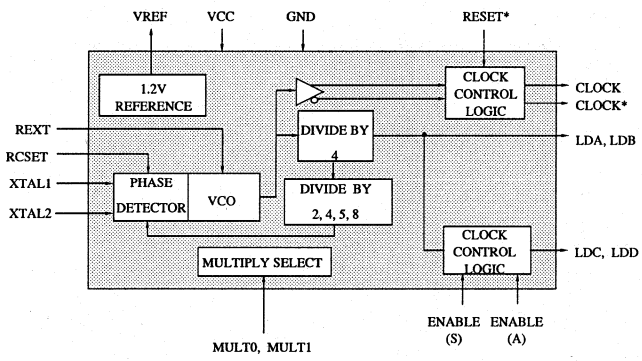
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Reduce Cost over Discretes
- Increases System Reliability
- Easy to Implement

Related Products

- Bt438
- Bt439

Functional Block Diagram



Product Description

The Bt440 is a clock generator for the high-speed Brooktree CMOS RAMDACs. It interfaces to a low-frequency quartz crystal and multiplies the crystal frequency by 8x, 16x, 20x, and 32x to generate the pixel clock signals that drive the RAMDAC.

The Bt440 requires no coils or variable capacitors for operation. Frequency range is set through an external resistor. The Bt440 loop filter uses standard RC components.

The pixel clock output is divided by 4 to generate the load signal.

A second load signal may be synchronously or asynchronously controlled to start and stop the clocking of the video DRAMs.

The Bt440 can also configure the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2 V voltage reference is also provided and may be used to provide the reference voltage for one to four RAMDACs.

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Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX (619) 452-1249
L440001 Rev. C

Brooktree®

Circuit Description

The Bt440 is designed to interface to low-frequency crystal and generate the clock signals required by the RAMDACs. XTAL1 and XTAL2 interface to a quartz crystal, yielding a cost-effective clock generation system.

The CLOCK and CLOCK* outputs interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5 V power supply.

MULT0 and MULT1 determine the multiplication factor for the pixel clock. The input oscillator frequency is multiplied by 8, 16, 20, or 32, depending on the MULT0 and MULT1 settings (see Table 1).

When the MULT0 and MULT1 are used to change to a different multiplication factor, RESET is not required. A phase lock loop will lock into the new frequency after a minimum time.

The LDA and LDB signals are generated by the pixel clock divided by 4. The LDA signal will interface directly to the LD* signal of the RAMDAC. The LDB, LDC, and LDD interface to the VRAMs. For all frequencies, LDA, LDB, LDC, and LDD maintain the same CLOCK/4 relationship.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros.

ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the same state.

While both ENABLE (S) and ENABLE (A) are a logical one, LDC and LDD will be free running and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally nonclocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt440, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt440 to set the pipeline delay of the RAMDACs to a specified number of clock cycles (with the exact number dependent on the RAMDAC). Following the first falling edge of XTAL1 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next falling edge of XTAL1, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt440 also generates a 1.2 V (typical) voltage reference, which may be used to drive the VREF input of one to four RAMDACs.

MULT1	MULT0	Pixel Clock
0	0	x8
0	1	x16
1	0	x20
1	1	x32

Table 1. Pixel Clock Multiplication Frequency.

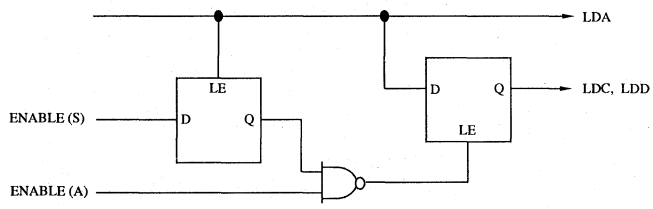

Figure 1. ENABLE Control Implementation.

Circuit Description *(continued)*

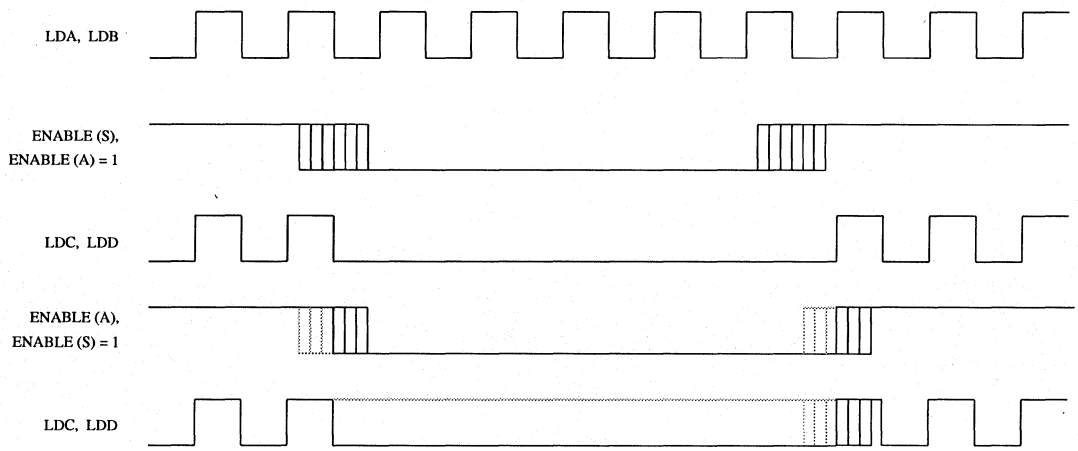

Figure 2. Load Output Timing.

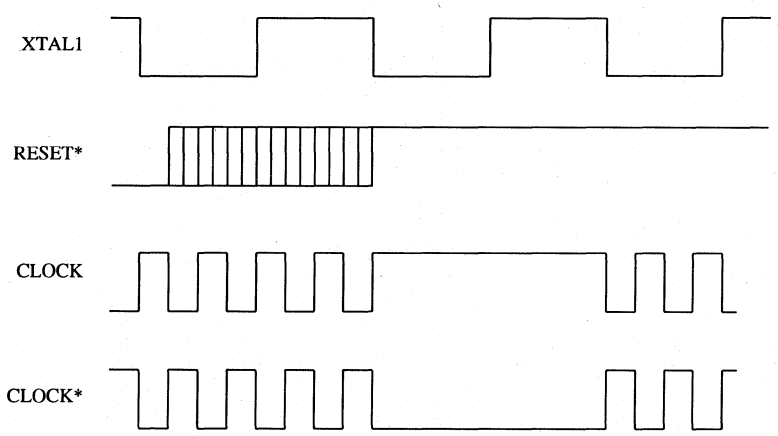

Figure 3. RESET Timing.*

Pin Descriptions

Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2 V (typical) reference and may be used to drive the VREF input of one to four RAMDACs.
XTAL1	Quartz crystal input. This input provides the base frequency for multiplication by the PLL circuitry.
XTAL2	Quartz crystal output.
CLOCK, CLOCK*	Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the crystal oscillator input rate times the multiplication factor. The multiplication factor is determined by MULT0 and MULT1. CLOCK and CLOCK* can drive up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply.
MULT0, MULT1	Multiply control inputs (TTL compatible). These inputs determine the multiplication factors for the pixel clock.
LDA, LDB	Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by 4. Each output may drive up to 20 pF without external buffering.
LDC, LDD	Load outputs (TTL compatible). When both ENABLE inputs are logical ones, these outputs have the same timing as the LDA and LDB outputs. Each output may drive up to 20 pF without external buffering.
REXT	External resistor. This resistor sets the frequency range of the Voltage Control Oscillator (VCO).
RCSET	RC network. This network filters the control voltage to the VCO. The network consists of two capacitors and one resistor.

Pin Descriptions *(continued)*

Pin Name	Description
ENABLE (S)	Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free running and in phase with the LDA and LDB outputs.
ENABLE (A)	Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the same state. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free running and in phase with the LDA and LDB outputs.
RESET*	Reset control input (TTL compatible). Following the first falling edge of XTAL1 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next falling edge of XTAL1, the CLOCK and CLOCK* outputs are set to be free running. Glitches should be avoided on this edge-triggered input.
AVCC	Analog device power. All AVCC pins must be connected.
DVCC(0), DVCC(1)	Digital device power. All DVCC pins must be connected.
AGND	Analog device ground. All AGND pins must be connected.
DGND(0), DGND(1)	Digital device ground. All DGND pins must be connected.

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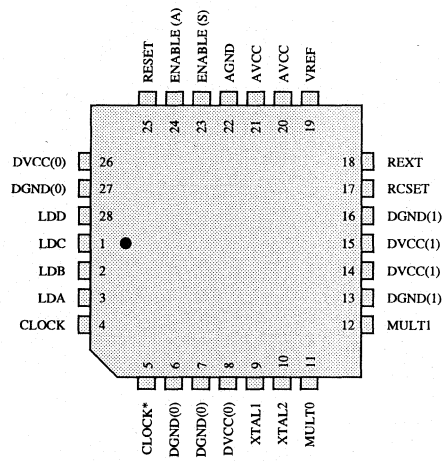
28-pin Plastic J-Lead (PLCC) Package with Internal Heatspreader



PC Board Layout Considerations

Power Planes

All of the VCC pins should be decoupled on the top PCB layer next to the device. A parallel 0.1 and 0.01 uF chip capacitor is recommended (see Figure 4).

To ensure subnanosecond CLOCK jitter, the Bt440 should be isolated through ferrite beads on the power and ground connections.

External Loop Components

All of the external loop components (REXT and RCSET) should be placed on the top PCB layer close the device.

High stability and ultra-low-leakage components should be used. (Chip capacitors and chip resistors are recommended.)

Pixel Clock Outputs

The CLOCK and CLOCK* outputs should be terminated on the top PCB layer at the Bt440 with 220 Ω chip resistors and then cross-terminated with 150 Ω as close as possible to the RAMDAC (see Figure 5).

The clock traces should be of equal length and continuous on one trace layer. Through-holes, 90-degree angles, and stubs should be avoided to reduce any signal reflections.

General

Unused TTL outputs should be left floating.

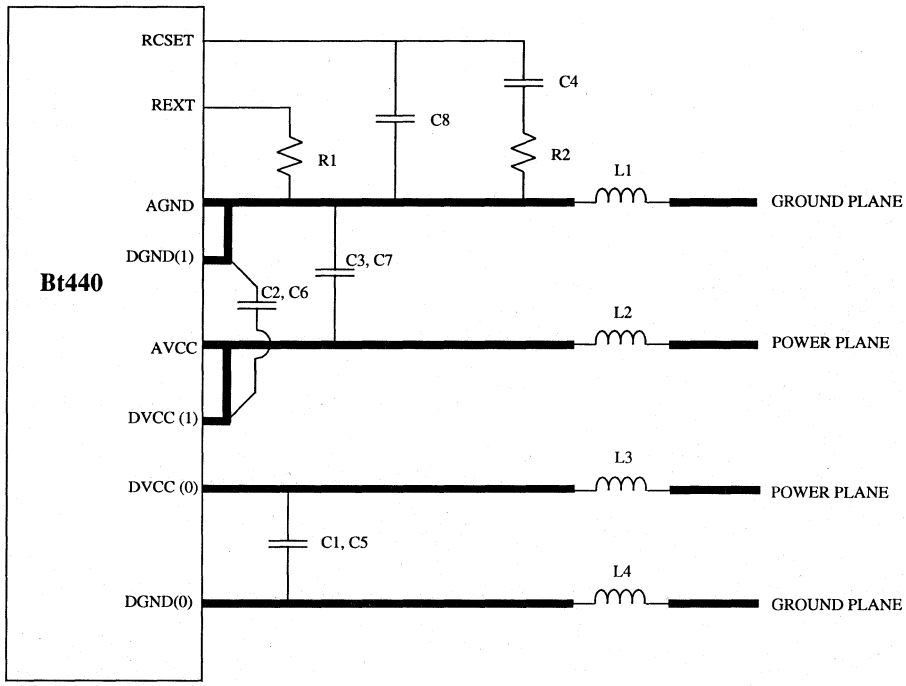
The Bt440 should not be located on the board where large transient currents, or large electric or magnetic fields are expected.

The Bt440 should not be socketed.

Wire-wrapped boards will not work.

If the LDC and LDD TTL outputs are not used, they should be disabled by tying E(s) to GND. This will reduce the CLOCK jitter and increase the stability of the Bt440.

PC Board Layout Considerations *(continued)*



Note: The decoupling capacitors should be connected as close as possible to the power pins.

7

Location	Description	Vendor Part Number
C1–C3	0.1 uF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C5–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
L1–L4	ferrite bead	Fair-Rite 2743001111
R1	2-kΩ 5% resistor	
R2	330-Ω 5% resistor	
C4	3000 pF 5% capacitor	
C8	300 pF 5% capacitor	

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt440.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

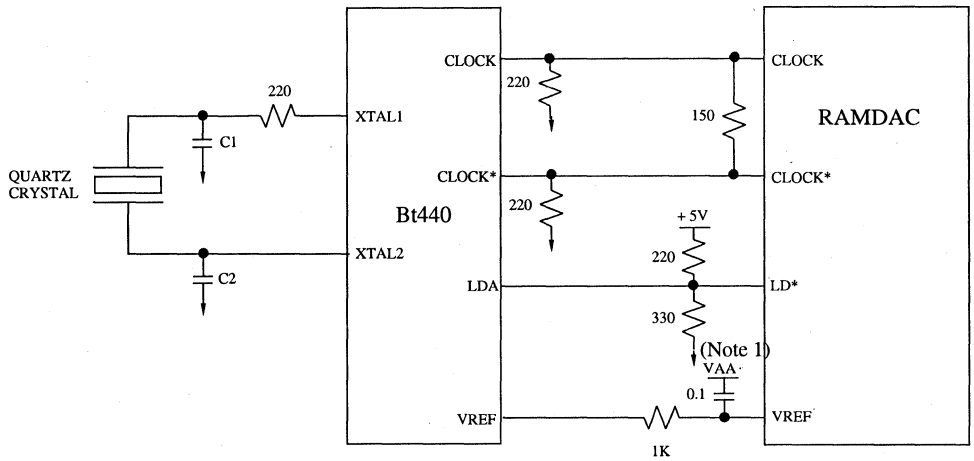
Interfacing to the RAMDAC

Figure 5 illustrates the interfacing of the Bt440 to the RAMDAC when a quartz crystal oscillator is used. Figure 6 illustrates the interfacing of the Bt440 to a TTL clock oscillator. Figure 7 illustrates the interface of the Bt440 to a CMOS clock oscillator. The Bt440 should be located as close as possible to the RAMDAC.

Termination resistors are required on the CLOCK and CLOCK* lines, located as close as possible to the Bt440.

The Bt440 may drive the CLOCK and CLOCK* inputs of one to four RAMDACs if they are located as close as possible to each other. Because proper synchronization between Bt440s cannot be ensured, multiple devices should not be used when multiple RAMDACs drive the same monitor.

A 1 k Ω (typical) resistor must be used to isolate the VREF output of the Bt440 from the VREF input of the RAMDAC. This isolates Bt440 voltage reference noise; it cannot be coupled onto the RAMDAC VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor, as specified in its datasheet.



Note 1: Decoupling capacitor may require connection to ground, depending on VAA noise level.

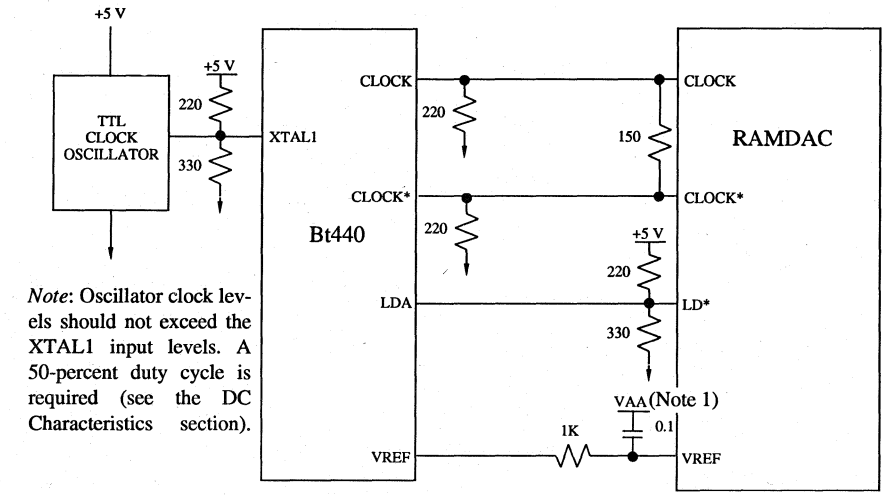
C1 min = 20 pf
C2 min = 100 pf

C2 > C1 by 30 pf

High stability and ultra-low-leakage components should be used. (Chip capacitors and chip resistors are recommended.)

Figure 5. Interfacing to a Quartz Crystal.

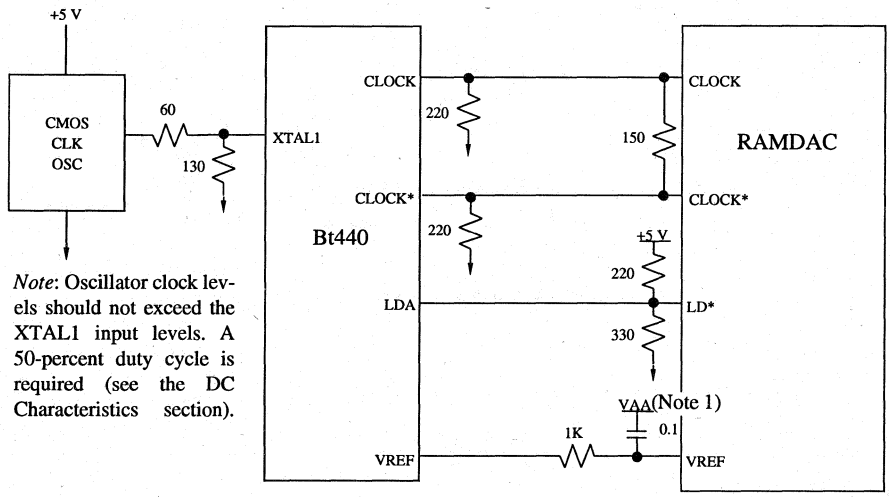
Application Information *(continued)*



Note: Oscillator clock levels should not exceed the XTAL1 input levels. A 50-percent duty cycle is required (see the DC Characteristics section).

Note 1: Decoupling capacitor may require connection to ground, depending on the VAA noise level.

Figure 6. Interfacing to a TTL Clock Oscillator.



Note: Oscillator clock levels should not exceed the XTAL1 input levels. A 50-percent duty cycle is required (see the DC Characteristics section).

Note 1: Decoupling capacitor may require connection to ground, depending on the VAA noise level.

Figure 7. Interfacing to a CMOS Clock Oscillator.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+ 70	°C
XTAL1 Input Levels	VIH VIL		3.0 0.5		V V

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Pin		GND–0.5		VCC + 0.5	V
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+ 125	°C
Storage Temperature	TS	–65		+ 150	°C
Junction Temperature	TJ			+ 175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4		pF
XTAL1 Input Voltage	VIH	2		3.8	V
	VIL	GND–0.5		0.8	V
Load Outputs					
Output High Voltage (IOH = –2 mA)	VOH	2.4			V
Output Low Voltage (IOL = 20 mA)	VOL			0.5	V
Clock Outputs					
Differential Output Voltage	ΔVOUT	.6			V
Voltage Reference					
Output Voltage (Note 1)	VREF	1.13	1.21	1.28	V
Output Current	IREF		100		µA
VCC Supply Current	ICC		150	185	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC – 2 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: RSET of the RAMDAC should be adjusted because the output voltage of the Bt440 is lower than the recommended VREF for the RAMDAC. IOG (mA) = $\frac{11294 \times VREF}{RSET}$ and IOG (typ) = 26.7 mA.

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AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Pixel Clock Rate Crystal Frequency	Fmax XTALmax	80 5		275 15	MHz MHz
CLOCK to LDA Skew (Note 1) LDA to LDB Output Skew (Note 1) LDA to LDC Output Skew (Note 1) LDC to LDD Output Skew (Note 1)	1	0 –2 –2 –2	2 0 0.5 0	4 2 2 2	ns ns ns ns
E(S) Setup (Figure 8) E(S) Hold E(A) Setup (Figures 9 and 10) E(A) Enable Time	2 3 4 5	5 5 4 7			ns ns ns ns
RESET* Active Low Time RESET* Setup Time	6 7	6 4			ns ns
Pixel Clock Jitter (Notes 2 and 3)			0.4		ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V with input rise/fall times ≤3 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs.

Note 1: LD outputs equally loaded with 20 pF. Unequal loading may result in additional output skew.
Note 2: Improper isolation will result in additional jitter. (See the PCB Layout Considerations section.)
Note 3: Guaranteed, but not 100-percent production tested.

Timing Waveforms

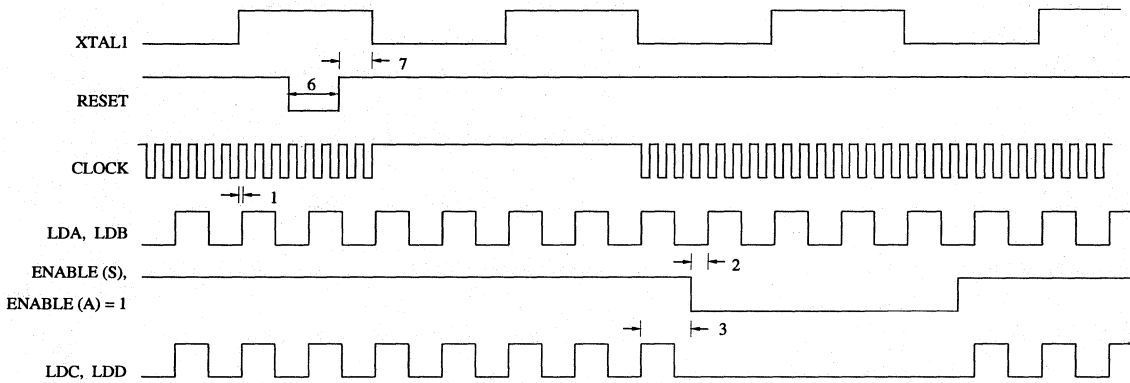

Figure 8. Synchronous Enable Operation.

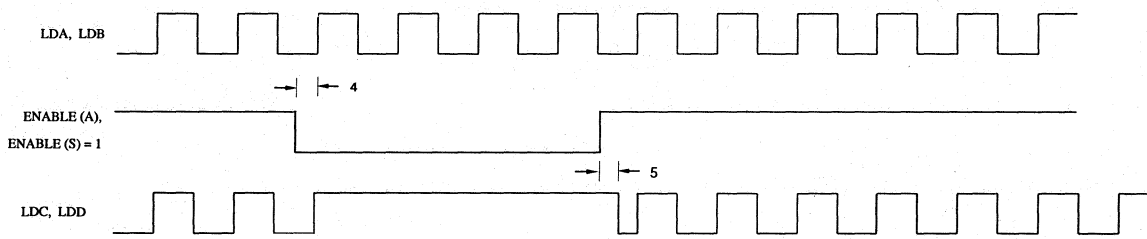

Figure 9. Asynchronous Enable Operation. Enable (A) Operation Pulled High Coincident When LDA and LDB are Low.

7

Timing Waveforms *(continued)*

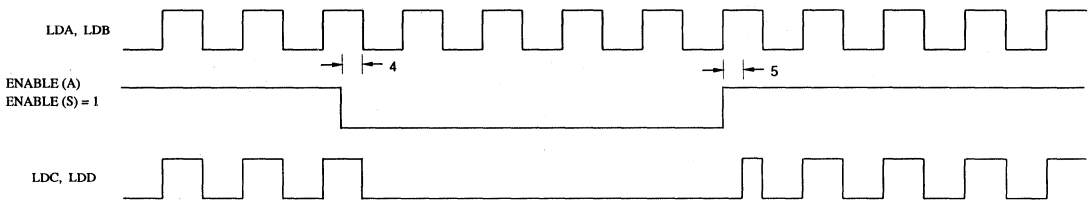

Figure 10. Asynchronous Enable Operation. Enable (A) Operation Pulled High Coincident When LDA and LDB are High.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt440KHJ	28-pin PLCC with internal heat spreader	0° to +70° C

Bt501

Bt502

ECL/TTL Octal Transceiver and Translator

Distinguishing Features

- 10KH or 100K ECL Compatibility
- Optional Single +5 V Operation
- Separate TTL and ECL Supply Pins
- Three-Statable TTL Pins
- TTL-Compatible Control Inputs
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 800 mW

Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplified PCB Layout
- Reduced PCB Interconnect
- Low Bus Loading

Product Description

The Bt501 and Bt502 are octal ECL/TTL bidirectional transceivers and translators. The Bt501 is 10KH ECL compatible, and the Bt502 is 100K ECL compatible.

The direction and output-enable control inputs are TTL compatible to simplify interfacing to a standard MPU.

Both devices provide a bidirectional interface between TTL signals and ECL signals. The ECL input/output signals may be generated from normal ECL, single +5 V, or split ECL supplies.

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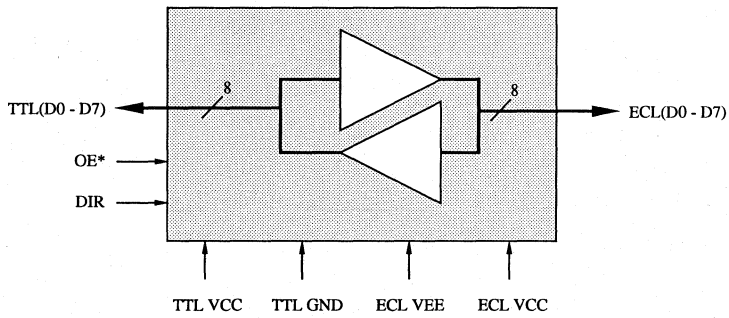
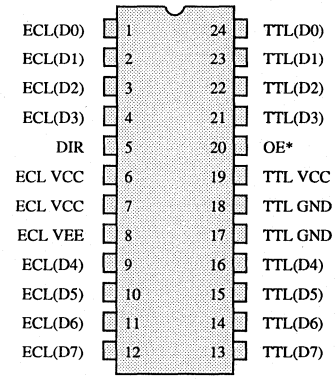
Functional Block Diagram





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L501001 Rev. H

Brooktree®

	Nominal Voltages Applied		
Supply Pin	**Single-Supply System**	**Dual-Supply System**	**Split ECL Supply**
TTL VCC	+5.0 V	+5.0 V	+5.0 V
TTL GND	0 V	0 V	0 V
ECL VCC	+5.0 V	0 V	+ 2.0 V
ECL VEE	0 V	–5.2 V	–3.2 V

Bt501 Supply Operation.

	Nominal Voltages Applied		
Supply Pin	**Single-Supply System**	**Dual-Supply System**	**Split ECL Supply**
TTL VCC	+5.0 V	+5.0 V	+5.0 V
TTL GND	0 V	0 V	0 V
ECL VCC	+5.0 V	0 V	+ 2.0 V
ECL VEE	0 V	–4.5 V	–2.5 V

The TTL (D0–D7), DIR, and OE* pins are TTL compatible regardless of the ECL power supply parameters. Changing the ECL power supply parameters affects the threshold levels of only the ECL(D0–D7) pins.

Bt502 Supply Operation.

DIR	OE*	Function
0	0	TTL (D0–D7) --> ECL (D0–D7)
1	0	ECL (D0–D7) --> TTL (D0–D7)
x	1	TTL (D0–D7) three-stated, ECL (D0–D7) = 0

Control Truth Table.

Bt501—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	V
ECL Device Ground	ECL VCC	0	0	0	V
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	V
ECL Power Supply	ECL VEE	–4.9	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+70	°C

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Bt501—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	V
TTL VCC (measured to TTL GND)				+7.0	V
Voltage on Any ECL Pin		ECL VCC		ECL VEE	V
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	V
ECL(D0–D7) Output Current				–50	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bt501—ECL DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Input High Voltage (Note 1)	VIH	0 +25 +70	–1170 –1130 –1070		–840 –810 –735	mV mV mV
Input Low Voltage (Note 1)	VIL	0 +25 +70	–1950 –1950 –1950		–1480 –1480 –1450	mV mV mV
Output High Voltage (Note 1)	VOH	0 +25 +70	–1020 –980 –920		–840 –810 –735	mV mV mV
Output Low Voltage (Note 1)	VOL	0 +25 +70	–1950 –1950 –1950		–1630 –1630 –1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	FULL			10	µA
ECL VEE Supply Current	IEE	FULL			85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Note 1: Relative to ECL VCC.

Bt501—TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 1)	VIH	2.0		TTL VCC +0.5	V
Input Low Voltage (Note 1)	VIL	TTL GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Output High Voltage (Note 1) (IOH = –2.0 mA)	VOH	2.5			V
Output Low Voltage (Note 1) (IOL = 16 mA)	VOL			0.5	V
Three-State Output Current	IOZ				
Vout = VOHmin				10	µA
Vout = VOLmax				–10	µA
TTL VCC Supply Current	ICC			95	mA
TTL(D0–D7) Short Circuit Output Current	IOS	–40		–150	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Relative to TTL GND.

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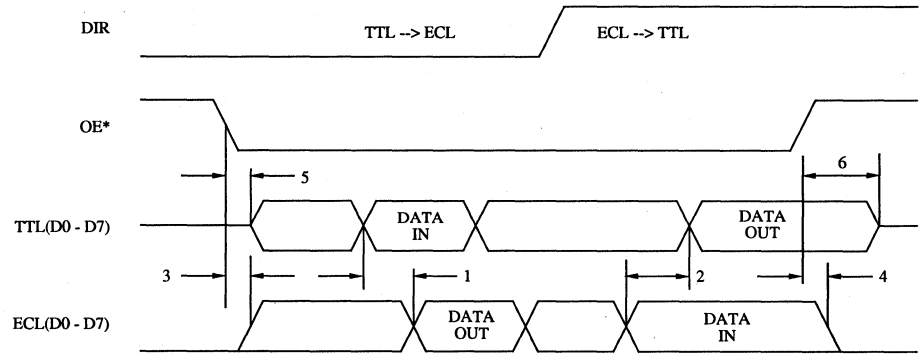
Bt501—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL --> ECL Propagation Delay ECL --> TTL Propagation Delay	1 2	0.5 2		7 11	ns ns
ECL (D0–D7) Enable Time ECL (D0–D7) Disable Time (Note 1)	3 4	2 3		11 11	ns ns
TTL (D0–D7) Enable Time TTL (D0–D7) Disable Time (Note 1)	5 6	0.5 0.5		6.5 6.5	ns ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are –2.0 to –0.80 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Subject to capacitive loading.



Input/Output Timing.

Bt502—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	V
ECL Device Ground	ECL VCC	0	0	0	V
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	V
ECL Power Supply	ECL VEE	–4.2	–4.5	–4.8	V
Ambient Operating Temperature	TA	0		+85	°C

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Bt502—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	V
TTL VCC (measured to TTL GND)				+7.0	V
Voltage on Any ECL Pin		ECL VCC		ECL VEE	V
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	V
ECL (D0–D7) Output Current				–50	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bt502—ECL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 1) Input Low Voltage (Note 1)	VIH VIL	–1165 –1810		–880 –1475	mV mV
Output High Voltage (Note 1) Output Low Voltage (Note 1)	VOH VOL	–1025 –1810	–955 –1705	–880 –1620	mV mV
Input High Current (Vin = VIH max)	IIH			10	µA
ECL VEE Supply Current	IEE			85	mA

See notes below.

Bt502—TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 2)	VIH	2.0		TTL VCC +0.5	V
Input Low Voltage (Note 2)	VIL	TTL GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Output High Voltage (Note 2) (IOH = –2.0 mA)	VOH	2.5			V
Output Low Voltage (Note 2) (IOL = 16 mA)	VOL			0.5	V
Three-State Output Current Vout = VOHmin Vout = VOLmax	IOZ			 10 –10	 µA µA
TTL VCC Supply Current	ICC			95	mA
TTL (D0–D7) Short Circuit Output Current	IOS	–40		–150	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

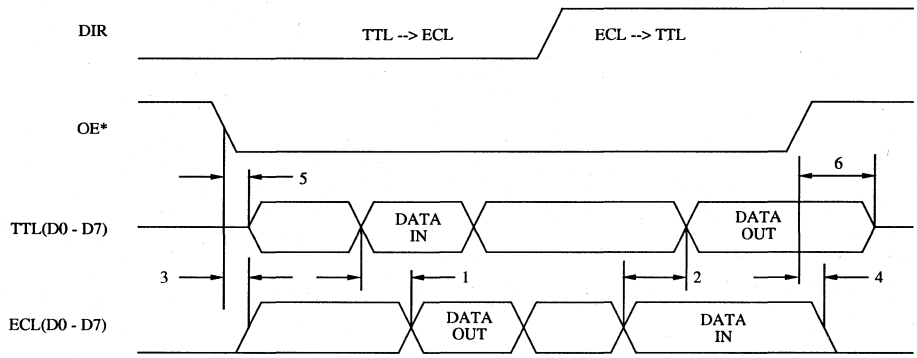
Note 1: Relative to ECL VCC
Note 2: Relative to TTL GND

Bt502—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL --> ECL Propagation Delay (Note 1) ECL --> TTL Propagation Delay (Note 1)	1 2	0.5 2		7 11	ns ns
ECL (D0–D7) Enable Time ECL (D0–D7) Disable Time (Note 1)	3 4	2 3		11 11	ns ns
TTL(D0–D7) Enable Time TTL(D0–D7) Disable Time (Note 1)	5 6	0.5 0.5		6.5 6.5	ns ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL(D0–D7) loading of 50 Ω to –2.0 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are –0.80 to –2.0 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Subject to capacitive loading.



Input/Ouput Timing.

Ordering Information

Model Number	Compatibility	Package	Ambient Temperature Range
Bt501KC	10KH ECL	24-pin 0.3" CERDIP	0° to +70° C
Bt502KC	100K ECL	24-pin 0.3" CERDIP	0° to +85° C

Bt622

Bt624

Very High-Speed Dual- and Quad-Channel ECL Delay Lines

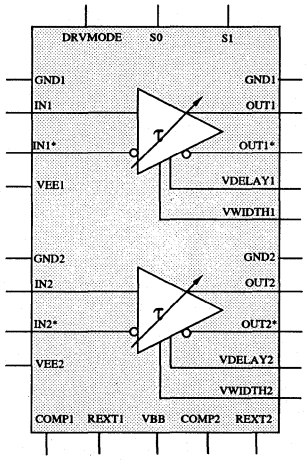
Distinguishing Features

- Greater than 200 MHz Bandwidth
- Four Adjustable Delay Lines in One Package
- Independent Delay Adjustments for Positive- and Negative-Going Transitions
- Three Selectable Delay Ranges: 10 ns, 20 ns, and 30 ns
- Mode Control for Common Signal Distribution to All Channels
- Adjustable Delays via External Voltages or Currents
- Individual GND/VEE Pins per Delay Section for Superior Crosstalk Performance
- Cascadable for Greater Delays and/or Multiple Taps
- 28-pin or 44-pin Plastic J-Lead (PLCC) Package with Internal Heat Spreader

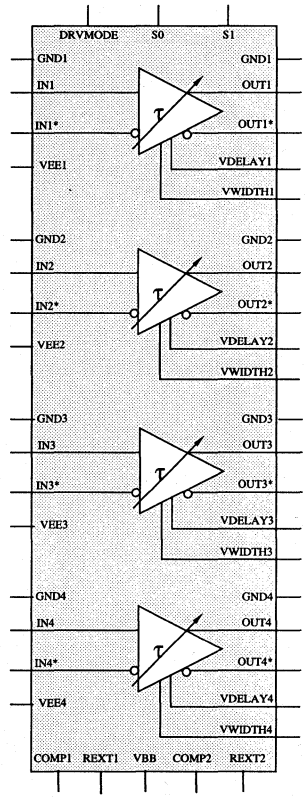
Applications

- Automatic Test Equipment
- Clocked ECL Circuitry
- CPU System Timing

Functional Block Diagrams



Bt622
Dual Channel



Bt624
Quad Channel

Product Description

The Bt622 and Bt624 Adjustable Delay Lines are designed for high-performance delay adjustments of high-frequency ECL signals. The Bt622 is a dual delay line, and the Bt624 is a quad version. Their varied applications include use in ATE as the prime method of deskewing multiple channels of a shared resource system, and the common need of signal timing adjustments in many clocked ECL circuits.

Two external delay adjustments are available for each channel, VDELAY and VWIDTH. Depending on the selected mode of operation, the adjustment inputs have different functions. When independent falling-edge delay adjustment is not required, VDELAY delays the input waveform over the selected ranges, and VWIDTH is not operational. When the falling-edge adjustment is enabled, VDLAY and VWIDTH adjust the delays of the rising (positive-going) and falling (negative-going) edges, respectively.

These devices allow for fine deskew control of multiple signal paths and permit compensation for differences in positive- versus negative-going signal delays through system paths.

The overlapping delay ranges allow for maximum versatility in optimizing the necessary delays while maintaining the required resolutions of adjustments.

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L622001 Rev. J

Brooktree®

Pin Descriptions

The signals that are individually assigned for each channel are suffixed by the channel number: 1 and 2 for the Bt622, and 1 through 4 for the Bt624.

Pin Name	Description
IN, IN*	Differential 10KH ECL-compatible inputs. The negative polarity input is indicated by the asterisk ("*"). The signal to be delayed is input to the device through this differential pair. Internal pullups and pulldowns ensure that, when they are left floating, IN will be pulled low and IN* will be pulled high to yield a stable differential low at the outputs.
OUT, OUT*	Differential ECL-compatible outputs. The negative polarity input is indicated by the asterisk ("*"). The signal to be delayed is output from the device through this differential pair.
DRVMODE	A single-ended 10KH ECL-compatible input. The input is internally pulled low. If DRVMODE is left floating or at ECL logical zero, the device acts as multiple independent delay channels. A logical one on this pin will distribute the signal input to channel 2 of the Bt624 to all other channels. The inputs to the other channels are also ORed into the signal path. The Bt622 channel 1 is driven to channel 2. In this mode the device acts as a skewable signal distribution component and minimizes the number of necessary connections to the package. Too many connections would degrade the input signal quality. Since the other channels are also ORed into the signal path, the fanned-out input signal may act as a modulation to all channels.
VDELAY	A voltage-control input that adjusts the delay through the channel. Depending upon the mode of operation selected by S0 and S1, this input is used in conjunction with VWIDTH for overall delay control. Nominal voltage range for this pin is –1.3 to –0.1 V for short and long delays, respectively. A 0.01 µF ceramic capacitor to GND is recommended on this pin for noise reduction. A constant current is mirrored internally at this pin with the current set by REXT1.
VWIDTH	A voltage-control input that adjusts the delay through the channel. Depending upon the mode of operation selected by S0 and S1, this input is used in conjunction with VDELAY for overall delay control. Nominal voltage range for this pin is –1.3 to –0.1 V. A 0.01 µF ceramic capacitor to GND is recommended on this pin for noise reduction. The VWIDTH pins are active only if S1 is a logical one or connected to VEE. A constant current is mirrored internally at this pin with the current set by REXT1.
COMP1	Compensation pin. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE.
COMP2	Compensation pin. A 0.1 µF ceramic capacitor must be connected between COMP2 and VEE.
S0	A single-ended 10KH ECL-compatible input. A logical zero selects the lower range of delay adjustment. A logical one selects the upper range of delay adjustment. The input may be connected to GND or VEE for a hard-wired range selection. Floating this input will select a logical zero. This is a global input that affects all channels. Used in conjunction with the S1 input pin, the S0 input selects the range of group delay for given control voltages at the VDELAY and VWIDTH input pins.
S1	A single-ended three-state input pin. An ECL logical zero disables the VWIDTH pins. Negative transitions will have the same delays as positive transitions. A logical one (or S1 tied to GND) will allow the VWIDTH pins to adjust the delays of the negative transitions through the delay channels. If –3.2 V is exceeded at this input while it is tied to VEE or left floating,

Pin Descriptions *(continued)*

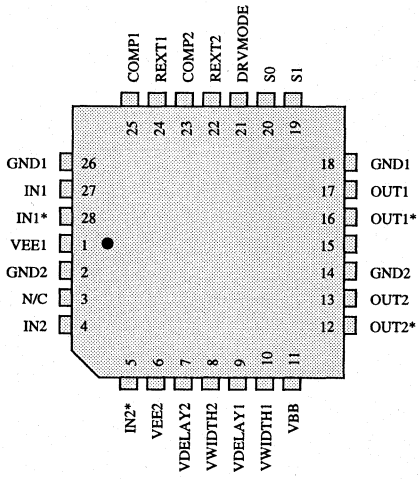
Pin Name	Description
	the extended delay range, Mode 5, will be enabled. In this mode, the VWIDTH input pins do not adjust the delay of the negative transition. The VWIDTH pins act as extensions to the VDELAY control pins. The text contains further explanation of the function of this pin. This is a global input that affects all channels.
VBB	Nominal –1.3 V output. When delay channels are driven single endedly, the complementary input may be connected to VBB. (Single-ended operation is not recommended for high-frequency or high-accuracy applications.) A 0.01 µF ceramic bypass capacitor to GND is recommended for applications with this pin.
GND	Device ground. All GND pins must be connected to ground.
VEE	Negative supply, typically –5.2 V. A 0.1 µF ceramic chip bypass capacitor to ground for all channels is essential for lowest crosstalk performance.
REXT1	Analog input. This input sets a reference current, which is mirrored internally at all VDELAY and VWIDTH control inputs. The nominal voltage at this node is –1.3 V. A 1.3 kΩ resistor to ground will develop a 1 mA reference current. Reference currents down to 50 µA may be used with no degradation in performance. The proper value depends upon the interfacing method to the VDELAY and VWIDTH inputs.
REXT2	Analog input. This input sets a reference current, which is mirrored throughout all of the internal gates of the Bt622/624. As such, this current input sets the overall power dissipation of the products. The current developed here will also alter the minimum delay and size of the delay range. By decreasing the current, the minimum propagation delay will increase on all channels and the range of delay for a given VDELAY/VWIDTH input will increase. The nominal voltage at this pin is –1.47 V. A 2.94 kΩ resistor to ground will develop a 500 µA reference current.

7

Pinouts for Bt622 and Bt624

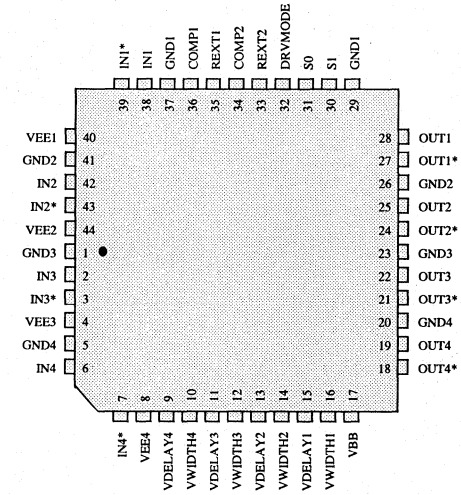
Bt622

28-pin Plastic J-Lead



Bt624

44-pin Plastic J-Lead



Application Information

Power Supply Decoupling

ALL VEE supply pins should be separately decoupled to GND with a 0.1 µF ceramic chip capacitor. The bypass capacitors should be as close as possible to the device.

A ground plane is recommended to provide a low-inductance ground return path. The individual channels have separate GND and VEE pins to maintain superior crosstalk performance. The bypass capacitor for each channel should be placed between GND1 and VEE1, GND2 and VEE2, GND3 and VEE3, and so on.

Internal Fanout

The DRVMODE control input is used to internally distribute the signal present at channel 2 of the Bt624 (channel 1 of the Bt622) to channels 1, 3, and 4 (channel 2 of the Bt622). This allows the user to terminate a high-quality signal at only one input, avoiding the larger lumped capacitances involved if multiple package inputs were daisy chained.

A detailed block diagram for the Bt624 is shown in Figure 1. DRVMODE enables the AND gate at channel 2 to drive the OR gate at the other channels, thereby buffering the signal and maintaining signal integrity. The unused channel inputs are still active. They have internal pullups and pulldowns to create a logical zero

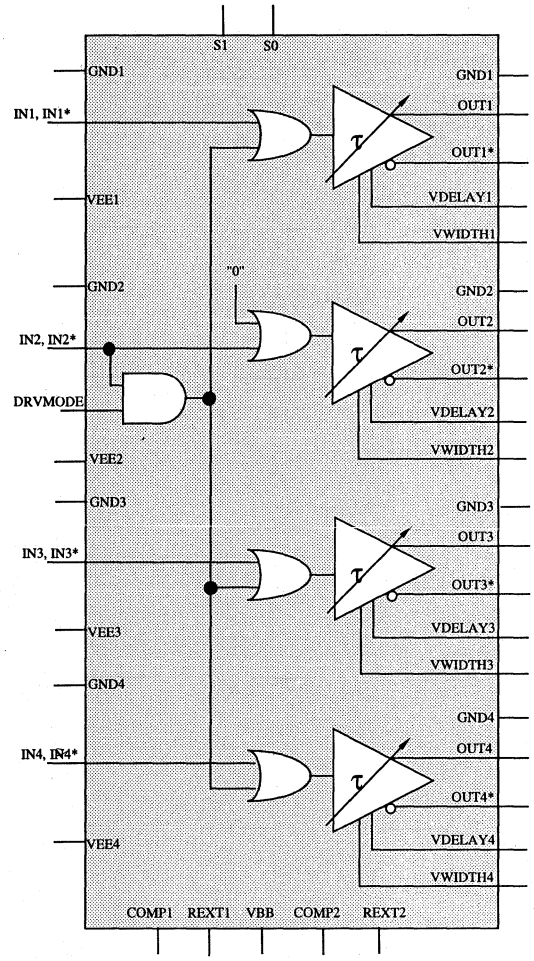


Figure 1. Bt624 Detailed Block Diagram.

at the inputs, allowing the user to float these inputs by leaving them unconnected. They may be driven with signals of their own, however. The application may be for a gated signal, such as a clock. The clock signal applied to channel 2 and fanned out through channel 1 may be controlled and gated ON or OFF at channel 1's output by asserting a logical zero or one, respectively, at channel 1's input.

When the signal is internally buffered and distributed to the other channel inputs, the signal may be delayed independently through each channel according to the mode selected and the signals present at the VDELAY and VWIDTH control inputs.

Ranges of Delay

The S0 and S1 control inputs select the range of delay for the signals through the Bt624. Two main types of delay are available. In the first type, the input signal is delayed and the output signal is a delayed version of the input signal. The other delay type allows independent delay control of the rising and falling edges.

Table 1 contains descriptions of modes versus control inputs. Modes 0, 1, and 5 are delays of type 1—group delays are imposed upon the input signal with *no* independent rising- and falling-edge adjustment. The criteria dictating which of these modes the application calls for are range of delay needed and the minimum pulse widths expected. Roughly, mode 0 is a 10 ns delay range, mode 1 is a 20 ns delay range, and mode 5 is an extended 30 ns delay range.

The equivalent circuit diagrams are depicted in Figures 2a, b, and c for modes 0, 1, and 5. Modes 0 and 1 delays are adjusted with the channel VDELAY inputs, only. The VWIDTH control inputs are nonfunctional and unused. Mode 0 uses a gate string of 15. Mode 1 has an additional 10 gates in the signal path to total 25 gates.

Mode 5 (Figure 2c) uses both the VDELAY and VWIDTH inputs for delay control. When Mode 5 is implemented, the VDELAY and VWIDTH inputs should be shorted together and a common control voltage should be applied. This extended delay range uses 35 gates in the signal path.

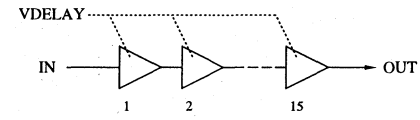


Figure 2a. Mode 0, 15 Gates.

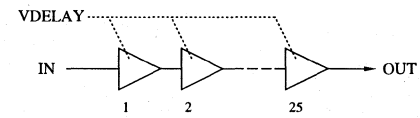


Figure 2b. Mode 1, 25 Gates.

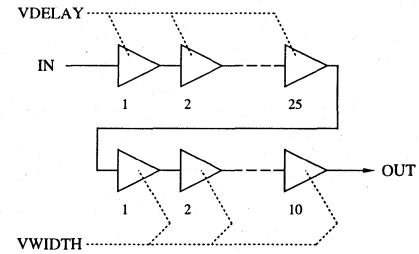


Figure 2c. Mode 5, 35 Gates.

MODE #	Input Pins		VWIDTH Operation Description	Nominal TSPAN	WIDTH Adj. Range
	S1	S0			
0	0	0	Unused	10	-
1	0	1	Unused	20	-
2	1	0	Active, Falling Edge	10	±5
3	1	1	Active, Falling Edge	20	±5
4 (Note 1)	~~VEE~~	~~0~~	~~Short to VDELAY~~	~~20~~	~~-~~
5	VEE	1	Short to VDELAY	30	-

Note 1: Mode 4 should not be used. It is functionally equivalent to mode 1.

Table 1. Delay Ranges Versus Input Configurations.

7

Application Information *(continued)*

Independent Edge Delays

Modes 2 and 3 can independently adjust the delays of the rising and falling signal edges. Mode 2 is a 10 ns delay range, and mode 3 is a 20 ns range. The selection of range depends on the desired range of overall delay (group delay) of the signal and on the amount of falling-edge adjustment required.

Figure 3 is a representation of the circuit topology of modes 2 and 3. The number of delay cells for the falling-edge adjustment remains constant. The VWIDTH delay range of adjustment is fixed and is the same for both modes 2 and 3 at 10 delay elements. The number of delay cells for the rising-edge adjustments changes from 15 to 25 for modes 2 and 3, respectively. The positive-going edge triggers the set input to the S-R flip-flop. The signal is inverted after it is delayed for the negative-going edge and triggers the reset input to the flip-flop.

Note: Upon power-up of the device or when operating modes are being changed, the S-R flip-flop is in an indeterminate state. A rising or falling edge that propagates through the channel will correct the situation. Therefore, before the device is used in mode 2 or 3, a dummy edge should be applied to the device before calibration takes place.

The falling-edge adjustment (with VWIDTH) controls the falling-edge delay only; it has no effect on the rising-edge delay. The VDELAY control has an effect on both the rising and falling edges. Therefore, delay calibration should be performed first with VDELAY, then with VWIDTH. This will be covered more fully in Calibrating a System Channel.

Figure 4 is a tool to determine whether mode 2 or 3 should be implemented in a particular application. When VDELAY is at minimum delay, the range of adjustment of the falling edge is 0 to +10 ns at the VWIDTH input. When VDELAY is at maximum delay, the falling edge has –10 to 0 ns of adjustability. These points set the ranges of adjustment that are available at the VWIDTH pin. The shaded area indicates the operating zone. The user should first determine the required range of adjustability of the falling-edge versus the rising-edge position. This will dictate what range of overall group delay is available for the particular mode. As an example, if ±2 ns of falling-edge adjustment is required, the intercepts for the operating range are at 20 percent and 80 percent of the VDELAY range. This relates to the center 60-percent range of overall VDELAY. This would allow 8.4 ns and 14.4 ns of group delay for modes 2 and 3, respectively, each calculated as 60 percent of the nominal available range. Similarly, if ±1 ns of falling-edge adjustment is required, 10 percent and 90 percent are the intercepts. These would allow 11.2 ns and 19.2 ns of adjustment range for modes 2 and 3, respectively.

Minimum Pulse Widths

The minimum pulse widths through the channels of delay are related to the chosen range of delay. The longer the range of delay, the longer a very small pulse width may be delayed before incurring inaccurate tracking and subsequent pulse swallowing.

The delay elements have bandwidth constraints for different range configurations and group delay control voltages. These bandwidth differences limit the acceptable minimum pulse widths [TPW(min)] for a delay channel.

Figure 5 illustrates the approximate minimum pulse widths that may be passed through the delay channels. These are nominal graphs of TPW(min) for the ranges achievable for modes 0 through 5.

The result of violating these minimum curves is a missing output pulse, as the pulse is swallowed.

Figure 5 refers to minimum pulse width. For modes 0, 1, and 5, the input and output pulse widths are the same. Modes 2 and 3 require special consideration for minimum pulse width involving the input pulse width [TPW(in)], the rising-edge delay [Tpd(rising)], the falling-edge delay [Tpd(falling)], and the minimum input pulse width [TPW(min)].

To obtain the desired output pulse while modes 2 and 3 are being used, the relationship in the following equation must be maintained:

$$TPW(in) - Tpd(rising) + Tpd(falling) \geq TPW(min)$$

With the Bt622/624, the falling-edge delay of the output pulse can be programmed for less than (or greater than) the rising-edge delay for a positive input pulse (or negative pulse). If the above relationship is violated, an undesirable state of operation will exist (see equivalent circuit of Figure 3).

Application Information *(continued)*

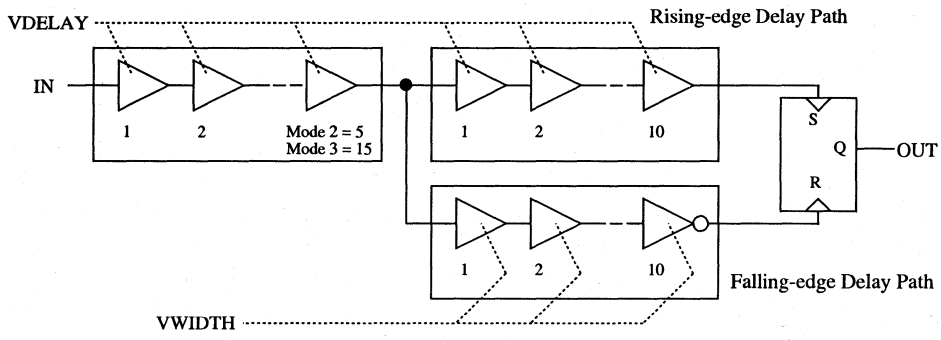


Figure 3. Modes 2 and 3 Equivalent Circuit.

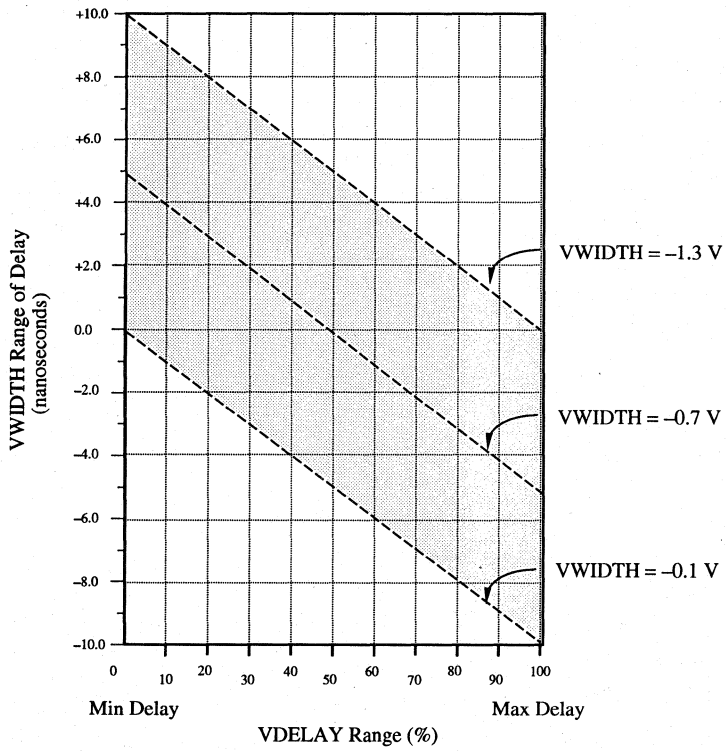


Figure 4. VWIDTH Delay Range Versus VDELAY.

7

Application Information *(continued)*

As shown in Figure 3, while modes 2 and 3 are being used, the rising and falling edges of the output pulse are controlled by setting and resetting, respectively, the output of a flip-flop. The programmed rising edge will set the flip-flop to output the rising edge [Tpd(rising)] of the output pulse. The programmed falling edge will then reset the flip-flop to output the falling edge [Tpd(falling)] of the output pulse.

If the above equation is not followed, the falling edge may be programmed for less than (or greater than) the rising edge for a positive input pulse (or negative input pulse). In this case, the signal to reset (or set) the flip-flop will appear prior to the signal to set (or reset) the flip-flop. The resultant output will not be a pulse but only a polarity reversal.

Therefore, while modes 2 and 3 are being used, the input pulse must be sufficient in width to accommodate the minimum input pulse width shown in Figure 5, and the difference between the falling- and rising-edge delays must be as desired.

The mode selection of a particular range of delay and falling-edge adjustment offers the user great flexibility in optimizing the needs of the applications at hand. Different range modes use more or less of the Bt622/624 circuitry. Unused on-chip circuitry is powered down to allow cooler operation.

Sample Application

Figure 6 depicts the Bt622 in a mode-2 application. The S1 input pin is connected to GND. This programs a logical one, which enables the VWIDTH pins for adjustment of negative transitions through all channels.

The DRVMODE input is set to a logical low (tied to –5.2 V), which allows channel 1 and channel 2 inputs to both be valid. If the pin had been a logical one, the input to channel 1 would also be ORed into channel 2.

Channel 1 is being driven with a differential ECL input as a high-performance application. The S0 input is set low (tied to –5.2 V) to enable the lower delay span for both channels. The VDELAY and VWIDTH control inputs are being driven from a current output DAC (e.g., a Bt110 octal DAC) with 1 mA full-scales. This offers complete digital programmability of the group delay (VDELAY) and the fine adjustment of the negative transitions (VWIDTH). The 1 mA current sources at these pins are added to the DAC output currents to enable voltages from –1.3 to –0.1 V, the entire adjustment range.

Channel 2, in contrast, is a lower-performance application. The input is driven single-endedly. The inverting input (IN2*) is connected to the VBB output of the Bt622 to allow proper ECL switching at the –1.3 V point. The delay control inputs are adjusted by the trimming resistor (R4) to ground. The VDELAY and

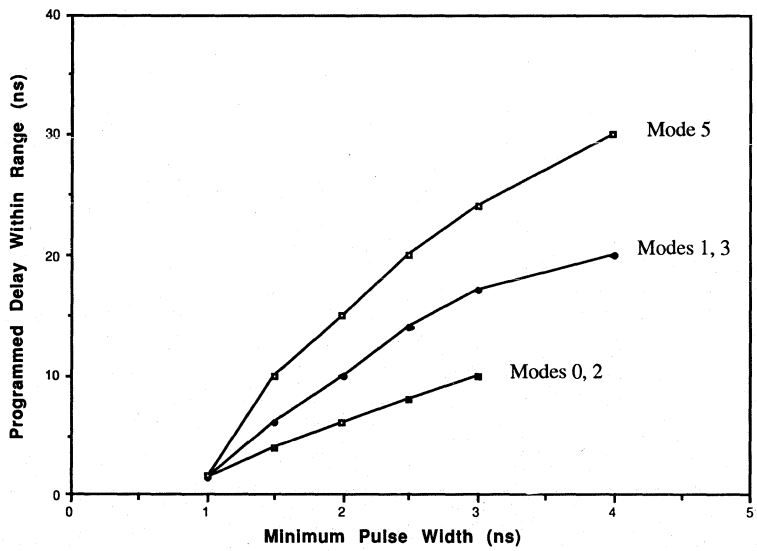


Figure 5. Minimum Pulse Width Versus Group Delay.

Application Information *(continued)*

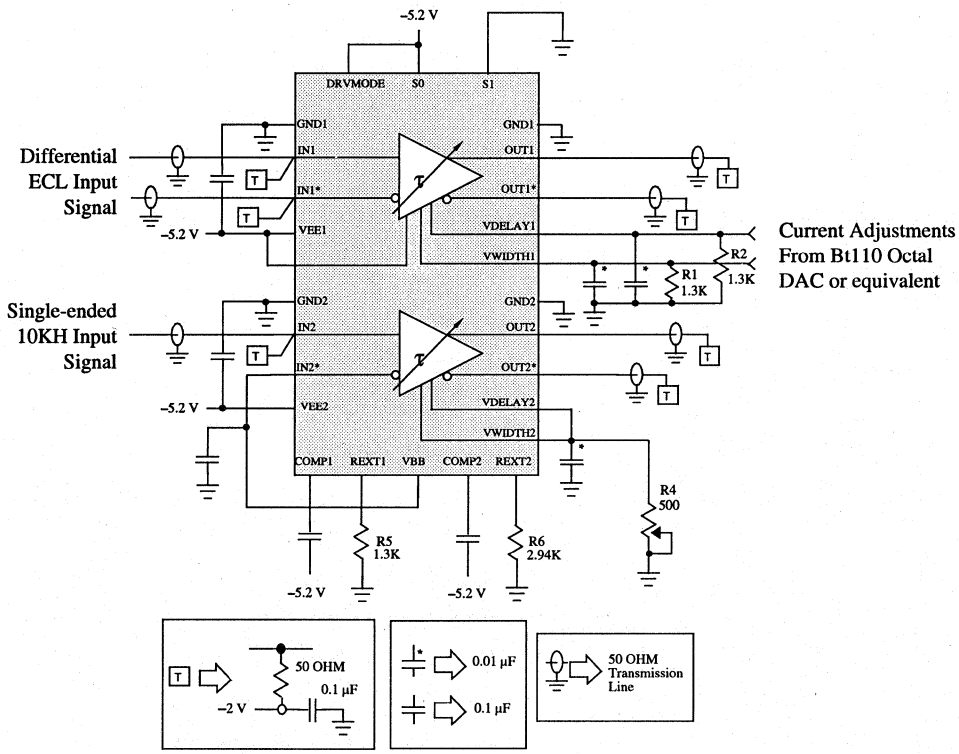


Figure 6. Bt622 Typical Applications.

VWIDTH control inputs are shorted together and tied to this same controlling resistor. Since two control inputs are tied together, 2 mA of node current results (1 mA for each input). Therefore, the 500 Ω trimming resistor will allow a range of –1 to 0 V. This type of connection is used for less demanding applications where the relevant timing is only to a single edge, and independent adjustment of rising and falling edges is not needed. With the two inputs commoned to the same voltage node, the delays of the rising and falling edges will track and be approximately the same.

The Bt622/624 have open-emitter outputs; thus, they must be terminated through 50 Ω resistors to –2 V at the end of the transmission paths or the equivalent. Microstrip layout techniques are recommended. The input signals should also abide by proper high-frequency layout rules. Possible reflection sources should be minimized, and a constant low-impedance transmission line to the device should be maintained.

Figure 6 shows both channels' differential outputs terminated. Single-ended terminations of the outputs are not recommended for maximum performance. All differential stages should be equally loaded. Figure 6 also shows each termination resistor with its own bypass capacitor to ground for the –2 V termination voltage. The use or nonuse of individual capacitors for each termination resistor is a function of the actual layout, and the resultant ground and –2 V path impedances. Adjacent termination resistors may be able to use a single bypass capacitor. Chip resistors are recommended for maximum performance. Common resistor networks are not recommended for optimum operation.

Although the Bt622/624 is designed to operate with constant power dissipation, the airflow requirement of 400 LFPM is recommended to minimize thermal variations, which may result in tens of picoseconds of delay variations.

Maximum performance from the Bt622/624 can only be obtained by careful layout and evaluation. Timing measurements in the sub-100 picosecond range are valid only if great care in the total environment of the device is observed. Great care was taken to design and specify these devices for maximum performance and ease of use. The user should follow these recommendations in the applications and evaluations of the devices.

Application Information *(continued)*

Delay Channel Linearity

Figure 7 is a graph of the delay linearity versus VDELAY control voltage. The transfer curve is not an ideal straight line; there is a characteristic nonlinearity to the curve. The Bt622/624 was not designed to be ultralinear. It is guaranteed monotonic; any decrease in control voltage will increase the programmed delay. All modes will exhibit this characteristic curve over the delay range. The figure calculates the nonlinearity as a percentage of the full-scale delay span.

Table 1 is a further aid in visualizing the flexibility of ranges available. Given the two input pins, S1 and S0, six different range configurations are possible. Since these ranges are all unique in group delay and falling-edge adjustment capability, they are enumerated as mode numbers 0 through 5. Mode 4 has been marked through; it is functionally redundant to mode 1. For this reason, it is not specified in the document and not tested for performance.

The AC Characteristics section of this document specifies the sensitivities at the endpoints of the transfer function for given voltages at the VDELAY control inputs. A further aid for determination of the required DAC resolution necessary for adjustment resolution is offered in Figure 8. The figure quantifies the approximate resolutions of delay attainable given different resolutions of DACs programming the VDELAY input pins. The figure separates the DAC resolutions necessary for low and high delay ranges. The VDELAY control input is a voltage-dependent input. Since the node has an internal 1 mA current source, a controlling current may also be used. A 1 kΩ resistor to ground will generate –1.0 V at the VDELAY or VWIDTH inputs. Variable currents injected into this node will supply currents to the current source and, therefore, reduce the voltage created at the control inputs. If only 8-bit DACs are available, two current outputs may be added together, with one output having a 1 mA full-scale output and the other DAC having a 125 µA full-scale output. The effective resolution would then be equivalent to a single 11-bit DAC driving the VDELAY pin.

Another method for obtaining greater resolution, but at the expense of overall range, is use of a fixed resistor to ground as a coarse adjustment to the beginning of the required range. A DAC current output then added into the node will act as a fine dither adjustment.

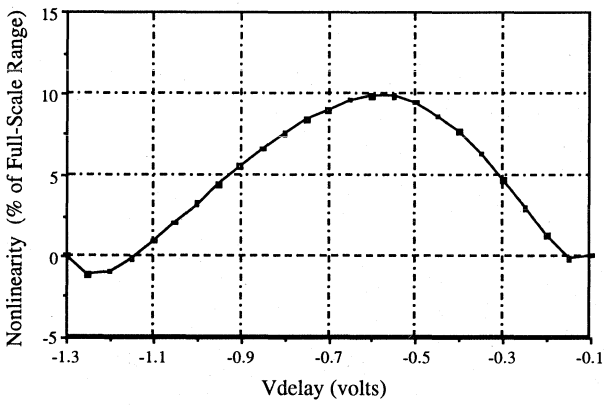


Figure 7. Bt622/624 Delay Linearity Versus VDELAY.

Nominal Picoseconds/LSB	DAC Resolution (# of bits)	
	Modes 0, 2	Modes 1, 3
156.0	6	7
78.0	7	8
39.0	8	9
19.0	9	10
9.7	10	11
4.9	11	12
2.4	12	

Figure 8. Bt622/624 Delay Versus DAC Resolution.

Application Information *(continued)*

Calibrating a System Channel

When the Bt622/624 delay lines are used to calibrate positive- and negative-going transitions, it is necessary to calibrate the positive-going transitions first. This is the case when mode 2 or 3 is implemented.

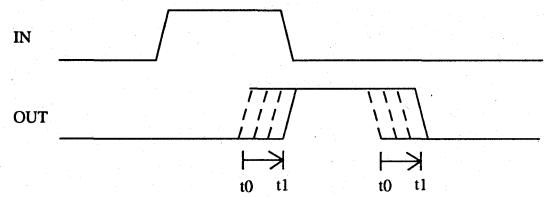
Figure 9 is a graphic representation of channel calibration with these devices. In Figure 9a, the adjustment is made at the VDELAY pin to move both polarities of transitions from t0 to t1. The falling edge moves less than the rising edge, but only the positive-going edges are being calibrated. Although both edge polarities are being adjusted, only the positive-going edge is relevant to the system at this point in the calibration. The VWIDTH adjustment pin is programmed for midscale while the positive edge is calibrated.

When the positive-going edge has been calibrated, the negative-going edges are calibrated at the VWIDTH pin. The VWIDTH pin can now be adjusted to provide more or less delay for the negative-going edges. Figure 9b indicates that the edge is being moved more positive by t3 ns. The rising-edge delay remains constant when the VWIDTH pin is adjusted.

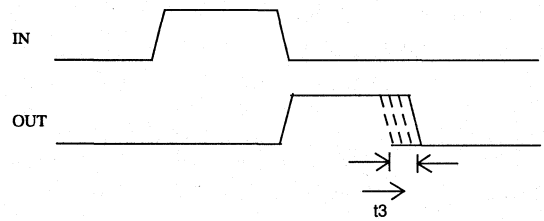
When a system channel is calibrated in mode 2 or 3, the output flip-flop must first be set to a determinate state. Figure 3 is a graphic representation of the circuit. Upon power-up of the part, the output S-R flip-flop is indeterminate. An input edge, either rising or falling, will set the output to the correct state, and calibration may proceed from there.

Also, when a system channel is calibrated in mode 2 or 3, a large pulse width should be allowed. When a small pulse width is applied (less than 10 ns) and calibration is proceeding on the rising edge by varying the VDELAY control, the pulse could disappear if the VWIDTH control is at or near minimum voltage. If VDELAY is set at or near maximum voltage (–1.3 V) and VWIDTH is set at or near minimum voltage (–0.1 V), the falling edge is delayed –10 ns with respect to the rising edge. This means that the pulse can no longer exist. For this reason, calibration should take place with pulses greater than 20 ns. Fine adjustments to VDELAY and VWIDTH may subsequently be made with small pulse widths.

When this calibration is complete, the channel has been deskewed to other channels. Any variation of delay between positive- and negative-going signals from the beginning to the end of the system channel has been accounted for and adjusted out.



a. Servo the Group Delay at VDELAY Pin.



b. Servo the Negative Transition at VWIDTH Pin.

Figure 9. Bt622/624 Channel Calibration.

Application Information *(continued)*

Control Voltage Circuits

The output delay control pins VDELAY and VWIDTH can be interfaced with a current-output DAC (as in the Bt110), a voltage-output DAC, or a resistor connection to ground.

The VDELAY and VWIDTH nodes, as described in the Pin Descriptions section, are inputs to internal current sinks. This is graphically indicated in Figures 10a and 10b.

Figure 10a shows the connection to a current-output DAC. For this discussion, Vcntrl will equal VDELAY or VWIDTH. The resistor value for R1 should be chosen so that the required full-scale control voltage, Vcntrl, is generated by the referenced current I. This full-scale voltage will be generated with the DAC outputting zero current. As the DAC sources more current into the node, less current flows through the resistor R1. Therefore, the voltage generated across the resistor decreases and generates the minimum control voltage. So, the equation is:

$$Vcntrl = (Idac - I)*R1.$$

Figure 10b indicates the connection for a positive voltage-output DAC controlling Vcntrl. As shown, the combination of current source I and resistor R1 generates the proper offset voltage, and resistor R2 generates the required attenuation.

The method with which to calculate the resistor values R1 and R2, given the DAC output voltages and Vcntrl endpoints, is as follows:

$$Vcntrl = Vdac*(R2/(R1 + R2) - I*R1*R2/(R1 + R2)$$

With

$$A = R2/(R1 + R2) \text{ and } B = R1*R2/(R1 + R2)$$

so

$$Vcntrl = Vdac*A - I*B$$

and assuming

$$0\ V \le Vdac \le Vdac(max) \text{ and,}$$
$$Vcntrl(min) \le Vcntrl \le Vcntrl(max),$$

then, isolating A and B, and substituting yields,

$$B = -Vcntrl(min)/I,$$
$$A = [Vcntrl(max) + B*I]/Vdac(max),$$

and

$$R2 = B*(1 + A/(1 - A))$$
$$R1 = R2*(1 - A)/A.$$

For example:

$$0\ V \le Vdac \le 7\ V,$$
$$-1.0\ V \le -0.1\ V, \text{ and,}$$
$$I = 1.0\ mA.$$

Substituting into the above equation

$$B = 1.0\ V/1.0\ mA = 1000\ \Omega,$$
$$A = (-0.1\ V + 1000\ \Omega*1.0\ mA)/7\ V = 0.128\ V,$$
$$R2 = 1000*[1 + 0.128/(1 - 0.128)] = 1148\ \Omega$$

and

$$R1 = 1148*(1 - 0.128)/0.128 = 7776\ \Omega.$$

Application Information *(continued)*

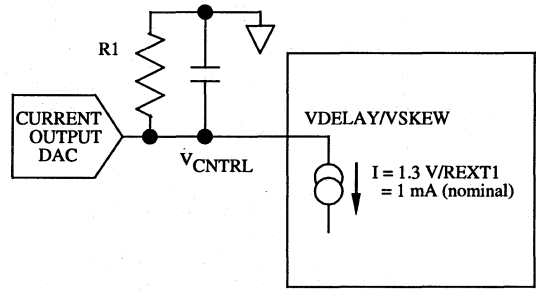


Figure 10a. Control Voltage from IOUT DAC.

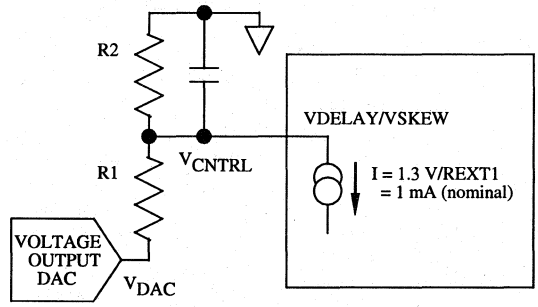


Figure 10b. Control Voltage from VOUT DAC.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	V
Negative Power Supply	VEE	–4.9	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Thermal Resistance					
Junction to Air					
Bt622KHJ					
Still Air	θJA		48.8		°C/W
50 LFPM of Airflow	θJA		35.5		°C/W
400 LFPM of Airflow	θJA		26.4		°C/W
Bt624KHJ					
Still Air	θJA		41		°C/W
50 LFPM of Airflow	θJA		33		°C/W
400 LFPM of Airflow	θJA		21		°C/W
Junction to Case					
Bt622KHJ	θJC		11.3		°C/W
Bt624KHJ	θJC		12.4		°C/W

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute (LFPM) over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (relative to GND)		0		–6.0	V
Voltage on any Digital Pin				VEE	V
Output Current				–50	mA
Ambient Operating Temperature	TA	–55		+70	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Digital Input High Voltage (Note 1)						
IN, IN*	VIH	0	–1170		–840	mV
		+25	–1130		–810	mV
		+70	–1070		–735	mV
Digital Input High Voltage (Note 1)						
DRVMODE, S0, S1	VIH	0	–1170		0	mV
		+25	–1130		0	mV
		+70	–1070		0	mV
Digital Input Low Voltage (Note 1)						
IN, IN*	VIL	0	–1950		–1480	mV
		+25	–1950		–1480	mV
		+70	–1950		–1450	mV
Digital Input Low Voltage (Note 1)						
DRVMODE, S0	VIL	0	VEE		–1480	mV
		+25	VEE		–1480	mV
		+70	VEE		–1450	mV
Digital Input Low Voltage (Note 1)						
S1	VIL	0	–2100		–1480	mV
		+25	–2100		–1480	mV
		+70	–2100		–1450	mV
S1 Third State (Extended Delay)		FULL	VEE		–3.2	V
Digital Output High Voltage		0	–1020		–760	mV
(Note 1)	VOH	+25	–980		–730	mV
		+70	–920		–680	mV
Digital Output Low Voltage		0	–1950		–1630	mV
(Note 1)	VOL	+25	–1950		–1630	mV
		+70	–1950		–1600	mV
Input High Current (Vin = VIHmax)						
IN, DRVMODE, S0, S1	IIH	FULL		100	250	µA
IN*	IIH	FULL	–100	–20		µA
Input Low Current (Vin =VILmin)						
IN, DRVMODE, S0, S1	IIL	FULL		40	150	µA
IN*	IIL	FULL	–100	–40		µA

See test conditions and note at the end of this section.

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DC Characteristics *(continued)*

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
VEE Supply Current						
Quad Channel (Bt624)						
Mode 0.	IEE	FULL		240	300	mA
Modes 1, 2		FULL		300	370	mA
Modes 3, 5		FULL		360	450	mA
Dual Channel (Bt622)						
Mode 0	IEE	FULL		160	215	mA
Modes 1, 2		FULL		195	230	mA
Modes 3, 5		FULL		230	280	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with all OUT and OUT* outputs terminated through 50 Ω to –2.0 V, REXT1 = 1.3 kΩ, and REXT2 = 2.94 kΩ. All parameters specified at 0°C are guaranteed by characterization and are not 100-percent production tested. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., –5.2 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Note 1: Relative to GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays (Note 1)					
Minimum Delays					
MODE S1 S0 VDELAY VWIDTH					
0 0 0 –0.1 V X	TPDmin	4.6	6.5	7.9	ns
1 0 1 –0.1 V X	TPDmin	7.2	9.1	11.0	ns
2 1 0 –0.1 V –0.1 V	TPDmin	5.4	7.1	8.6	ns
3 1 1 –0.1 V –0.1 V	TPDmin	7.9	9.9	12.3	ns
5 VEE 1 –0.1 V –0.1 V	TPDmin	10.7	12.9	15.9	ns
Delay Adjustment Ranges					
MODE					
0 Vcontrol = VDELAY	TPDspan	10.0	15.0	20.0	ns
1 Vcontrol = VDELAY	TPDspan	17.3	25	32.0	ns
2 Vcontrol = VDELAY & VWIDTH	TPDspan	10.0	16.3	20.0	ns
3 Vcontrol = VDELAY & VWIDTH	TPDspan	17.3	26.3	32.0	ns
5 Vcontrol = VDELAY & VWIDTH	TPDspan	25.0	36	44.0	ns
Rising-Edge Delay Versus VWIDTH Delay Change (Modes 2 and 3) (Note 4)			±30		ps
Delay Versus Frequency (Notes 2 and 4)			50		ps
VWIDTH Range of Adjustment (Mode 2 or 3 Only) VWIDTH = –0.1 V to –1.3 V		7.0	10.0	13.0	ns
Rising- to Falling-Edge Delay Matching					
Modes 0, 1, 5 (Note 4)			–100		ps
Modes 2, 3 (Notes 4, 5)			1		ns
Propagation Delay Tempco (Notes 3 and 4)			0.05		% TPD/ °C
Output Rise/Fall Times (20% to 80%) (Note 4)	Tr, Tf		850		ps
Power Supply Rejection Ratio (Note 4)	PSRR		0.5		% TPD/V

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 °C with 400 LFPM of airflow, and all outputs terminated with 50 Ω to –2.0 V. Timing reference points at the differential crossing points for input and output signals, REXT1 = 1.3 kΩ, and REXT2 = 2.94 kΩ. All input signals are fully differential. Values are based on nominal temperature and supply voltage of –5.2 V.

Note 1: All measurements refer to both rising and falling edges for modes 0, 1, and 5, and rising edges only for modes 2 and 3. DRVMODE is logically low. Delay adjustment ranges are the difference in propagation delay with Vcontrol at –1.3 V and –0.1 V. Modes 2, 3, and 5 delay minimums and delay ranges are measured with VWIDTH = VDELAY.

Note 2: Delay versus frequency characteristics are measured by setting VDELAY = VWIDTH = –0.7 V. The delay is measured for both rising and falling edges of a pulse at a 10 MHz repetition rate (100 ns period). The rising- and falling-edge delays are again measured at a 100 MHz repetition rate (10 ns period). The variation in delays is the delay versus frequency. Measurements are performed with a pulse width of 5 ns.

Note 3: For example, 5 ps/ °C when programmed for a 10 ns delay (see Figure 11).

Note 4: Not 100-percent tested, based upon characterization data.

Note 5: The falling-edge delay is longer than the rising-edge delay for modes 2 and 3 when Vcontrols = –0.1 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

AC Characteristics *(continued)*

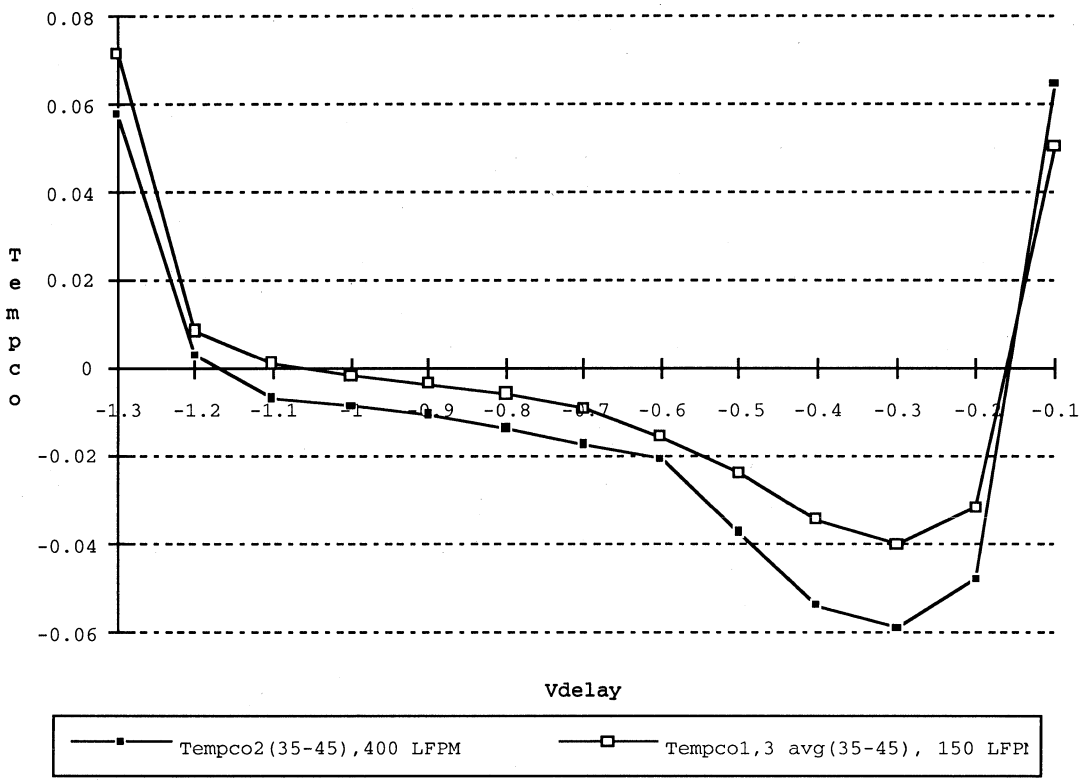
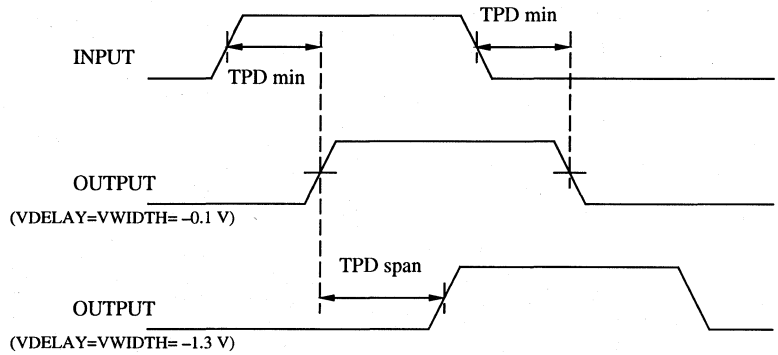


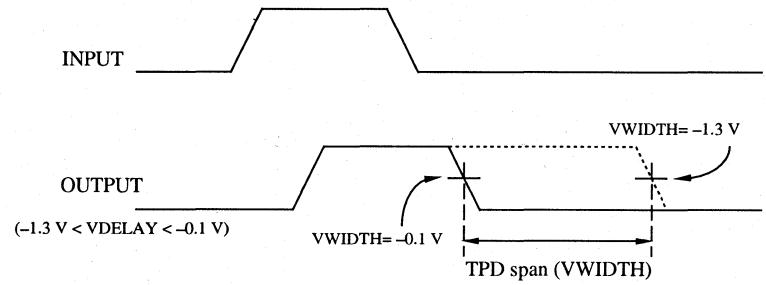
Figure 11. Tempco Versus Vdelay, 35°–40°C, Mode 5.

Timing Waveforms

All Modes



Modes 2 and 3 Only



Ordering Information

Model Number	Package	Ambient Temperature Range
Bt622KHJ	28-pin PLCC (with internal heat spreader)	0° to +70° C
Bt624KHJ	44-pin PLCC (with internal heat spreader)	0° to +70° C

Bt630

Monolithic CMOS High Bandwidth Programmable Range 20–400 Nanoseconds 5-Tap Delay Line

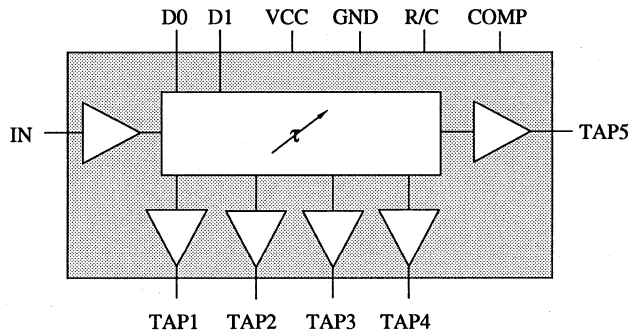
Distinguishing Features

- Up to 50 MHz Bandwidth
- 15 ns Minimum Input Pulse Width
- Monolithic CMOS Construction
- Programmable Full-scale Delays 20–400 ns
- 50 mW Typical Power
- Five Buffered Taps at 20, 40, 60, 80, and 100% of Full-scale Delay
- Output Delay Accuracies to ±10% or ±3 ns, whichever is greater

Applications

- CPU Clock Timing
- Memory Timing
- Pulse Generator Circuits
- Bus Interface Timing

Functional Block Diagram



Product Description

The Bt630 is a buffered tapped delay line with input and output compatibility to TTL logic families.

The Bt630 is useful for generating multiple edges from a clock signal at its input. The five delay taps are at the 20%, 40%, 60%, 80%, and 100% points of the programmed full-scale delay.

Unlike fixed tapped delay lines, the Bt630 is adjustable in full-scale delay from 20–400 ns. This flexibility allows the user a range of delays that would be impossible without a large inventory of different, fixed span, tapped delay lines.

Selection of the full-scale delay is performed by a coarse and fine adjustment. The coarse adjustment is set by two digital input bits. The four selectable ranges are 20–50, 40–100, 80–200, and 160–400 ns.

The fine adjustment is set by an external resistor and capacitor. Fixed value components may be used, or variable resistors can be employed to adjust delays individually.

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(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L630001 Rev. D

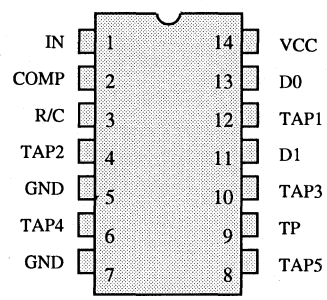
Brooktree®

Pin Description

Pin Name	Description
D0, D1	The digital control inputs which select the operating full-scale delay range. D0 is the LSB. The truth table for range value is:
R/C	The node where a resistor and capacitor connect to set up the precise full-scale delay for a given range selected by pins D1 and D0.
COMP	A compensation pin where a 0.1 µF filter capacitor to ground is connected. The nominal voltage at this point is 3.3 V.
IN	The input to the delay line. TTL-compatible input thresholds.
TAP5	The full-scale delay output. TTL compatible.
TAP4	The 80% of full-scale delay output. TTL compatible.
TAP3	The 60% of full-scale delay output. TTL compatible.
TAP2	The 40% of full-scale delay output. TTL compatible.
TAP1	The 20% of full-scale delay output. TTL compatible.
VCC	Power input pin, 5 V nominal. A 0.1 µF ceramic capacitor to ground is recommended for bypassing.
GND	Power ground pins.
TP	This is a manufacturing test pin. No connection should be made to this pin by the user.
	(Unused outputs should be left open.)

D1	D0	RANGE
0	0	20–50 ns
0	1	40–100 ns
1	0	80–200 ns
1	1	160–400 ns

Bt630KP



Application Information

Power Supply

COMP and VCC pins should be separately decoupled to GND with 0.1 µF ceramic capacitors. The bypass capacitors should be as close as possible to the device pins.

Upon power up of the Bt630, approximately 100 milliseconds should be allowed for the device to settle on its programmed delay. After this time, the device will meet specifications of performance.

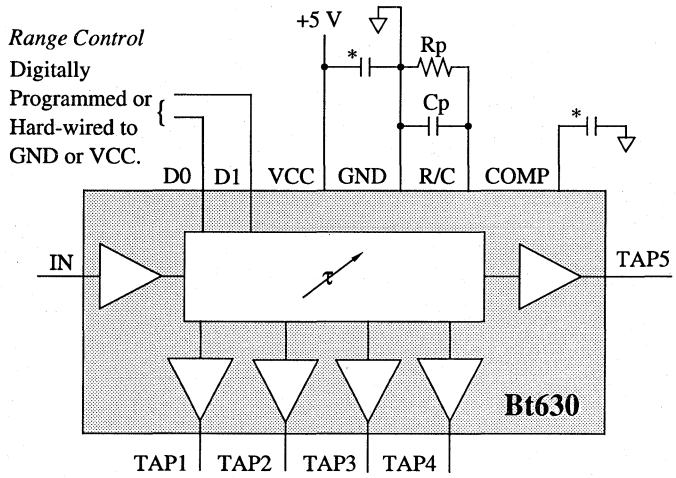
Applications

The full-scale delay of the Bt630 is set with an external resistor/capacitor combination and two digital bits of range control. The digital ranging bits offer the selection of the range in coarse increments. The resistor/capacitor combination allows the user to fine tune the selected delay within the range. Cp and Rp are the programming capacitor and resistor combination (see Figure 1). Once the range has been selected via the digital control bits and given a fixed value capacitor, the delay can be adjusted over a 2:1 range using Rp.

The ranges available using the digital control bits are indicated in Table 1. The base period, Tbase, is controlled by the digital bits. The overall delay follows the formula:

$$Tdelay = [Rp * (Cp + 1.8)]/k$$

where k varies, based on Tbase.



* = 0.1 microfarad ceramic capacitor, 10%.

Figure 1. Bt630 Typical Application.

Range	k	Tbase	Range of Delays
0	32	20 ns	20–50 ns
1	16	40 ns	40–100 ns
2	8	80 ns	80–200 ns
3	4	160 ns	160–400 ns

Table 1. Bt630 Delay Ranges.

Application Information *(continued)*

The relationship in Table 1 allow for common units to be used in the equation,

$$Tdelay\ (ns) = [Rp(k\Omega) * (Cp(pF) + 1.8\ pF)] / k$$

where 1.8 pF is attributed to package capacitance. Recommendations are to choose Cp and Rp so that Cp is a 1% mica capacitor (this is a low-cost, easily-obtained value with temperature coefficients of ±100 ppm/°C) and Rp is a metal-film type resistor (easily obtained in 100 ppm/°C, e.g., RN55D, down to ±25 ppm/°C, e.g., RN55E, and temperature coefficients with a tolerance of 1% to 0.1%).

Jitter

Preliminary characterization data taken to categorize jitter shows that the amount of jitter is directly dependent upon the combination of the programming resistance (Rp) and capacitance (Cp) used to set the full-scale delay. To a lesser extent, jitter is also dependent upon the range and tap selected to obtain the desired delay of the device.

It can be reduced substantially by using the lowest combination of Rp and Cp possible in fine tuning the desired full-scale delay of the device. Values of Rp and Cp should be chosen as close as possible to the specified minimum product of

$$Rp(\Omega) * Cp(F) \geq 400 * 10^{-9}$$

This will ensure that the delay of the device is in accordance with that specified by the Tdelay formula and will substantially reduce the amount of jitter. It is imperative to use the lowest possible RpCp combination if a reduction in the amount of jitter is desired.

The apparent jitter of the device has also been found to increase with both range (0–3) and tap (1–5). Therefore, to further minimize the jitter of the device, the lowest range along with the lowest of the 5 taps available should be used with the minimum combination of RpCp. The relationship between the combination of RpCp and range for apparent jitter of the device is shown in Figure 2 with Cp = 100 pF and Rp from 6–16 kΩ for tap 5.

Even though the relationship as shown in Figure 2 is not linear, the following formulas have been derived to assist in determining the approximate jitter (peak-to-peak) present for the chosen RpCp combination within each range of operation (shown in Figure 3).

Range	Typical Jitter (ns, peak-to-peak) where Rp (in kΩ), Cp (in pF)
0, 1	(0.0032 * Rp * Cp) – 1.8
2	(0.0036 * Rp * Cp) – 1.9
3	(0.0045 * Rp * Cp) – 2.3

In summary, to reduce the amount of jitter in the delay, the combination of RpCp should be as close as possible to the specified minimum, and the lowest range and the lowest tap should be used.

Application Information *(continued)*

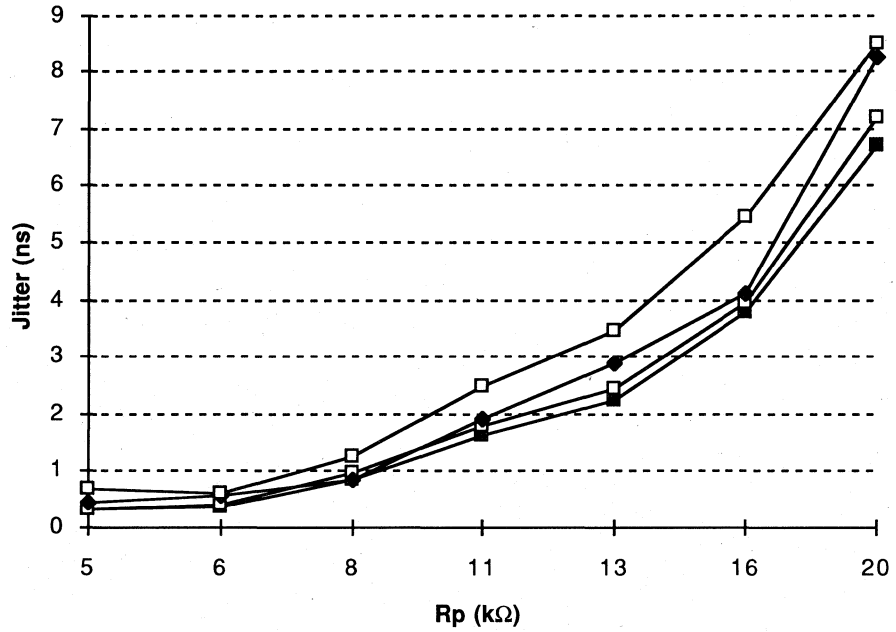


Figure 2. Typical Jitter versus Rp (at 25°C with Cp = 100 pF).

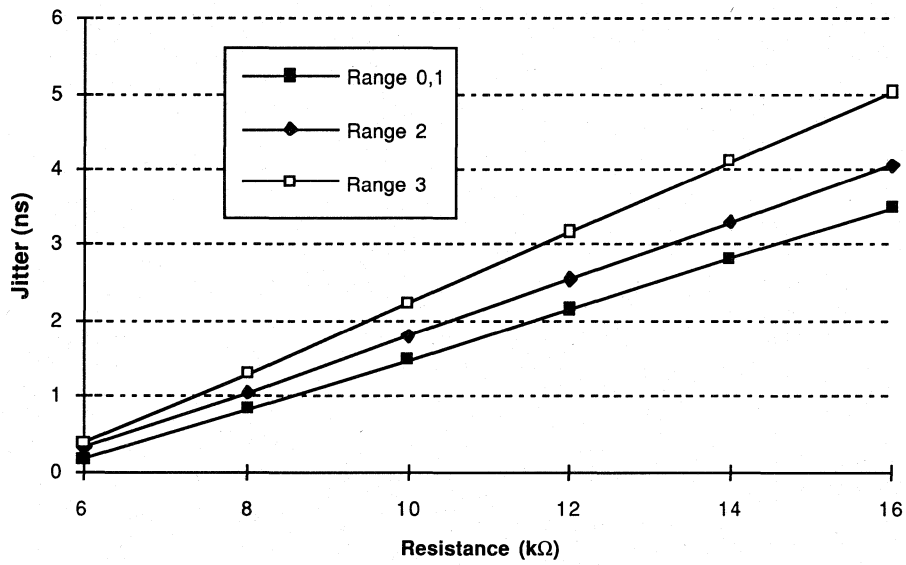


Figure 3. Typical Jitter versus Rp by Range Using Formulas (at 25°C with Cp = 100 pF).

7

Recommended Operation Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive	VCC	4.75	5.0	5.25	V
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (relative to GND)				7.0	V
Voltage on any Digitial Pin		GND–0.5		VCC + 0.5	V
Output Current (any one output)				–50	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature 5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH	–10		10	µA
Input Low Current (Vin = 0.4 V)	IIL	–10		10	µA
Input Capacitance (Note 1) (f = 1 MHz, Vin = 2.4 V)	CIN			10	pF
Digital Outputs					
Output High Voltage (IOH = –0.4 mA)	VOH	2.4	3.3		V
Output Low Voltage (IOL = 16 mA)	VOL			0.4	V
VCC Power Supply Rejection (Measured at Tap5, Range = 0) (Notes 1 and 2)	PSRR		0.2		%/V
VCC Supply Current					
Static—No Input Signal	ICC (static)		10	25	mA
25 MHz Input Signal	ICC(dynamic)		30	45	mA
Output Drive /Tap				10	TTL Loads
Output Drive/ all Taps (Note 3)				20	TTL Loads
Programming Capacitance (Notes 1 and 4)	Cp			300	pF
Programming Resistance (Notes 1 and 4)	Rp	6		16	kΩ

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Cp = 100 pF, Rp = 8.0 kΩ and 16 kΩ at 25°C. All parameters specified at 0°C and 70°C are guaranteed by characterization and are not 100 percent production tested.

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Note 1: Not tested in production. Based on characterization data.
Note 2: PSRR as a percentage change in Tdelay versus supply voltage.
Note 3: More loads may be driven with degraded delay accuracy specification. See Figure 4, Output Delay versus Loading. One TTL load is defined as Vil = 0.4 V max at Iil = 1.6 mA and Vih = 2.4 V min at –40 µA.
Note 4: The product of Rp and Cp must be greater than 400×10^{-9}, $Rp(\Omega) * Cp(F) \geq 400 \times 10^{-9}$, to ensure output delay according to the formula for Tdelay = [Rp * (Cp + 1.8)]/k.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Minimum Input Pulse Width					
at Minimum Delay					
Range 0, 1, 2	TPWH, TPWL	10			ns
Range 3	TPWH, TPWL	15			ns
at Maximum Delay					
Range 0	TPWH, TPWL	20			ns
Range 1	TPWH, TPWL	25			ns
Range 2	TPWH, TPWL	35			ns
Range 3	TPWH, TPWL	45			ns
Delay Accuracy (Note 1)	Tdelay	–10		+10	% of nominal
			or		
(Rising or Falling Signals)		–3		+3	ns
Delay Tempco (Note 2)					
Range 0			5	15	ps/°C
Range 1			10	20	ps/°C
Range 2			20	25	ps/°C
Range 3			40	50	ps/°C
Output Rise/Fall Time (Measured at 0.6 V and 2.4 V)	Tr, Tf		2		ns

AC characteristics test conditions (unless otherwise specified): "Recommended Operating Conditions" with all outputs loaded with 1 TTL load (plus 20 pF lumped capacitance). Input signal per timing diagram (Figure 5) with input Tr, Tf = 2 ns (20 percent to 80 percent).

Note 1: Tdelay is guaranteed at 25°C and nominal V_{CC} (5.0 V) only. Tdelay is specified for all taps from input to tap output with Cp = 100.0 pF and ideal Rp resistor value. Nominal delays are calculated using the formula Tdelay = [Rp * (Cp + 1.8)]/k. If ±10 percent of Tdelay nominal is < 3 ns, then ±3 ns is the delay accuracy. Tolerances on Cp and Rp add to the Tdelay accuracy specification.

Note 2: For optimum performance, choose low-temperature coefficient components for Rp and Cp.

AC Characteristics *(continued)*

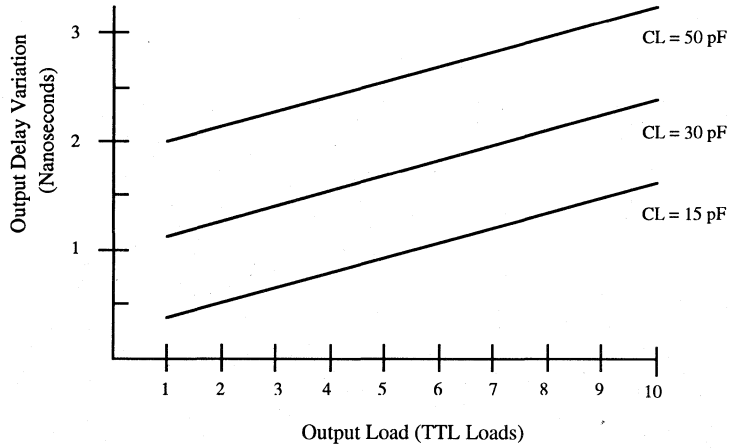

Figure 4. Output Delay versus Tap Loading.

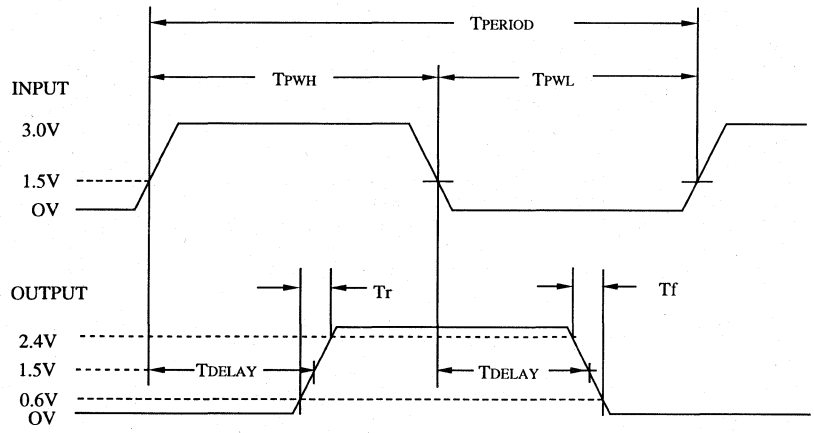

Figure 5. Timing Diagram.

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Ordering Information

Model Number	Package	Ambient Temperature Range
Bt630KP	14-pin Plastic DIP	0°C to +70°C

Section 8

PACKAGING INFORMATION

Contents

Part Numbering System

Bt458 K G 125

optional speed gradeout information. For VIDEODACs and RAMDACs, specifies MHz.

package type:

C	CERDIP
CJ	ceramic J-lead (CERQUAD)
D	ceramic sidebraze DIP
F	ceramic flatpack (with heatsink)
FN	ceramic flatpack (no heatsink)
G	ceramic PGA
L	ceramic leadless chip carrier
P	plastic DIP
PJ	plastic J-lead (PLCC)
PF	plastic Quad flatpack
S	150 mil SOIC
SW	300 mil SOIC
HJ	plastic J-lead (PLCC with heatsink)

performance gradeout:

B	–25 to +85 °C
K	0 to +70 °C (0 to +85 °C for 100K ECL)
L	0 to +70 °C, Low power
S	–55 to +125 °C

For other than standard grades, refer to the individual datasheet for letter designation.

basic model number

100–149	D/A converters
200–249	A/D converters
250–299	imaging components
300–399	reserved
400–449	graphics peripherals
450–499	RAMDACs
500–599	general components
600–699	ATE components
700–799	reserved
800–899	reserved
900–999	reserved

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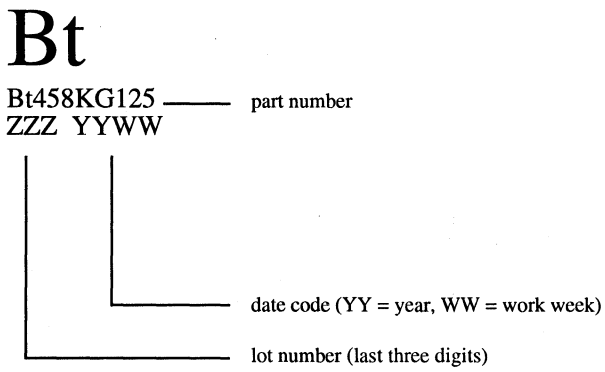
Device Marking (Top)



Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$PD = (TJ–TA) / \theta JA$$

where:

PD = power dissipation at ambient operating temperature
TJ = maximum junction operating temperature (typically 150 °C is used)
TA = maximum ambient operating temperature (free air)
θ JA = typical thermal resistance of junction to ambient (°C/ W)

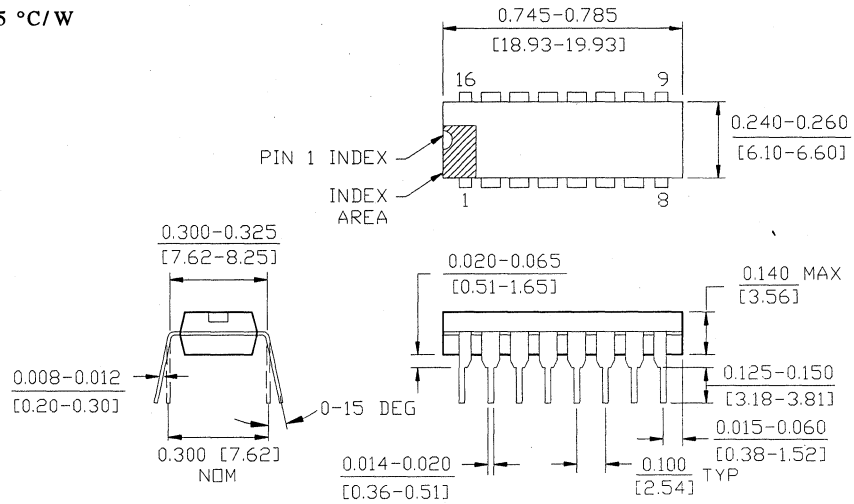
Packaging Notes

1. Unless otherwise indicated, all thermal impedances listed are typical range values or values in static free air for the package only. These impedances will vary when additional heat-sinking capability is provided through PCB solder attachment or air flow.

Plastic DIP Packages

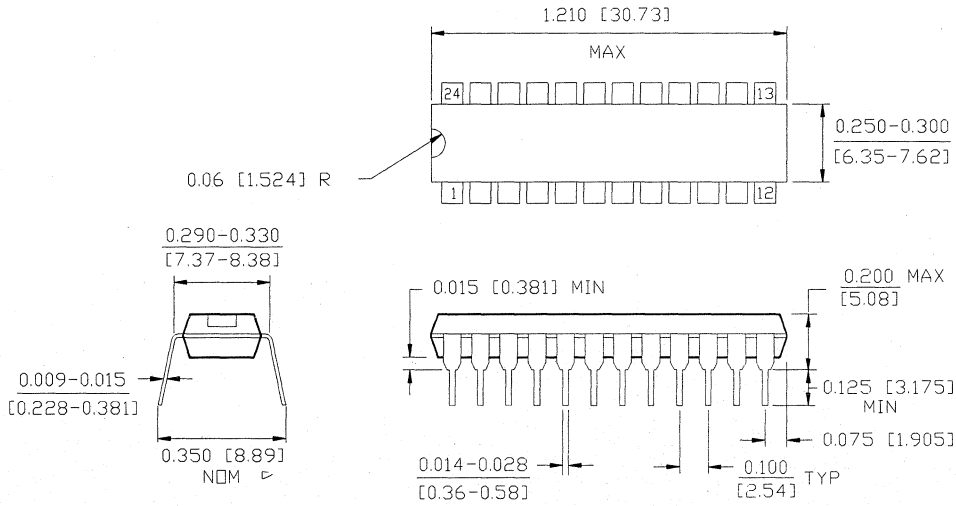
16-Pin 0.3" Plastic DIP

θJA = 75 °C/W



24-Pin 0.3" Plastic DIP

θJA = 60 °C/W



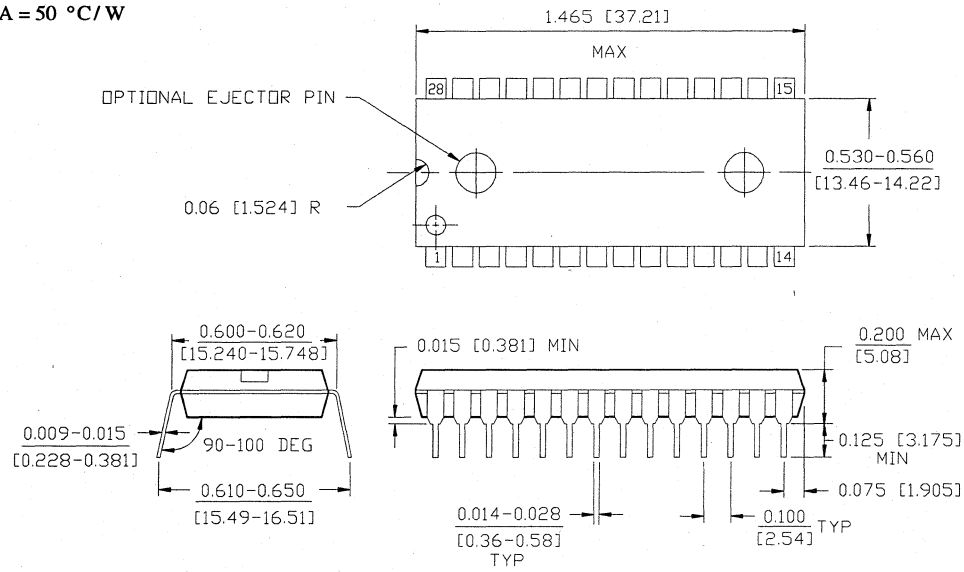
NOTES—Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

Plastic DIP Packages (continued)

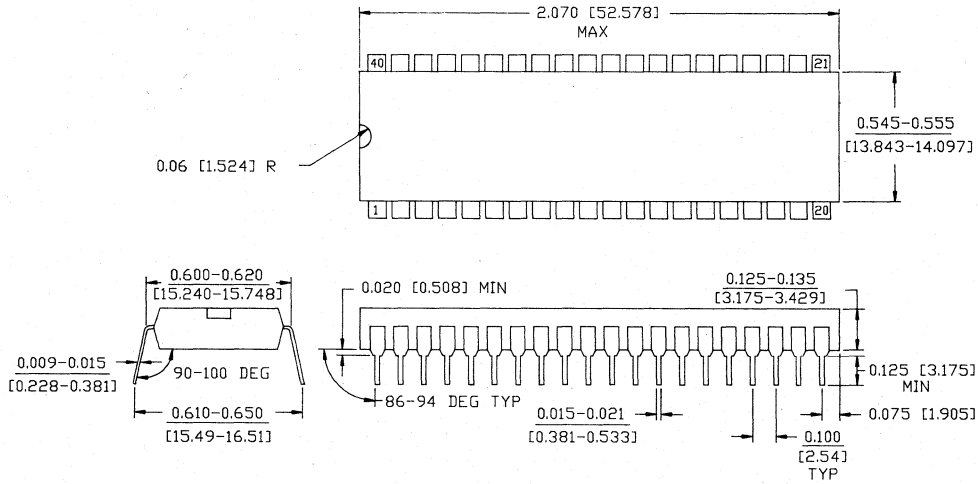
28-Pin 0.6" Plastic DIP

θJA = 50 °C/W



40-Pin 0.6" Plastic DIP

θJA = 45 °C/W

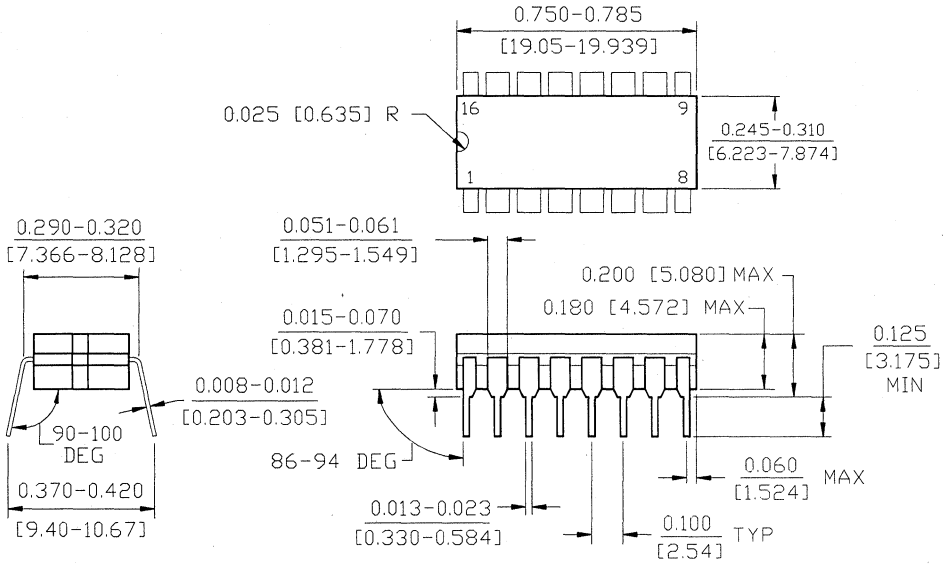


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

CERDIP Packages

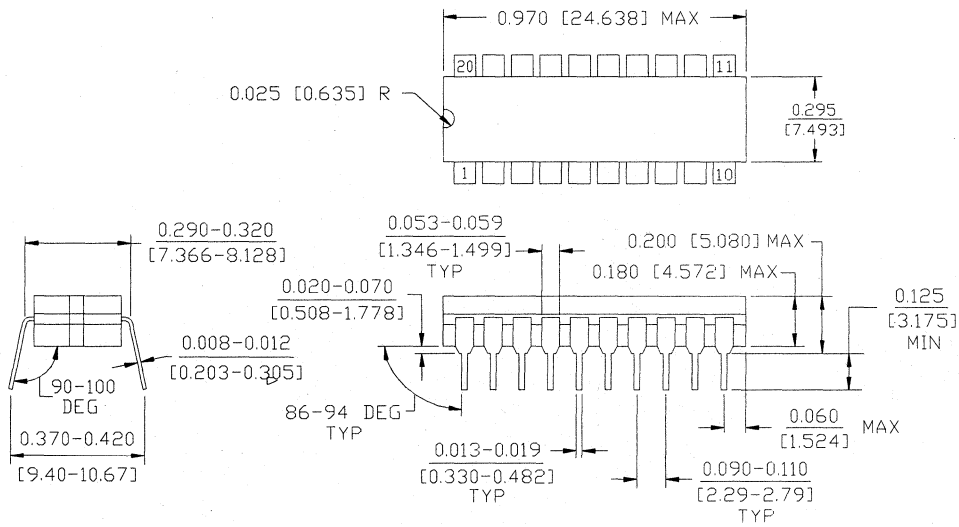
16-Pin 0.3" CERDIP

θJA = 90–95 °C/W



20-Pin 0.3" CERDIP

θJA = 85–90 °C/W



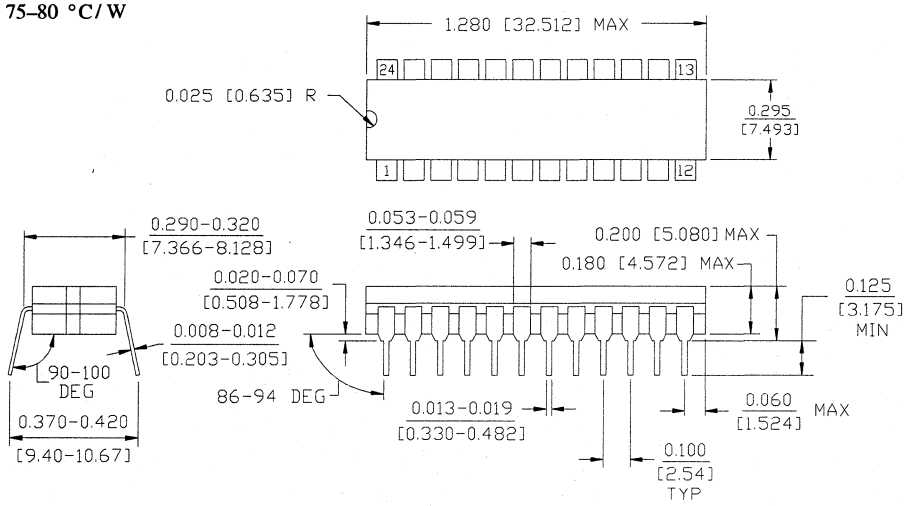
NOTES—Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

CERDIP Packages (continued)

24-Pin 0.3" CERDIP

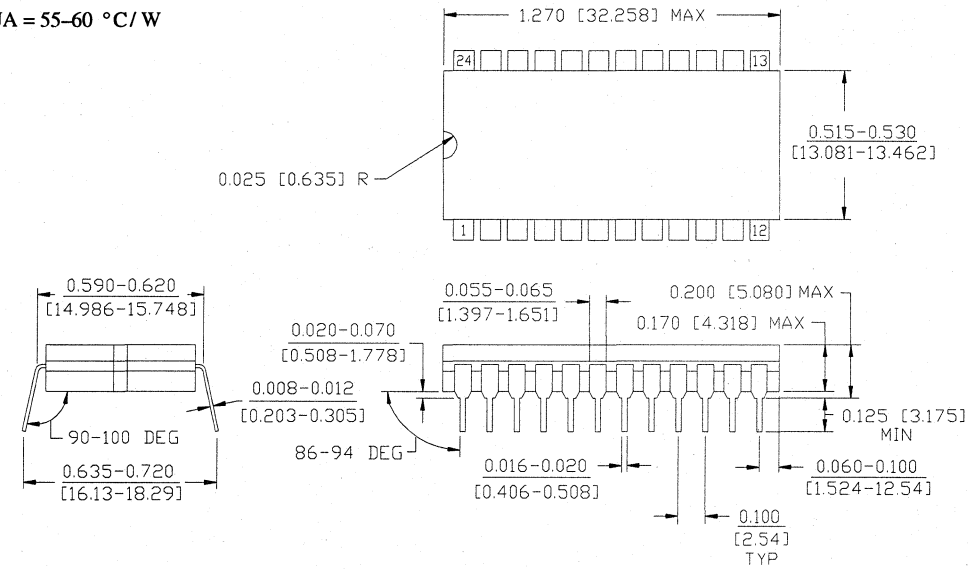
θJA = 75–80 °C/W



NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

24-Pin 0.6" CERDIP

θJA = 55–60 °C/W



NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

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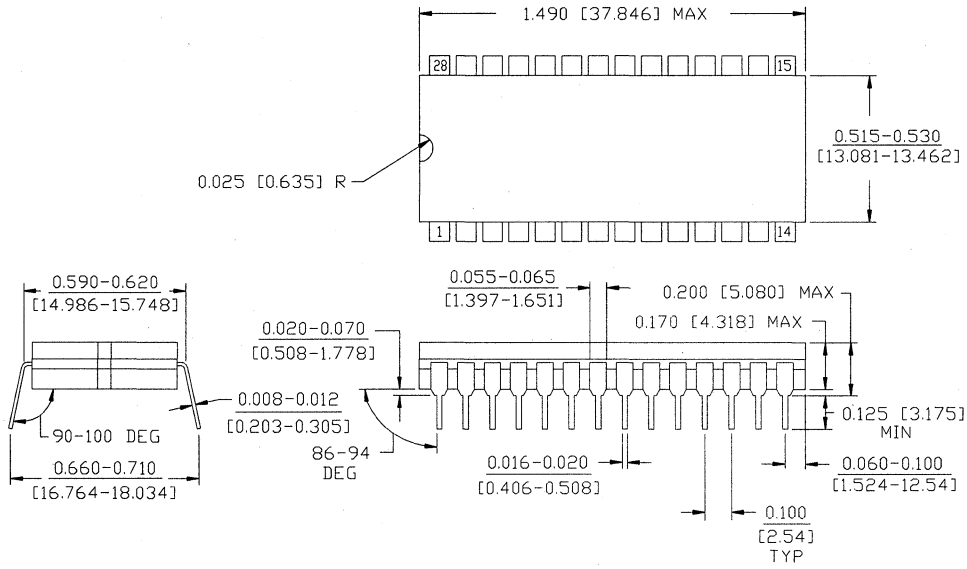
CERDIP Packages (continued)

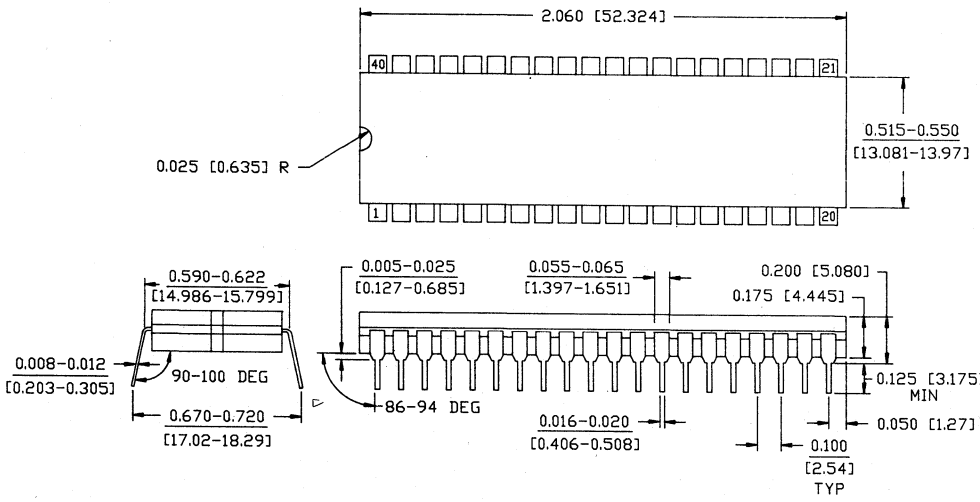
28-Pin 0.6" CERDIP

θ JA = 55–60 °C/ W



40-Pin 0.6" CERDIP

θ JA = 50–55 °C/ W



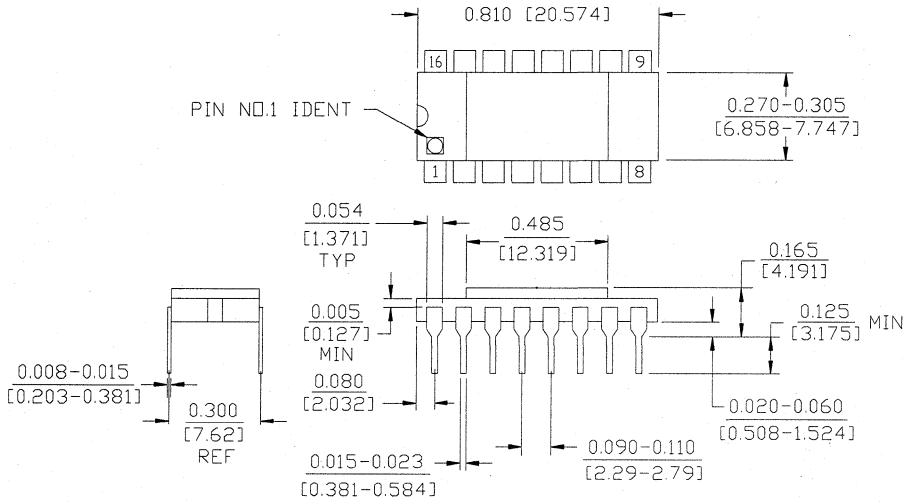
NOTES—Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Sidebraze DIP Packages

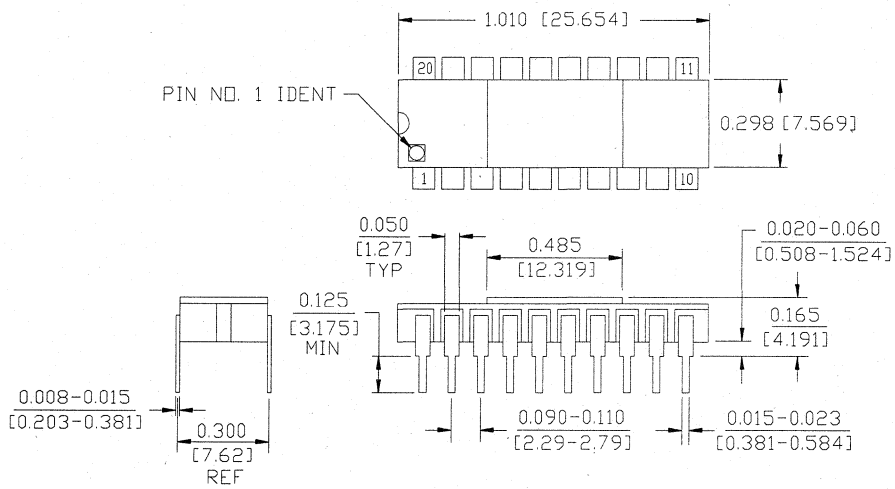
16-Pin 0.3" Ceramic Sidebraze DIP

θJA = 95 °C/W



20-Pin 0.3" Ceramic Sidebraze DIP

θJA = 85–90 °C/W

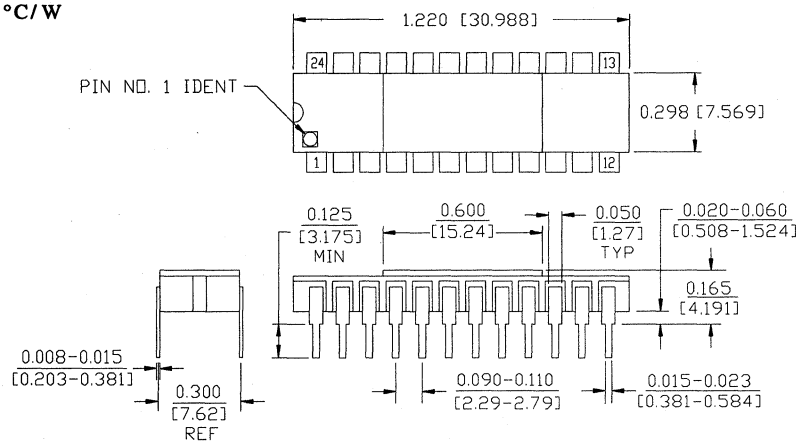


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

Ceramic Sidebraze DIP Packages (continued)

24-Pin 0.3" Ceramic Sidebraze DIP

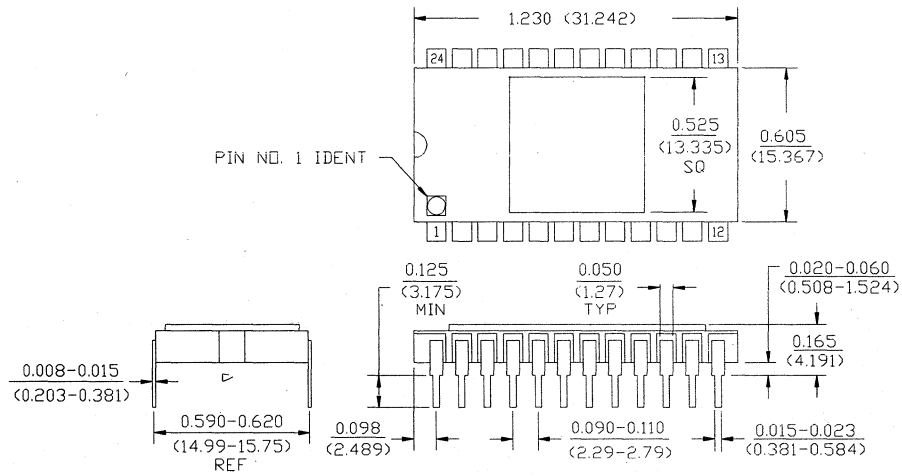
θJA = 60–65 °C/W



NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

24-Pin 0.6" Ceramic Sidebraze DIP

θJA = 55–60 °C/W

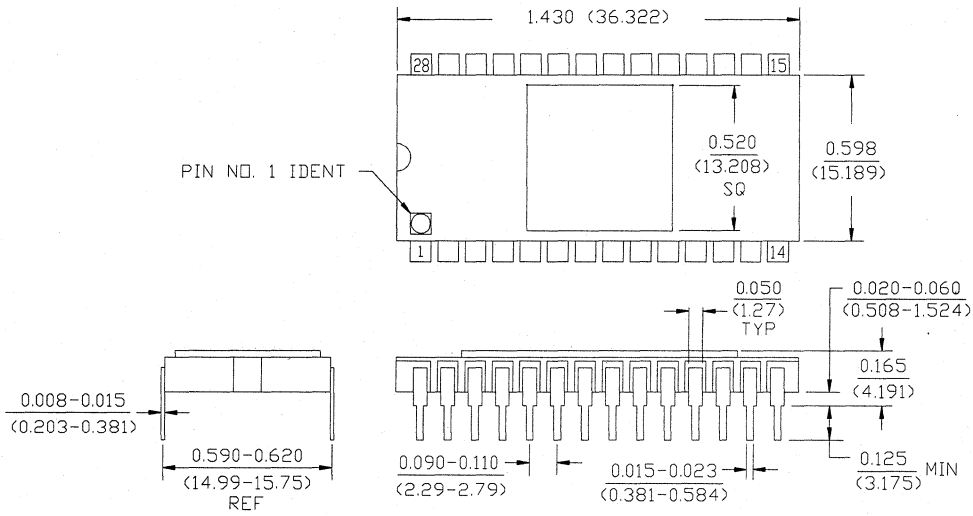


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Sidebraze DIP Packages (continued)

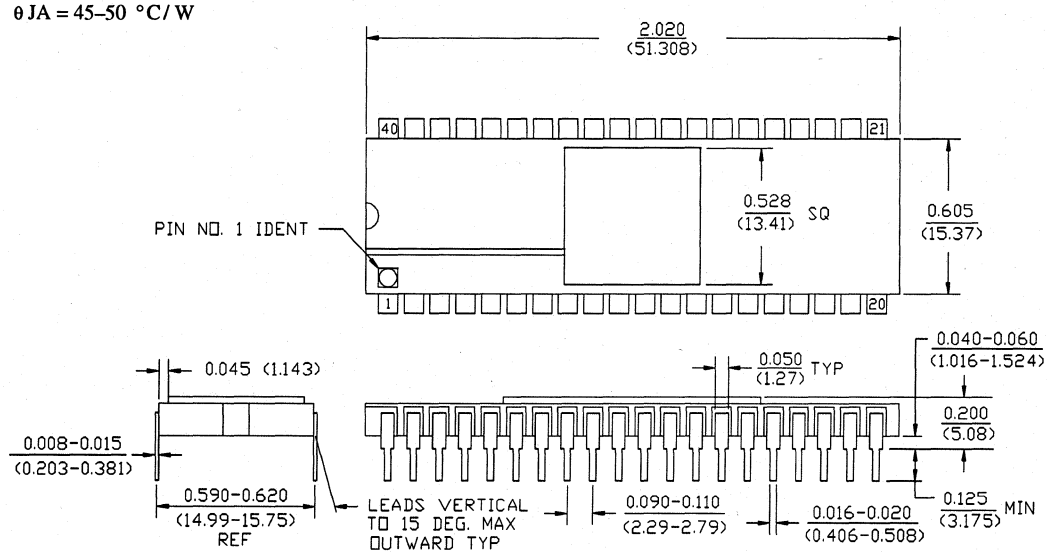
28-Pin 0.6" Ceramic Sidebraze DIP

θJA = 50–55 °C/W



40-Pin 0.6" Ceramic Sidebraze DIP

θJA = 45–50 °C/W

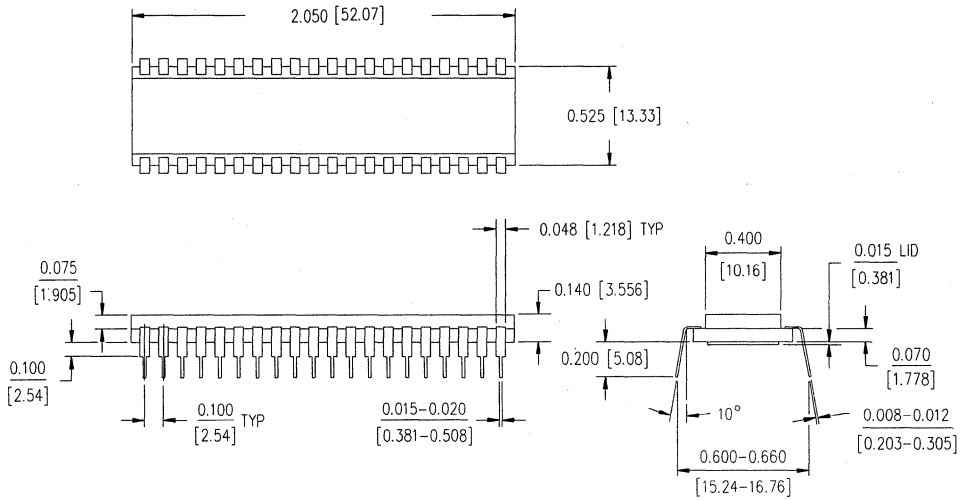


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Cavity Down DIP Packages

40-Pin 0.6" Ceramic Cavity Down DIP

θ JA = 30–40 °C/ W

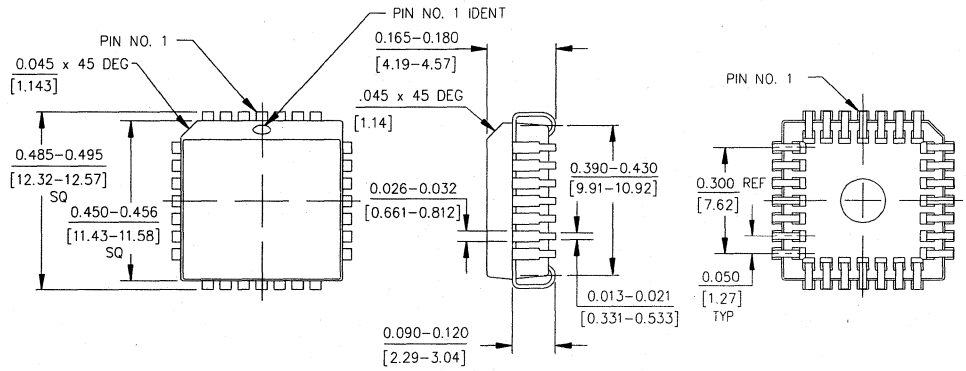


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Plastic J-Lead (PLCC) Packages

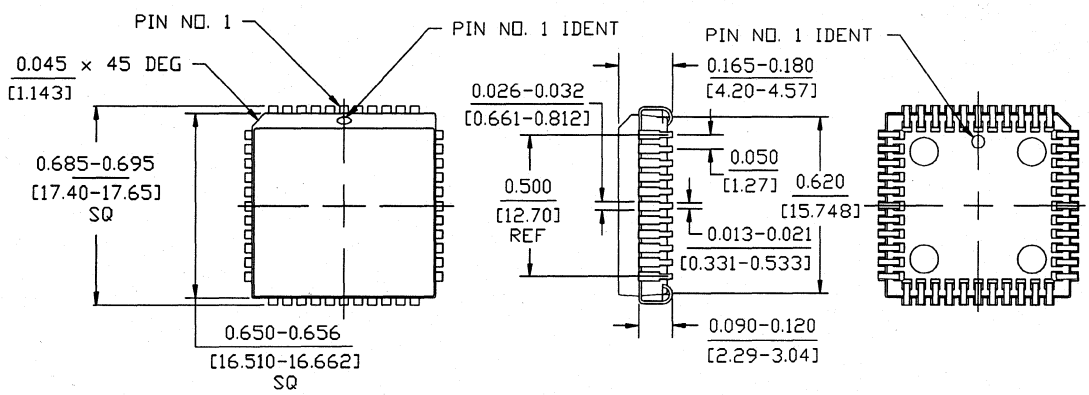
28-Pin Plastic J-Lead

θJA = 65–70 °C/W



44-Pin Plastic J-Lead

θJA = 50–55 °C/W

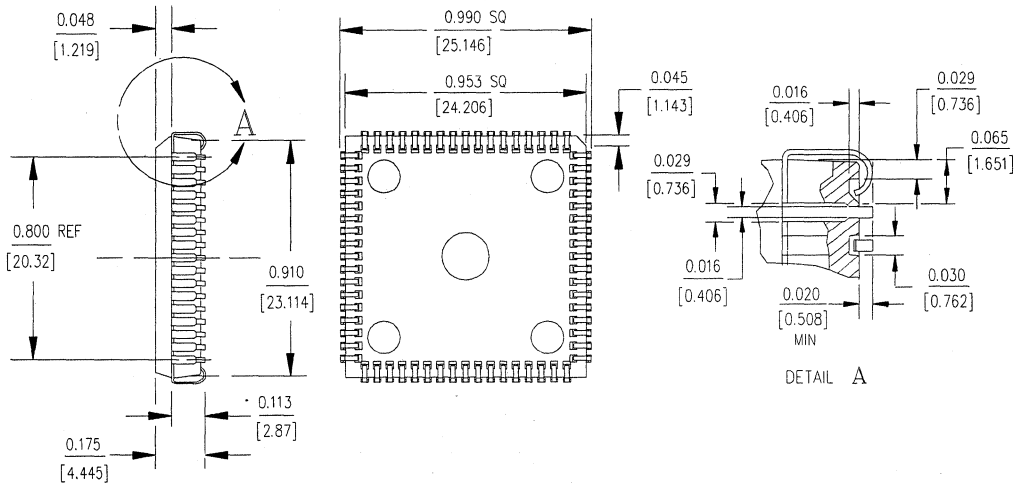


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

68-Pin Plastic J-Lead

θJA = 45–50 °C/W

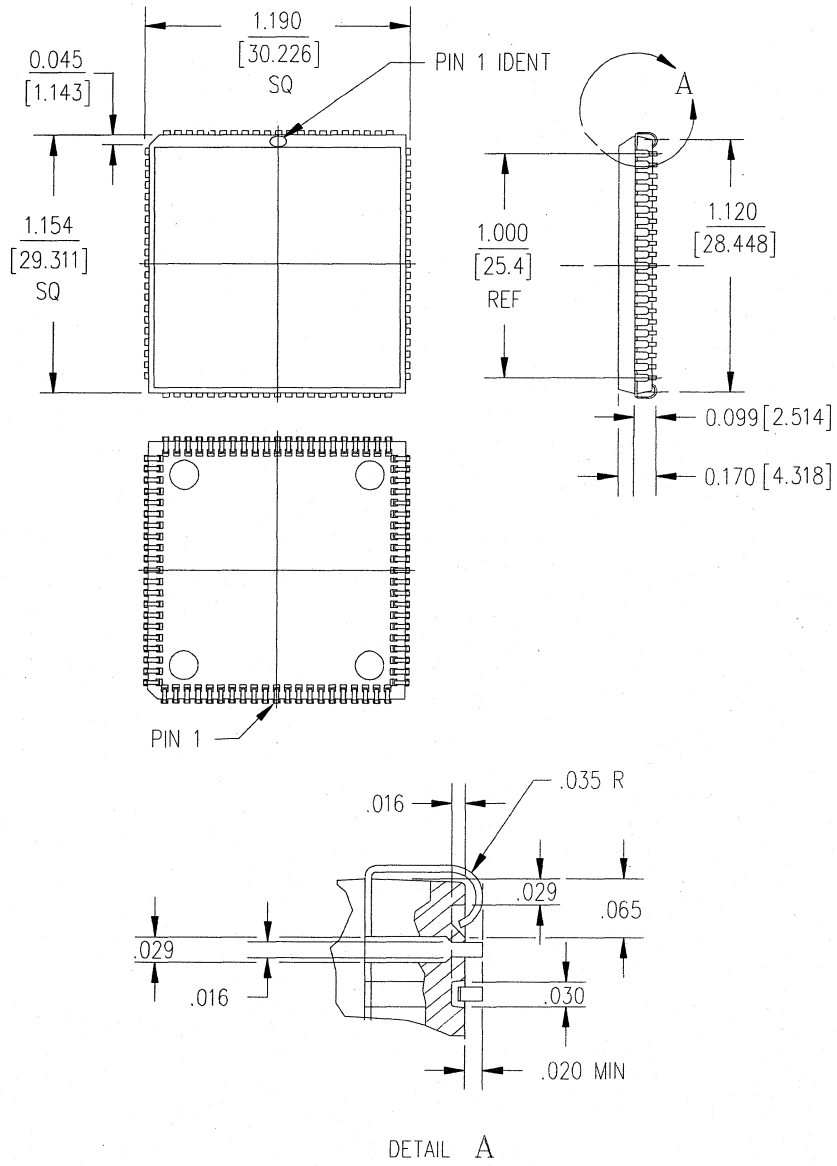


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

84-Pin Plastic J-Lead

θ JA = 35–40 °C/ W

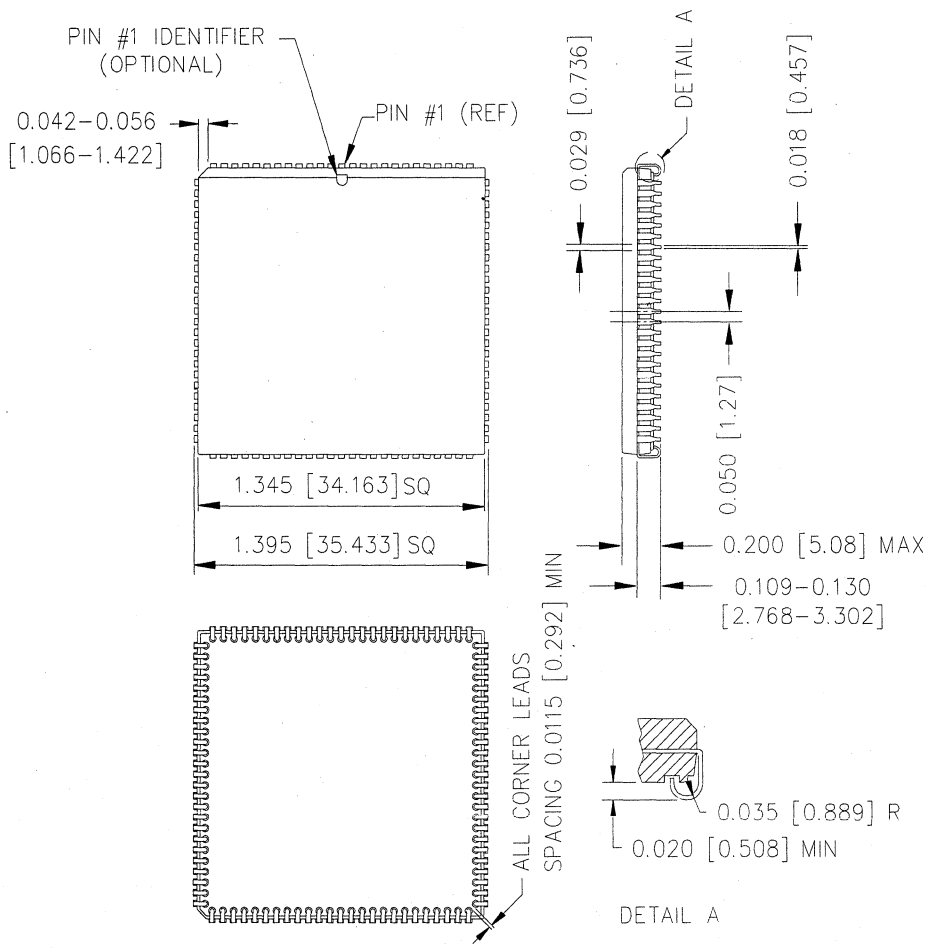


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

100-Pin Plastic J-Lead

θ JA = To be determined.

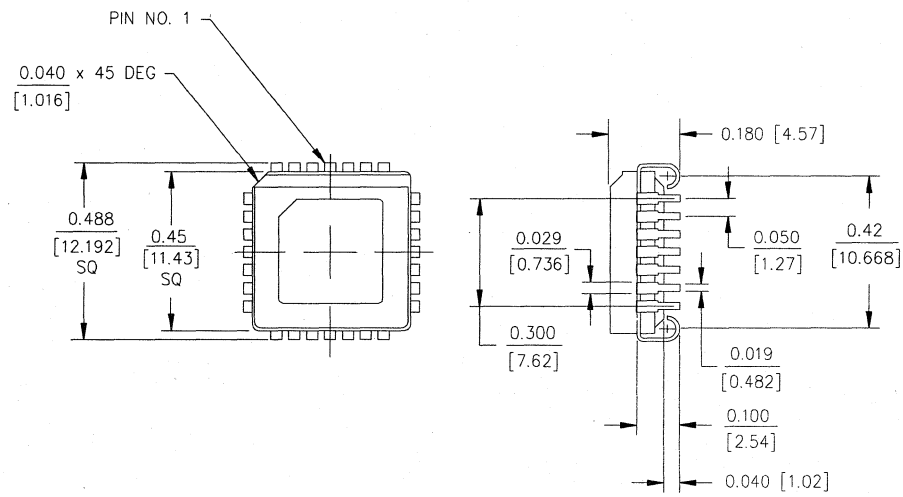


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ceramic J-Lead (CERQUAD) Packages

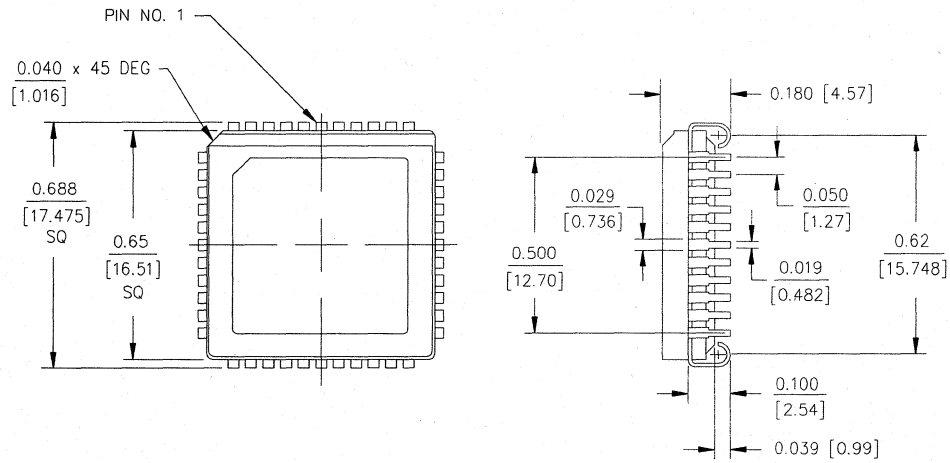
28-Pin Ceramic J-Lead

θ JA = 75–80 °C/ W



44-Pin Ceramic J-Lead

θ JA = 58–62 °C/ W

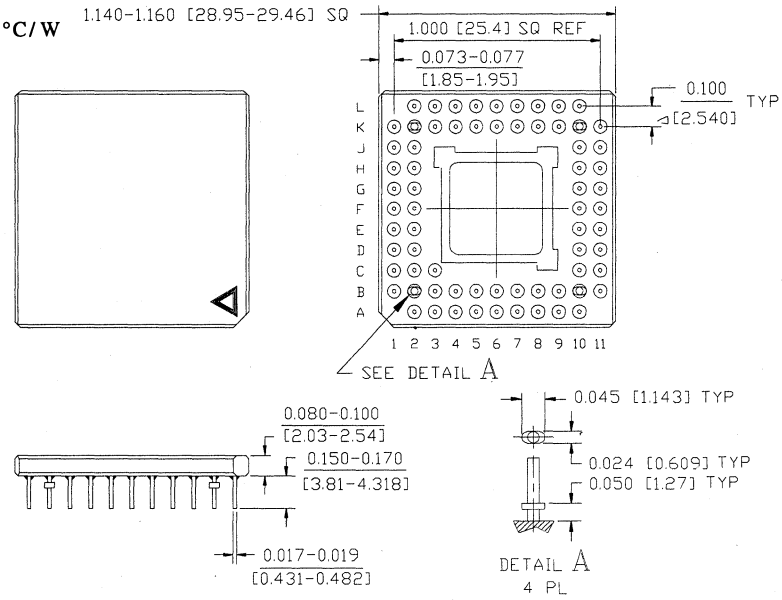


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XX ± 0.01 [0.254] .XXX ± 0.005 [0.127]
3. CERQUAD packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ceramic Pin Grid Array (PGA) Packages

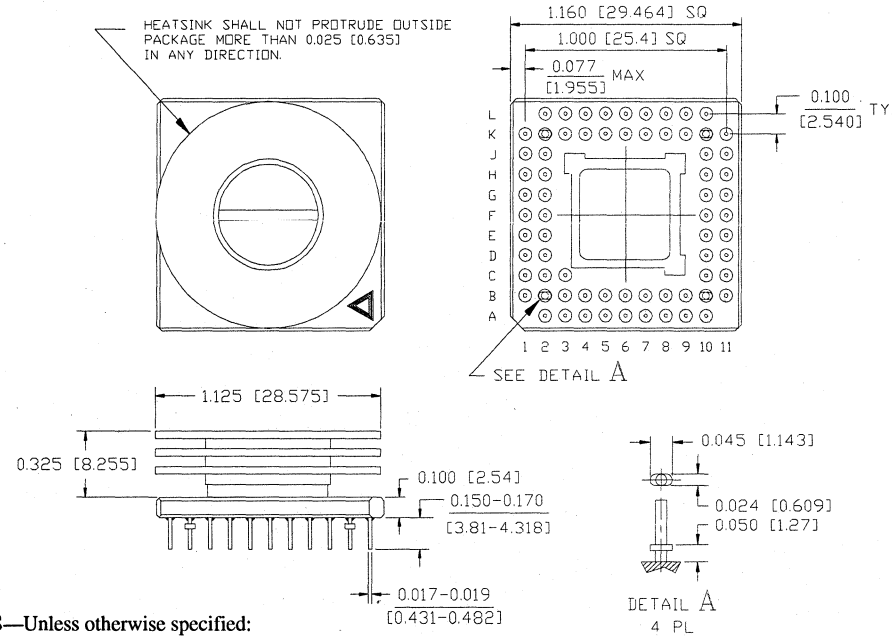
68-Pin Ceramic PGA

θJA = 35–40 °C/W



68-Pin Ceramic PGA with Heatsink and Alignment Pin

θJA = 25–28 °C/W

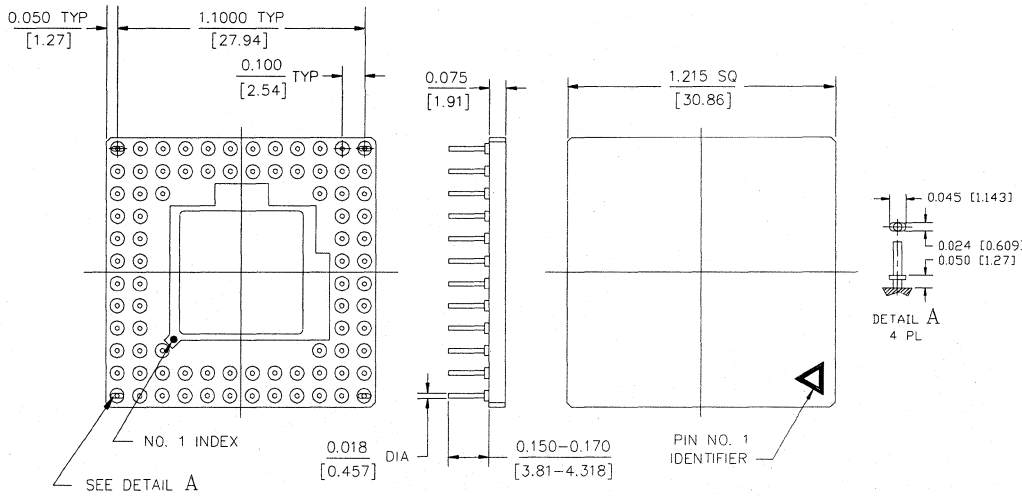


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Pin Grid Array (PGA) Packages (continued)

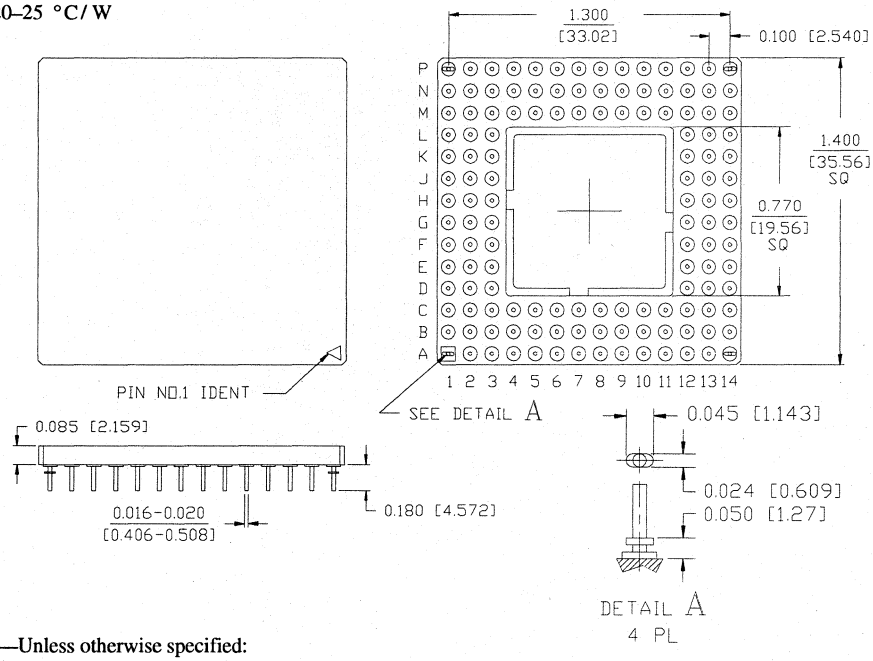
84-Pin Ceramic PGA

θJA = 30–35 °C/W



132-Pin Ceramic PGA

θJA = 20–25 °C/W



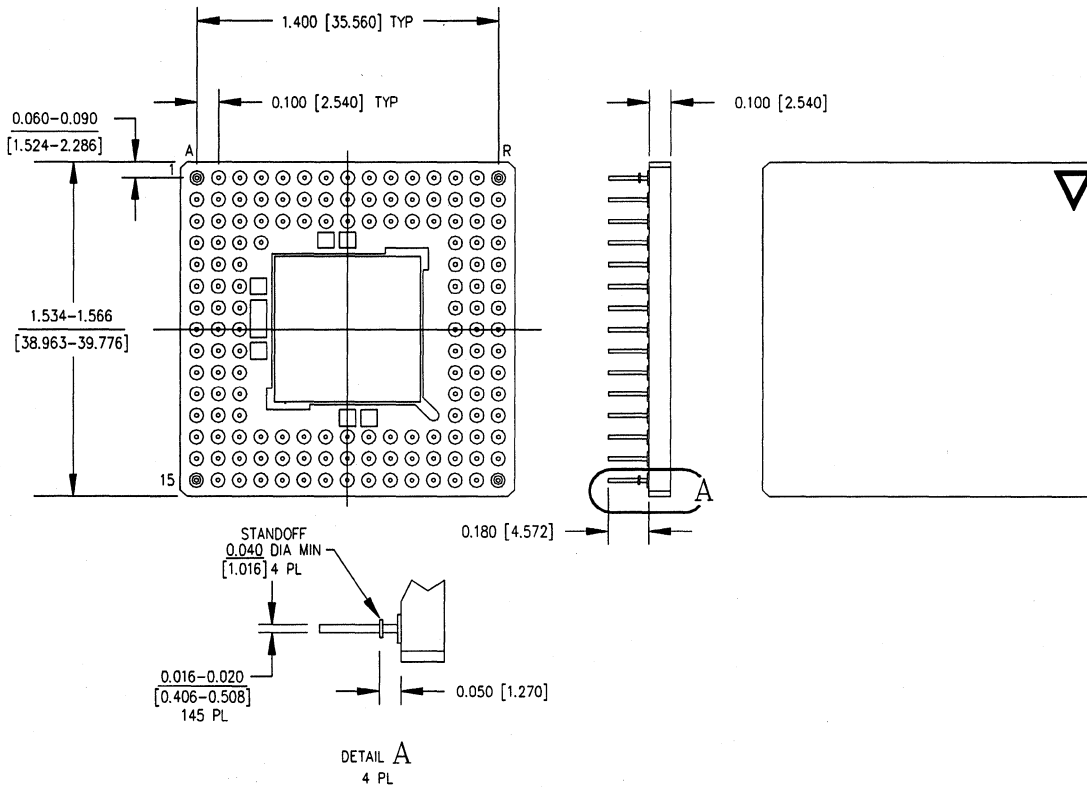
NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

8

Ceramic Pin Grid Array (PGA) Packages (continued)

144-Pin Ceramic PGA with Alignment Pin

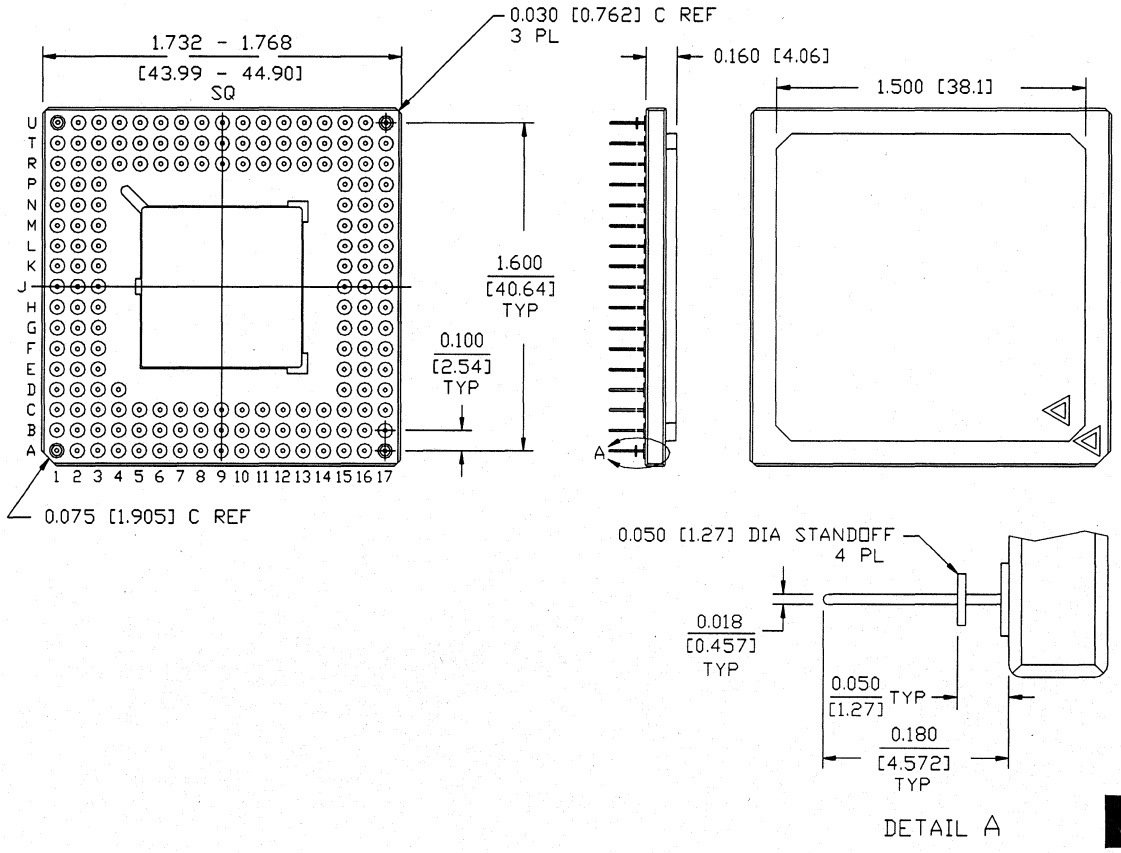
θJA = 18–23 °C/W



NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Pin Grid Array (PGA) Packages (continued)

169-Pin Ceramic PGA with Flatsink

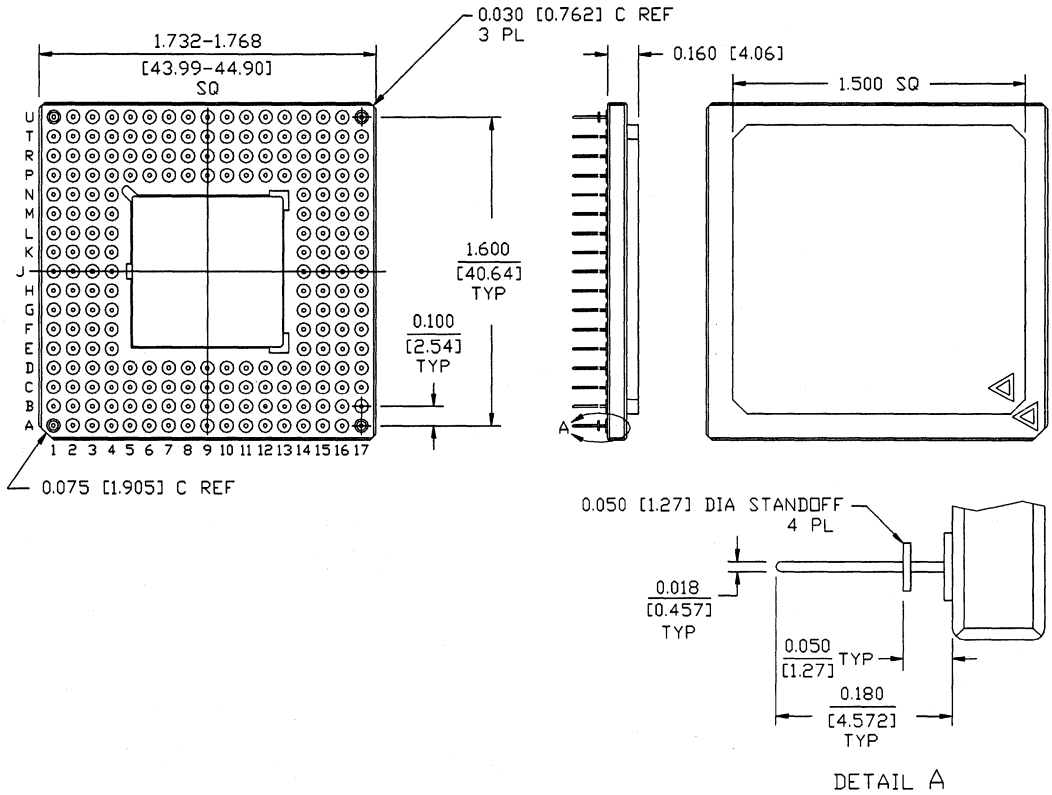


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

8

Ceramic Pin Grid Array (PGA) Packages (continued)

208-Pin Ceramic PGA with Flatsink

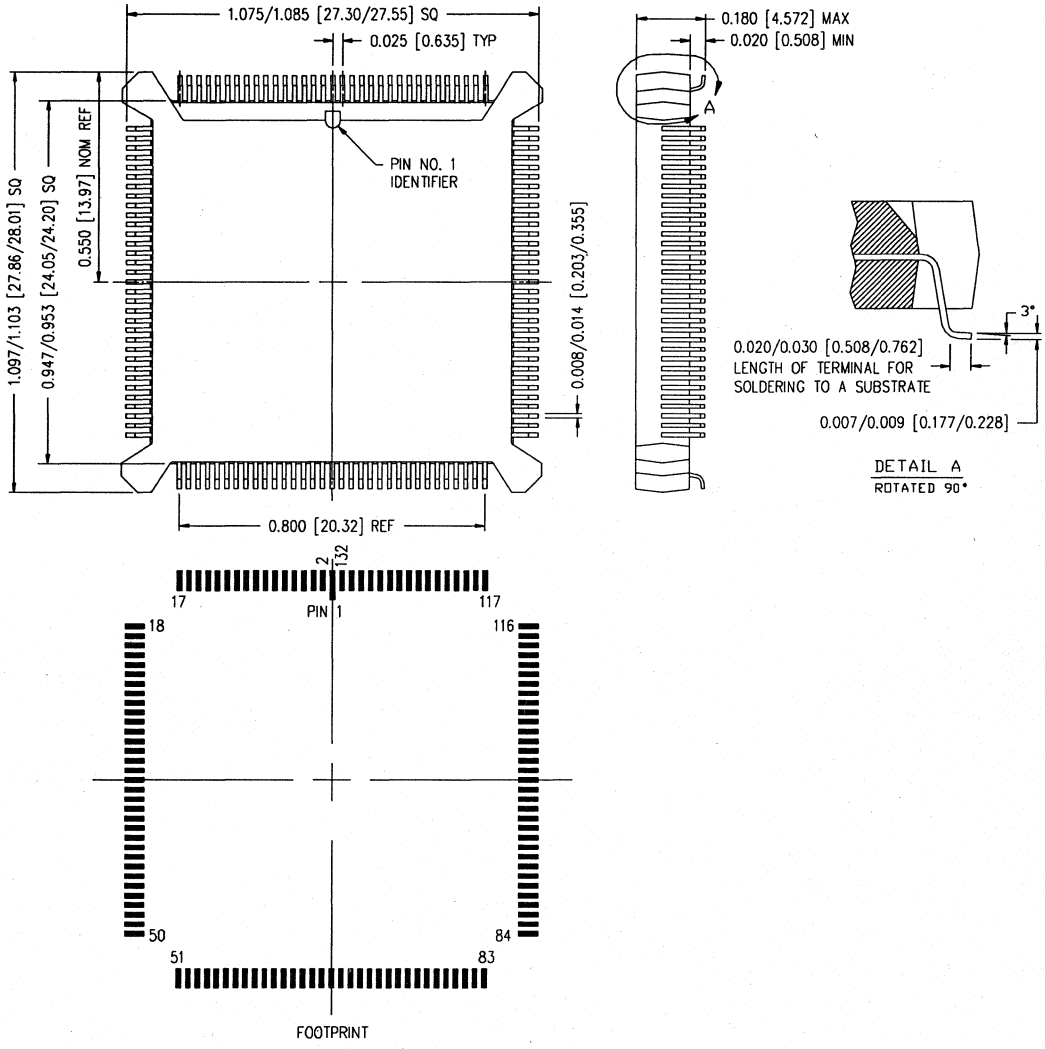


NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Plastic Quad Flatpack (PQFP) Package

132-Pin Plastic Quad Flatpack

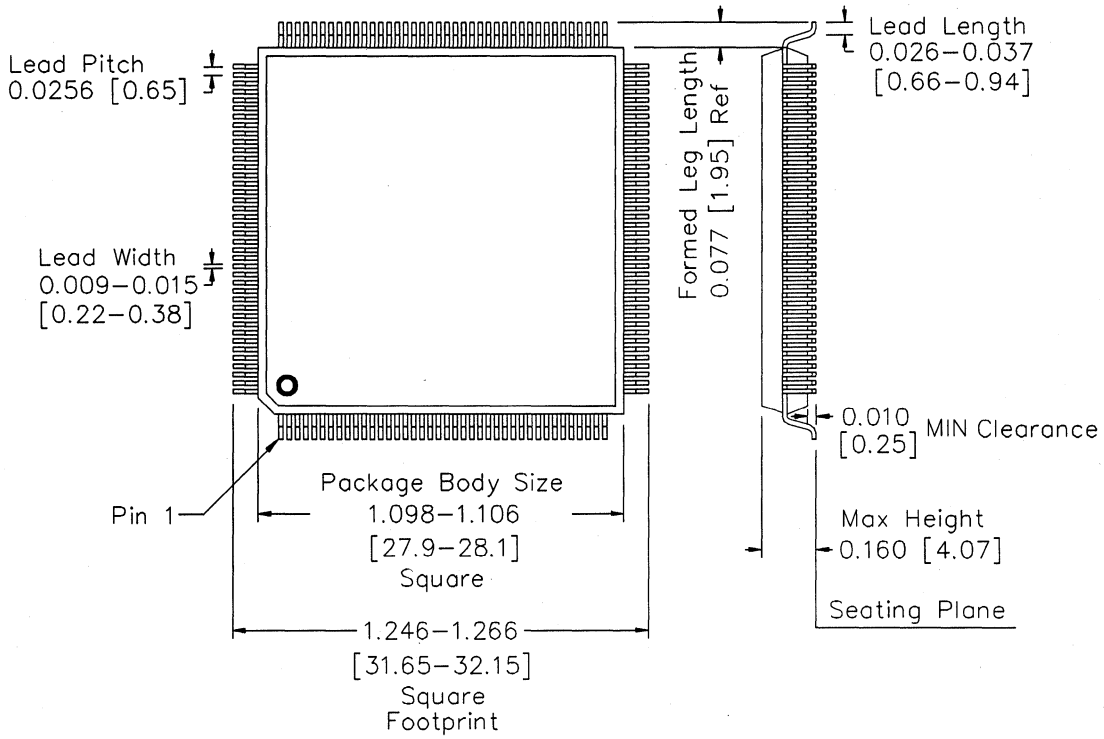
θJA = 35–40 °C/W



8

Plastic Quad Flatpack (EIAJ-PQFP) Package

160-Pin Plastic Quad Flatpack



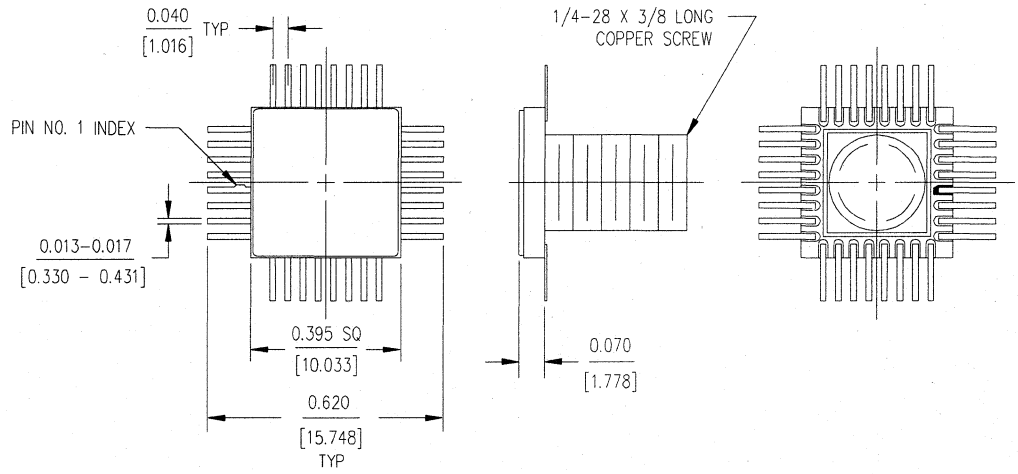
NOTES—Unless otherwise specified:

1. Dimensions are in inches [millimeters]. Millimeters are the controlling dimension.
2. Package body size does not include mold protrusion or mismatch.
3. PCB pad layout suggestions:
   a. Pad size: 0.100 x 0.012 [2.54 x 0.30].
   b. Lead pitch (millimeters): Use 0.65 center-to-center spacing.
   c. Lead pitch (inches): If the PCB layout system to be used can handle fractional mils, use 0.0256 center-to-center spacing. If not, use a combination of 0.025 (A) and 0.026 (B) inch spacings in groups of five ("ABABA" repeated) to approximate the exact spacing as closely as possible. For example, "ABABA" "ABABA" and so forth.

Ceramic Flatpack Package

32-Pin Ceramic Flatpack with Heat Sink

θJA = 30–35 °C/W



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

8

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(301) 622-1118
FAX: (301) 622-0451

Florida

Hamilton/Avnet
5371 N.W. 33rd Avenue
Suite 204
Ft. Lauderdale, FL 33309
(305) 733-6300
FAX: (305) 484 -8369

Hamilton/Avnet
3247 Tech Drive North
St. Petersburgh, FL 33716
(813) 572-4346
FAX: (813) 572-0833

Hamilton/Avnet
7079 University Blvd.
Winter Park, FL 32792
(407) 657-3300
FAX: (407) 678-4414

Marshall
380 S. North Lake Blvd., Suite #1024
Altamonte Springs, FL 32701
(407) 767-8585
FAX: (407) 767-8676

Marshall
2700 W. Cypress Creek Road
Suite D114
Ft. Lauderdale, FL 33309
(305) 977-4880
FAX: (305) 977-4887

Marshall
2840 Scherer Dr., Suite 410
St. Petersburg, FL 33716
(813) 573-1399
FAX: (813) 573-0069

Georgia

Hamilton/Avnet
3425 Corporate Way
Suite G
Duluth, GA 30136
(404) 623-5475
FAX: (404) 623-5490

Marshall
5300 Oakbrook Parkway #140
Norcross, GA 30093
(404) 923-5750
FAX: (404) 923-2743

Idaho

Anthem
1907 120th Ave. NE
Suite 102
Bothell, WA 98011
(206) 483-1700
FAX: (206) 486-0571

Hamilton/Avnet
17761 N.E. 78th Place
Building C
Redmond, WA 98052
(206) 881-6697
FAX: (206) 867-0159

Marshall
11715 Northcreek Parkway S.
Suite 112
Bothell, WA 98011
(206) 486-5747
FAX: (206) 486-6964

North American Distributors *(continued)*

Illinois

Anthem
1300 Remington Rd. Suite A
Schaumburg, IL 60173
(708) 884-0200
FAX: (708) 884-0480

Hamilton/Avnet
1130 Thorndale Avenue
Bensenville, IL 60106
(708) 860-7700
FAX: (708) 860-8530

Marshall
50 E. Commerce Dr., Unit 1
Schaumburg, IL 60173
(708) 490-0155
FAX: (708) 490-0569

Indiana

Hamilton/Avnet
655 West Carmel Drive
Suite 160
Carmel , IN 46032
(317) 844-9533
FAX: (317) 844-5921

Marshall
6990 Corporate Drive
Indianapolis, IN 46278
(317) 297-0483
FAX: (317) 297-2787

Iowa

Hamilton/Avnet
2335-A Blairs Perry Rd. N.E.
Cedar Rapids, IA 52402
(319) 393-0033
FAX: (319) 393-7050

Kansas

Hamilton/Avnet
15313 W. 95th Street
Lenexa, KS 66219
(913) 888-8900
FAX: (913) 541-7951

Marshall
10413 W. 84th Terrace
Pine Ridge Business Park
Lenexa, KS 66214
(913) 492-3121
FAX: (913) 492-6205

Kentucky

Hamilton/Avnet
1847 Mercer Road, Suite G
Lexington, KY 40511
(606) 288-4911
FAX: (606) 288-4936

Marshall
3520 Park Center Drive
Dayton, OH 45414
(513) 898-4480
FAX: (513) 898-9363

Marshall
6990 Corporate Drive
Indianapolis, IN 46278
(317) 297-0483
FAX: (317) 297-2787

Louisiana

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651 N. Plano Road Suite 429
Richardson, TX 75081
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FAX: (214) 238-0237

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7079 University Blvd.
Winter Park, FL 32792
(407) 657-3300
FAX: (407) 678-4414

Marshall
3313 Memorial Parkway S.
Huntsville, AL 35801
(205) 881-9235
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Maine

Anthem
36 Jonspin Road
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(508) 657-5170
FAX: (508) 657-4761
Anthem
7168-A Columbia Gateway
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(410) 995-6640
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Hamilton/Avnet
10M Centennial Drive
Peabody, MA 01960
(508) 532-3701
FAX: (508) 532-9802

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

Marshall
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North American Distributors *(continued)*

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FAX: (508) 657-4761

Hamilton/Avnet
10M Centennial Drive
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(508) 532-3701
FAX: (508) 532-9802

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

Michigan

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41650 Gardenbrook
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(313) 347-4271
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Hamilton/Avnet
2876 28th Street S.W.
Suite 5
Grandville, MI 49418
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Marshall
31067 Schoolcraft
Livonia, MI 48150
(313) 525-5850
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Minnesota

Anthem
7646 Golden Triangle Drive
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FAX: (612) 944-3045

Hamilton/Avnet
9800 Bren Road E., Suite 410
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FAX: (612) 932-0613

Marshall
3955 Annapolis Lane
Plymouth, MN 55447
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Mississippi

Hamilton/Avnet
7079 University Blvd.
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(407) 657-3300
FAX: (407) 678-4414

Marshall
3313 Memorial Pky. South
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(205) 881-9235
FAX: (205) 881-1490

Missouri

Hamilton/Avnet
741 Goddard Avenue
Chesterfield, MO 63005
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FAX: (314) 537-4248

Marshall
3377 Hollenberg Drive
Bridgeton, MO 63044
(314) 291-4650
FAX: (314) 291-5391

North American Distributors *(continued)*

Montana

Alliance Electronics
10510 Research Ave., SE
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FAX: (505) 275-6392

Anthem
770 Wooten Road #103
Colorado Springs, CO 80915
(719) 597-4205
FAX: (719) 597-3207

Anthem
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Englewood, CO 80112
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Hamilton/Avnet
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Englewood, CO 80112
(303) 799-7800
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Marshall
12351 N. Grant Street
Thornton, CO 80241
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FAX: (303) 457-2899

Nebraska

Alliance Electronics
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FAX: (708) 860-8530

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FAX: (913) 492-6205

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FAX: (508) 532-9802

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FAX: (508) 657-5931

New Jersey Northern

Anthem
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FAX: (201) 227-9246

Hamilton/Avnet
10 Lanidex Road West
Parsippany, NJ 07054
(201) 575-3490
FAX: (201) 575-5447

Marshall
101 Fairfield Road
Fairfield, NJ 07004
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New Jersey Southern

Hamilton/Avnet
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FAX: (609) 751-2552

Marshall
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Mt. Laurel, NJ 08054
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Nevada Northern

Anthem
580 Menlo Drive Suite 8
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FAX: (916) 781-3819

Marshall
3039 Kilgore Avenue, #140
Rancho Cordova, CA 95610
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FAX: (916) 635-6044

North American Distributors *(continued)*

Nevada
Southern

Anthem
1555 W. 10th Place, Suite 101
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FAX: (602) 966-4826

Hamilton/Avnet
3170 Pullman Street
Costa Mesa, CA 92626
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FAX: (714) 641-4122

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9830 S. 51st St., Suite B121
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FAX: (505) 828-0360

Marshall
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FAX: (602) 893-9029

New York

Anthem
47 Mall Drive
Commack, NY 11725
(516) 493-2225
FAX: (516) 493-2244

Hamilton/Avnet
933 Motor Parkway
Hauppauge, NY 11788
(516) 434-7420
FAX: (516) 434-7426

Hamilton/Avnet
2060 Townline Road
Rochester, NY 14623
(716) 475-9130
FAX: (716) 475-9119

Hamilton/Avnet
100 Elwood Davis Road
North Syracuse, NY 13212
(315) 453-4000
FAX: (315) 453-4010

Marshall
275 Oser Avenue
Hauppauge, NY 11788
(516) 273-2424
FAX: (516) 434-4775

Marshall
100 Marshall Drive
Endicott, NY 13760
(607) 785-2345
FAX: (607) 785-5546

Marshall
1250 Scottsville Road
Rochester, NY 14624
(716) 235-7620
FAX: (716) 235-0052

North Carolina

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3510 Spring Forest Road
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(919) 878-0819
FAX: (919) 954-0940

Marshall
5224 Green's Dairy Road
Raleigh, NC 27604
(919) 878-9882
FAX: (919) 872-2431

North Dakota

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7646 Golden Triangle Drive
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(612) 944-5454
FAX: (612) 944-3045

Hamilton/Avnet
9800 Bren Rd. E., Suite 410
Minnetonka, MN 55343
(612) 932-0678
FAX: (612) 932-0613

Marshall
3955 Annapolis Lane
Plymouth, MN 55447
(612) 559-2211
FAX: (612) 559-8321

North American Distributors *(continued)*

Ohio

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2600 Corp. Exchange Drive
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FAX: (614) 882-8650

Hamilton/Avnet
7760 Washington Village Dr.
Dayton, OH 45459
(513) 439-6721
FAX: (513) 439-6711

Hamilton/Avnet
30325 Bainbridge Road
Building A
Solon, OH 44139
(216) 349-4910
FAX: (216) 349-1766

Marshall
3520 Park Center Drive
Dayton, OH 45414
(513) 898-4480
FAX: (513) 898-9363

Marshall
30700 Bainbridge Road
Unit A
Solon, OH 44139
(216) 248-1788
FAX: (216) 248-2312

Oklahoma

Hamilton/Avnet
12101 E. 51st Street
Suite 106
Tulsa, OK 74146
(918) 252-7297
FAX: (918) 250-8763

Oregon

Anthem
9090 SW Gemini Drive
Beaverton, OR 97005
(503) 643-1114
FAX: (503) 626-7928

Hamilton/Avnet
9750 SW Nimbus Avenue
Beaverton, OR 97005
(503) 526-6200
FAX: (503) 641-5939

Marshall
9705 SW Gemini Dr.
Beaverton, OR 97005
(503) 644-5050
FAX: (503) 646-8256

Pennsylvania Eastern

Anthem
Horsham Business Center
355 Business Center Drive
Horsham, PA 19044
(215) 443-5150
FAX: (215) 675-9875

Hamilton/Avnet
1 Keystone Avenue
Building #36
Cherry Hill, NJ 08003
(609) 424-0110
FAX: (609) 751-2552

Marshall
158 Gaither Drive
Mt. Laurel, NJ 08054
(609) 234-9100
FAX: (609) 778-1819

Pennsylvania Western

Hamilton/Avnet
213 Executive Drive
Suite 320
Mars, PA 16046
(412) 772-1881
FAX: (412) 349-1766

Marshall
401 Parkway View Dr.
Pittsburgh, PA 15205 -1408
(412) 788-0441
FAX: (412) 788-0447

Rhode Island

Anthem
36 Jonspin Road
Wilmington, MA 01887
(508) 657-5170
FAX: (508) 657-4761

Hamilton/Avnet
10M Centennial Drive
Peabody, MA 01960
(508) 532-3701
FAX: (508) 532-9802

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

South Carolina

Hamilton/Avnet
3510 Spring Forest Road
Raleigh, NC 27604
(919) 878-0819
FAX: (919) 954-0940

Marshall
5224 Green's Dairy Road
Raleigh, NC 27604
(919) 878-9882
FAX: (919) 872-2431

North American Distributors *(continued)*

South Dakota

Anthem
7646 Golden Triangle Drive
Eden Prairie, MN 55344
(612) 944-5454
FAX: (612) 944-3045

Hamilton/Avnet
9800 Bren Rd. E., Suite 410
Minnetonka, MN 55343
(612) 932-0678
FAX: (612) 932-0613

Marshall
3955 Annapolis Lane
Plymouth, MN 55447
(612) 559-2211
FAX: (612) 559-8321

Tennessee

Hamilton/Avnet
7079 University Blvd.
Winter Park, FL 32792
(407) 657-3300
FAX: (407) 678-4414

Marshall
5300 Oakbrook Pky. #140
Norcross, GA 30093
(404) 923-5750
FAX: (404) 923-2743

Marshall
3313 Memorial Pky. S.
Huntsville, AL 35801
(205) 881-9235
FAX: (205) 881-1490

Texas

Anthem
651 N. Plano Rd. Suite 429
Richardson, TX 75081
(214) 238-7100
FAX: (214) 238-0237

Hamilton/Avnet
1826-F Kramer Lane
Austin, TX 78758
(512) 832-4306
FAX: (512) 832-4315

Hamilton/Avnet
4004 Beltline Road
Suite 200
Dallas, TX 75244
(214) 308-8105
FAX: (214) 308-8109

Hamilton/Avnet
1235 North Loop West
Suite 521
Houston, TX 77008
(713) 861-8517
FAX: (713) 861-6541

Marshall
8504 Cross Park Drive
Austin, TX 78754
(512) 837-1991
FAX: (512) 832-9810

Marshall
1551 N. Glenville Drive
Richardson, TX 75081
(214) 705-0600
FAX: (214) 705-0675

Marshall
10681 Haddington Street, Suite
#160
Houston, TX 77043
(713) 467-1666
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Utah

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1279 W. 2200 S.
Salt Lake City, UT 84119
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Hamilton/Avnet
1100 East 6600 South
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Salt Lake City, UT 84121
(801) 972-2800
FAX: (801) 263-0104

Marshall
2355 S. 1070 West, Suite D
Salt Lake City, UT 84119
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FAX: (801) 973-2296

Vermont

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36 Jonspin Road
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(508) 657-5170
FAX: (508) 657-4761

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FAX: (508) 532-9802

Marshall
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FAX: (508) 657-5931

North American Distributors *(continued)*

Virginia

Anthem
7168-A Columbia Gateway Drive
Columbia, MD 21046
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Hamilton/Avnet
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FAX: (301) 622-0451

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Redmond, WA 98052
(206) 881-6697
FAX: (206) 867-0159

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Bothell, WA 98011
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FAX: (301) 995-3553

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FAX: (414) 784-9509

Marshall
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FAX: (414) 797-8270

Wisconsin Western

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FAX: (612) 944-3045

Hamilton/Avnet
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8610 Commerce Court
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2795 Rue Halpern
St. Laurent, Quebec H4S 1P8
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Hamilton/Avnet
190 Colonnade Road
Nepean, Ontario K2E 7J5
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FAX: (613) 226-1184

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Brampton, Ontario L6T 5G3
(416) 458-8046
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Marshall
148 Brunswick Blvd.
Point Claire, Quebec H9R 5P9
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Hamilton/Avnet
87 De Diega Avenue
San Francisco Plaza #215
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Austria

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7430 Ikast
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Comodo Oy
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France

Tekelec Airtronic
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Ireland

MEMEC Ireland
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Italy

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The Netherlands

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H.Y. Associates
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Chuo-ku
Osaka-shi 541
Tel. 81 06 266 0611
FAX: 81 06 266 0630

Nissei Electronics
Hitachi Atago Bldg.
15-12, Nishi-Shimbashi
2-Chome
Minato-ku, Tokyo 105
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VSI Promark Electronics-Melbourne
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Section 10

PRODUCT INDEX

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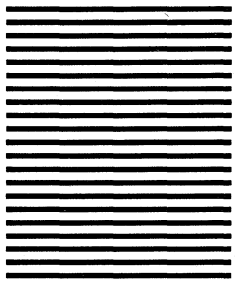

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